## Features

- **Single Voltage Read/Write Operation: 2.65V to 3.3V (BV), 3.0V to 3.6V (LV)**
- **Access Time – 70 ns**
- **Sector Erase Architecture**
  - **Fifteen 32K Word (64K Bytes) Sectors with Individual Write Lockout**
  - **Eight 4K Word (8K Bytes) Sectors with Individual Write Lockout**
- **Fast Word Program Time – 20 µs**
- **Fast Sector Erase Time – 300 ms**
- **Suspend/Resume Feature for Erase and Program**
  - **Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector**
  - **Supports Reading Any Byte/Word by Suspending Programming of Any Other Byte/Word**
- **Low-power Operation**
  - **30 mA Active**
  - **10 µA Standby**
- **$\overline{\text{Data}}$ Polling, Toggle Bit, Ready/$\overline{\text{Busy}}$ for End of Program Detection**
- **VPP Pin for Write Protection and Accelerated Program/Erase Operations**
- **$\overline{\text{RESET}}$ Input for Device Initialization**
- **Sector Lockdown Support**
- **TSOP and CBGA Package Options**
- **Top or Bottom Boot Block Configuration Available**
- **128-bit Protection Register**

## Description

The AT49BV/LV801(T) is a 3.0-volt 8-megabit Flash memory organized as 524,288 words of 16 bits each or 1,048,576 bytes of 8 bits each. The x16 data appears on I/O0 - I/O15; the x8 data appears on I/O0 - I/O7. The memory is divided into 23 sectors for erase operations. The device is offered in a 48-lead TSOP and a 48-ball CBGA packages. The device has $\overline{\text{CE}}$ and $\overline{\text{OE}}$ control signals to avoid any bus contention. This device can be read or reprogrammed using a single 2.65V power supply, making it ideally suited for in-system programming.

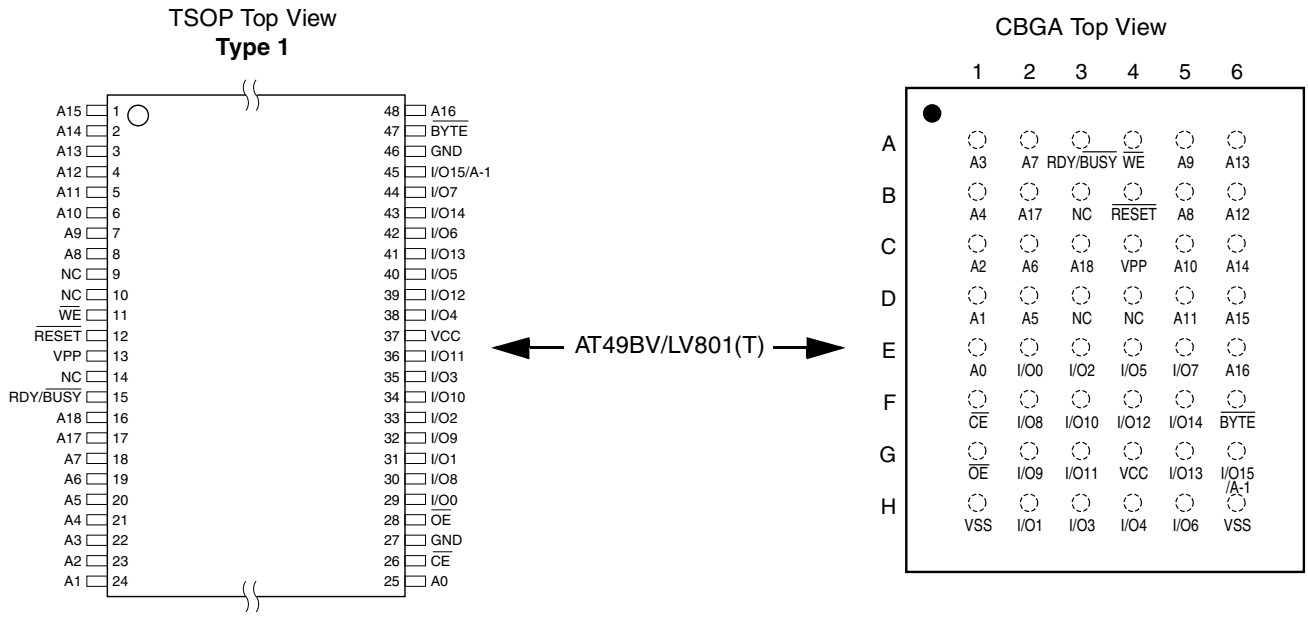
## Pin Configurations

| Pin Name | Function |
|---|---|
| A0 - A18 | Addresses |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| $\overline{\text{WE}}$ | Write Enable |
| $\overline{\text{RESET}}$ | Reset |
| RDY/$\overline{\text{BUSY}}$ | READY/$\overline{\text{BUSY}}$ Output |
| VPP | Write Protection and Power Supply for Accelerated Program/Erase Operations |
| I/O0 - I/O14 | Data Inputs/Outputs |
| I/O15 (A-1) | I/O15 (Data Input/Output, Word Mode)<br>A-1 (LSB Address Input, Byte Mode) |
| $\overline{\text{BYTE}}$ | Selects Byte or Word Mode |
| NC | No Connect |

# 8-megabit (512K x 16/ 1M x 8) 3-volt Only Flash Memory

# AT49BV801
# AT49BV801T
# AT49LV801
# AT49LV801T

Rev. 3280A–FLASH–06/02




The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector. (See “Sector Lockdown” section.)

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the Erase or Program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory. The end of a program or an erase cycle is detected by the Ready/$\overline{\text{Busy}}$ pin, $\overline{\text{Data}}$ Polling or by the toggle bit.

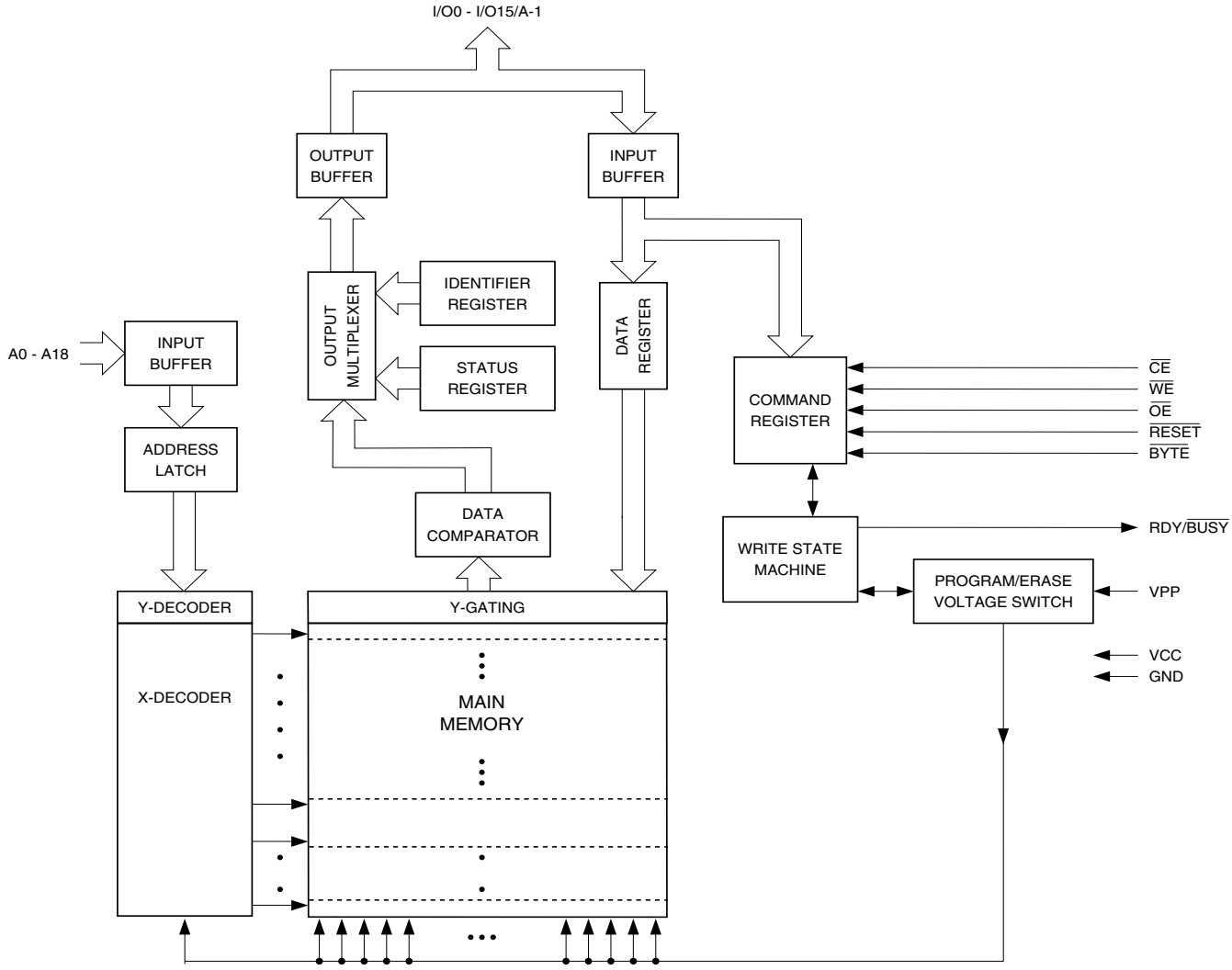
The VPP pin provides data protection and faster programming. When the $V_{PP}$ input is below 0.8V, the program and erase functions are inhibited. When $V_{PP}$ is at 1.65V or above, normal program and erase operations can be performed. With $V_{PP}$ at 5.0V or 12.0V, the program and erase operations are accelerated.

A six-byte command (Enter Single Pulse Program Mode) sequence to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Byte/Word Program) is exited by powering down the device, or by pulsing the $\overline{\text{RESET}}$ pin low for a minimum of 500 ns and then bringing it back to $V_{CC}$. Erase, Erase Suspend/Resume, and Program Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

The $\overline{\text{BYTE}}$ pin controls whether the device data I/O pins operate in the byte or word configuration. If the $\overline{\text{BYTE}}$ pin is set at logic “1”, the device is in word configuration, I/O0 - I/O15 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$.

If the $\overline{\text{BYTE}}$ pin is set at logic “0”, the device is in byte configuration, and only data I/O pins I/O0 - I/O7 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$. The data I/O pins I/O8 - I/O14 are tri-stated, and the I/O15 pin is used as an input for the LSB (A-1) address function.

## Block Diagram



## Device Operation

**READ:** The AT49BV/LV801(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high-impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

**COMMAND SEQUENCES:** When the device is first powered on, it will be reset to the read or standby mode, depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the "Command Definition in Hex" table on page 12 (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

**RESET:** A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the read or standby mode, depending upon the state of the control inputs.

**ERASURE:** Before a byte/word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase command.

**CHIP ERASE:** The entire device can be erased at one time by using the six-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is $t_{EC}$.

If the sector lockdown has been enabled, the chip erase will not erase the data in the sector that has been locked out; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

**SECTOR ERASE:** As an alternative to a full chip erase, the device is organized into 23 sectors (SA0 - SA22) that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched on the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a sector is $t_{SEC}$. When the sector programming lockdown feature is not enabled, the sector will erase (from the same Sector Erase command). An attempt to erase a sector that has been protected will result in the operation terminating in 2 µs.

**BYTE/WORD PROGRAMMING:** Once a memory block is erased, it is programmed (to a logical "0") on a byte-by-byte or on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified $t_{BP}$ cycle time. The Data Polling feature or the Toggle Bit feature may be used to indicate the end of a program cycle. If the erase/program status bit is a "1", the device was not able to verify that the erase or program operation was performed successfully.

**VPP PIN:** The circuitry of the AT49BV/LV801(T) is designed so that the device can be programmed or erased from the $V_{CC}$ power supply or from the VPP input pin. When $V_{PP}$ is greater than 1.65V and less than or equal to the VCC pin, the device selects the $V_{CC}$ supply for programming and erase operations. When the VPP pin is greater than the $V_{CC}$ supply, the device will select the $V_{PP}$ input as the power supply for programming and erase operations. The device will allow for some variations between the $V_{PP}$ input and the $V_{CC}$ power supply in its selection of $V_{CC}$ or $V_{PP}$ for program or erase operations. If the VPP pin is within 0.3V of $V_{CC}$ for $2.65V < V_{CC} < 3.6V$, then the program or erase operations will use $V_{CC}$ and disregard the $V_{PP}$ input signal. When the $V_{PP}$ signal is used for program and erase operations, the $V_{PP}$ must be in the 5V ± 0.5V or 12V ± 0.5V range to ensure proper operation. The $V_{pp}$ pin cannot be left floating.

**PROGRAM/ERASE STATUS:** The device provides several bits to determine the status of a program or erase operation: I/O2, I/O3, I/O5, I/O6 and I/O7. The "Status Bit Table" on page 11 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the AT49BV/LV801(T) contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, "00" or "01". If the configuration register is set to "00", the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a "01", a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a "00" or to a "01", any unsuccessful program or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is "00". Using the four-bus cycle Set Configuration Register command as shown in the "Command Definition in Hex" table on page 12, the value of the configuration register can be changed. Voltages applied to the RESET pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

**DATA POLLING:** The AT49BV/LV801(T) features Data Polling to indicate the end of a program cycle. If the status configuration register is set to a "00", during a program cycle an attempted read of the last byte/word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. Data Polling may begin at any time during the program cycle. Please see "Status Bit Table" on page 11 for more details.

If the status bit configuration register is set to a "01", the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The $\overline{\text{Data}}$ Polling status bit must be used in conjunction with the erase/program and $V_{PP}$ status bit as shown in the algorithm in Figures 1 and 2 on page 9.

**TOGGLE BIT:** In addition to $\overline{\text{Data}}$ Polling, the AT49BV/LV801(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see "Status Bit Table" on page 11 for more details.

The toggle bit status bit should be used in conjunction with the erase/program and $V_{PP}$ status bit as shown in the algorithm in Figures 3 and 4 on page 10.

**ERASE/PROGRAM STATUS BIT:** The device offers a status bit on I/O5, which indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a "1", the device is unable to verify that an erase or a byte/word program operation has been successfully performed. The device may also output a "1" on I/O5 if the system tries to program a "1" to a location that was previously programmed to a "0". Only an erase operation can change a "0" back to a "1". If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a "1", the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a "0" while the erase or program operation is still in progress. Please see "Status Bit Table" on page 11 for more details.

**$V_{PP}$ STATUS BIT:** The AT49BV/LV801(T) provides a status bit on I/O3, which provides information regarding the voltage level of the VPP pin. During a program or erase operation, if the voltage on the VPP pin is not high enough to perform the desired operation successfully, the I/O3 status bit will be a "1". Once the $V_{PP}$ status bit has been set to a "1", the system must write the Product ID Exit command to return to the read mode. On the other hand, if the voltage level is high enough to perform a program or erase operation successfully, the $V_{PP}$ status bit will output a "0". Please see "Status Bit Table" on page 11 for more details.

**SECTOR LOCKDOWN:** Each sector has a programming lockdown feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockdown feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector's usage as a write-protected region is optional to the user.

At power-up or reset, all sectors are unlocked. To activate the lockdown for a specific sector, the six-bus cycle Sector Lockdown command must be issued. Once a sector has been locked down, the contents of the sector is read-only and cannot be erased or programmed.

**SECTOR LOCKDOWN DETECTION:** A software method is available to determine if programming of a sector is locked down. When the device is in the software product identification mode (see "Software Product Identification Entry/Exit" sections on page 23), a read from address location 00002H within a sector will show if programming the sector is locked down. If the data on I/O0 is low, the sector can be programmed; if the data on I/O0 is high, the program lockdown feature has been enabled and the sector cannot be programmed. The software product identification exit code should be used to return to standard operation.

**SECTOR LOCKDOWN OVERRIDE:** The only way to unlock a sector that is locked down is through reset or power-up cycles. After power-up or reset, the content of a sector that is locked down can be erased and reprogrammed.

**ERASE SUSPEND/ERASE RESUME:** The Erase Suspend command allows the system to interrupt a sector erase or chip erase operation and then program or read data from a different sector within the memory. After the Erase Suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

**PROGRAM SUSPEND/PROGRAM RESUME:** The Program Suspend command allows the system to interrupt a programming operation and then read data from a different byte/word within the memory. After the Program Suspend command is given, the device requires a maximum of 15 µs to suspend the programming operation. After the programming operation has been suspended, the system can then read data from any other byte/word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same.

**PRODUCT IDENTIFICATION:** The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see “Operating Modes” on page 16 (for hardware operation) or “Software Product Identification Entry/Exit” on page 23. The manufacturer and device codes are the same for both modes.

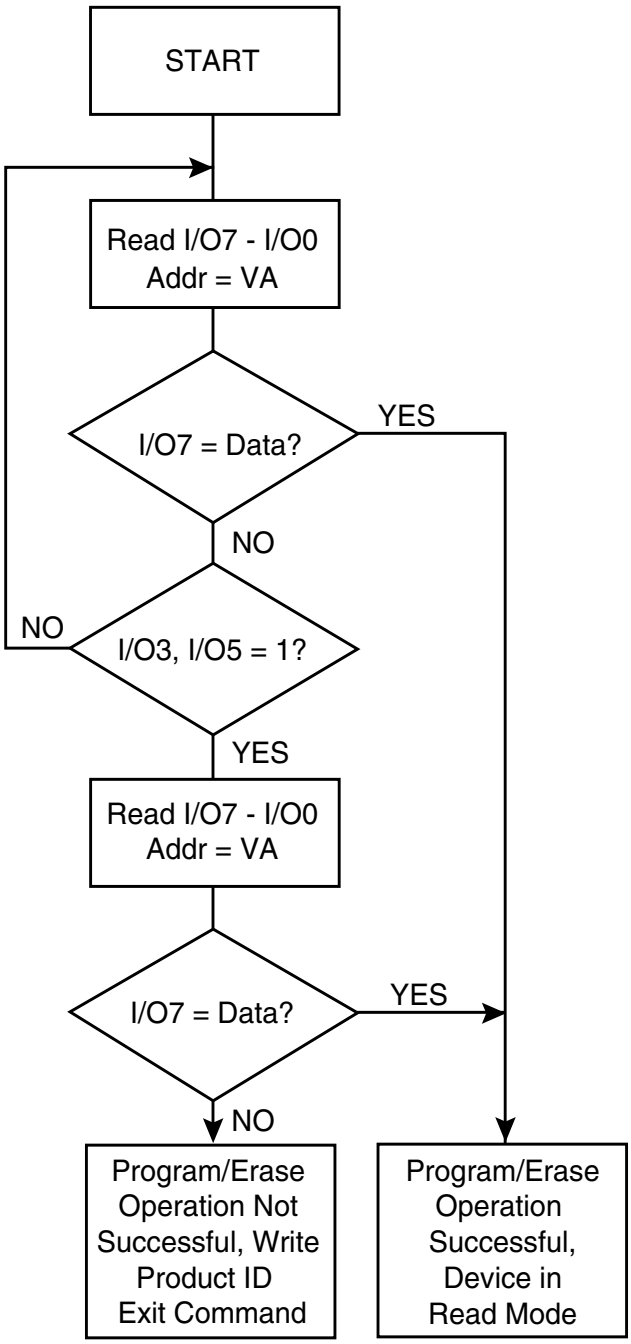
**128-BIT PROTECTION REGISTER:** The AT49BV/LV801(T) contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the “Command Definition in Hex” table on page 12. To lock out block B, the four-bus cycle Lock Protection Register command must be used as shown in the “Command Definition in Hex” table on page 12. Data bit D1 must be zero during the fourth bus cycle. All other data bits during the fourth bus cycle are don’t cares. To determine whether block B is locked out, the Product ID Entry command is given followed by a read operation from address 80H. If data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. Please see the “Protection Register Addressing Table” on page 13 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether block B is protected or not, or reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

**RDY/$\overline{\text{BUSY}}$:** An open-drain READY/$\overline{\text{BUSY}}$ output pin provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open-drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line. Please see "Status Bit Table" on page 11 for more details.

**HARDWARE DATA PROTECTION:** The Hardware Data Protection feature protects against inadvertent programs to the AT49BV/LV801(T) in the following ways: (a) $V_{CC}$ sense: if $V_{CC}$ is below 1.8V (typical), the program function is inhibited. (b) $V_{CC}$ power-on delay: once $V_{CC}$ has reached the $V_{CC}$ sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle. (e) Program inhibit: $V_{PP}$ is less than $V_{ILPP}$. (f) $V_{PP}$ power-on delay: once $V_{PP}$ has reached 1.65V, program and erase operations can occur after 100 ns.

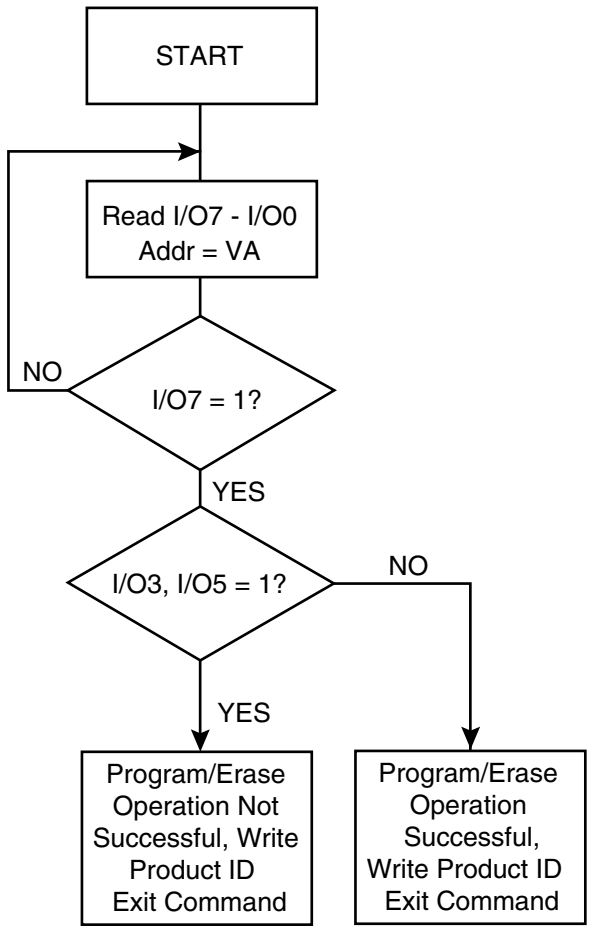
**INPUT LEVELS:** While operating with a 2.65V to 3.6V power supply, the address inputs and control inputs ($\overline{\text{OE}}$, $\overline{\text{CE}}$ and $\overline{\text{WE}}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to $V_{CC}$ + 0.6V.

**Figure 1.** $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 00)



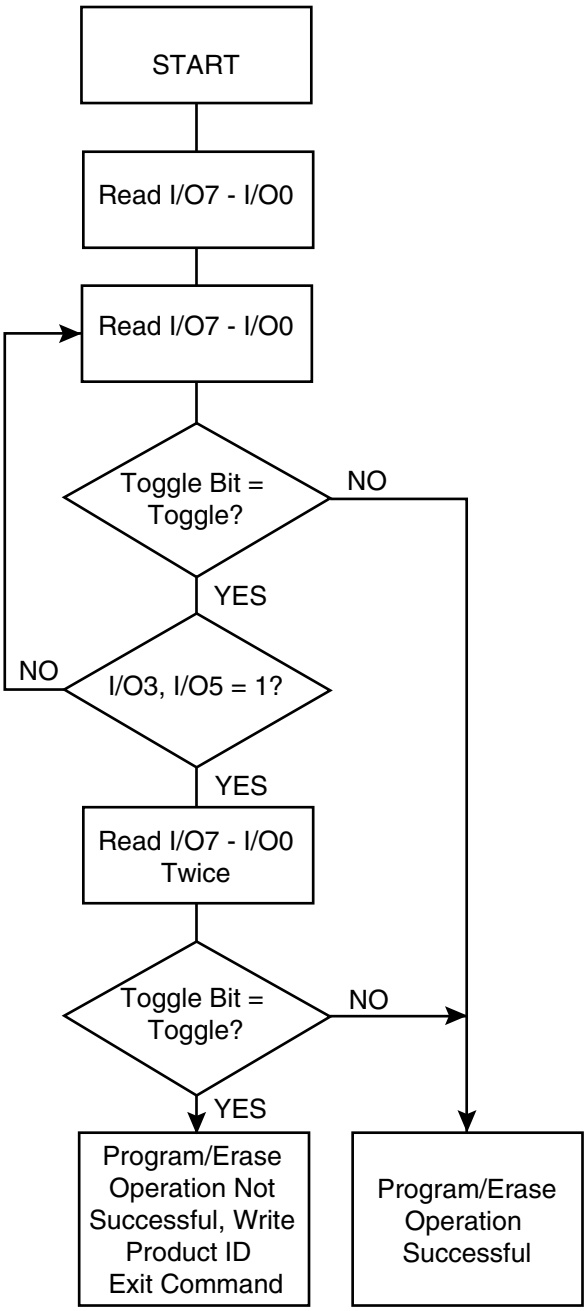

Notes: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

**Figure 2.** $\overline{\text{Data}}$ Polling Algorithm
(Configuration Register = 01)



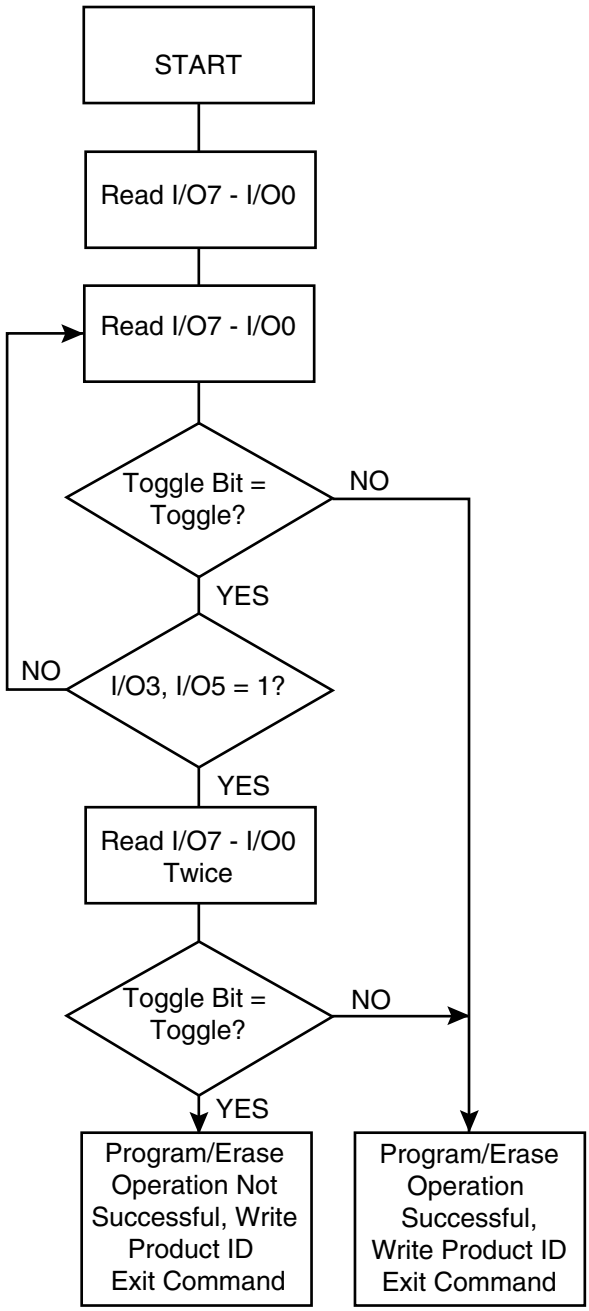

Note: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

**Figure 3.** Toggle Bit Algorithm (Configuration Register = 00)




Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

**Figure 4.** Toggle Bit Algorithm (Configuration Register = 01)




Note: 1. The system should recheck the toggle bit even if I/O5 = “1” because the toggle bit may stop toggling as I/O5 changes to “1”.

## Status Bit Table

| | Status Bit | | | | | | |
|---|---|---|---|---|---|---|---|
| | **I/O7** | **I/O7** | **I/O6** | **I/O5**[1] | **I/O3**[2] | **I/O2** | **RDY/$\overline{\text{BUSY}}$** |
| **Configuration Register:** | **00** | **01** | **00/01** | **00/01** | **00/01** | **00/01** | **00/01** |
| Programming | $\overline{\text{I/O7}}$ | 0 | TOGGLE | 0 | 0 | 1 | 0 |
| Erasing | 0 | 0 | TOGGLE | 0 | 0 | TOGGLE | 0 |
| Erase Suspended & Read Erasing Sector | 1 | 1 | 1 | 0 | 0 | TOGGLE | 1 |
| Erase Suspended & Read Non-erasing Sector | DATA | DATA | DATA | DATA | DATA | DATA | 1 |
| Erase Suspended & Program Non-erasing Sector | $\overline{\text{I/O7}}$ | 0 | TOGGLE | 0 | 0 | TOGGLE | 0 |

Notes: 1. I/O5 switches to a “1” when a program or an erase operation has exceeded the maximum time limits or when a program or sector erase operation is performed on a protected sector.
2. I/O3 switches to a “1” when the $V_{PP}$ level is not high enough to successfully perform program and erase operations.

## Command Definition in Hex[1]

| Command Sequence | Bus Cycles | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read | 1 | Addr | $D_{OUT}$ | | | | | | | | | | |
| Chip Erase | 6 | 555 | AA | AAA[2] | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | 10 |
| Sector Erase | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | SA[3][4] | 30 |
| Byte/Word Program | 4 | 555 | AA | AAA | 55 | 555 | A0 | Addr | $D_{IN}$ | | | | |
| Enter Single Pulse Program Mode | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | A0 |
| Single Pulse Byte/Word Program | 1 | Addr | $D_{IN}$ | | | | | | | | | | |
| Sector Lockdown | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | SA[3][4] | 60 |
| Erase/Program Suspend | 1 | XXX | B0 | | | | | | | | | | |
| Erase/Program Resume | 1 | XXX | 30 | | | | | | | | | | |
| Product ID Entry | 3 | 555 | AA | AAA | 55 | 555 | 90 | | | | | | |
| Product ID Exit[5] | 3 | 555 | AA | AAA | 55 | 555 | F0 | | | | | | |
| Product ID Exit[5] | 1 | XXX | F0 | | | | | | | | | | |
| Program Protection Register | 4 | 555 | AA | AAA | 55 | 555 | C0 | Addr | $D_{IN}$ | | | | |
| Lock Protection Register - Block B | 4 | 555 | AA | AAA | 55 | 555 | C0 | 080 | X0 | | | | |
| Status of Block B Protection | 4 | 555 | AA | AAA | 55 | 555 | 90 | 80 | $D_{OUT}$[6] | | | | |
| Set Configuration Register | 4 | 555 | AA | AAA | 55 | 555 | D0 | XXX | 00/01[7] | | | | |

Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). In word operation I/O15 - I/O8 are Don't Care. The ADDRESS FORMAT shown for each bus cycle is as follows: A11 - A0 (Hex). Address A18 through A11 are Don't Care in the word mode. Address A18 through A11 and A-1 are Don't Care in the byte mode.
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. SA = sector address. Any byte/word address within a sector can be used to designate the sector address (see pages 14 and 15 for details).
4. Once a sector is in the lockdown mode, data in the protected sector cannot be changed unless the chip is reset or power cycled.
5. Either one of the Product ID Exit commands can be used.
6. If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
7. The default state (after power-up) of the configuration register is "00".

## Absolute Maximum Ratings*

Temperature under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground .....-0.6V to +6.25V

All Output Voltages
with Respect to Ground .....-0.6V to $V_{CC}$ + 0.6V

Voltage on $\overline{OE}$ and $V_{PP}$
with Respect to Ground .....-0.6V to +13.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Protection Register Addressing Table

| Word | Use | Block | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | Factory | A | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 5 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 6 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 7 | User | B | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Note: 1. All address lines not specified in the above table must be “0” when accessing the protection register, i.e., A19 - A8 = 0.

## AT49BV/LV801 – Sector Address Table

| Sector | Size (Bytes/Words) | x8<br>Address Range (A18 - A-1) | x16<br>Address Range (A18 - A0) |
|---|---|---|---|
| SA0 | 8K/4K | 000000 - 001FFF | 00000 - 00FFF |
| SA1 | 8K/4K | 002000 - 003FFF | 01000 - 01FFF |
| SA2 | 8K/4K | 004000 - 005FFF | 02000 - 02FFF |
| SA3 | 8K/4K | 006000 - 007FFF | 03000 - 03FFF |
| SA4 | 8K/4K | 008000 - 009FFF | 04000 - 04FFF |
| SA5 | 8K/4K | 00A000 - 00BFFF | 05000 - 05FFF |
| SA6 | 8K/4K | 00C000 - 00DFFF | 06000 - 06FFF |
| SA7 | 8K/4K | 00E000 - 00FFFF | 07000 - 07FFF |
| SA8 | 64K/32K | 010000 - 01FFFF | 08000 - 0FFFF |
| SA9 | 64K/32K | 020000 - 02FFFF | 10000 - 17FFF |
| SA10 | 64K/32K | 030000 - 03FFFF | 18000 - 1FFFF |
| SA11 | 64K/32K | 040000 - 04FFFF | 20000 - 27FFF |
| SA12 | 64K/32K | 050000 - 05FFFF | 28000 - 2FFFF |
| SA13 | 64K/32K | 060000 - 06FFFF | 30000 - 37FFF |
| SA14 | 64K/32K | 070000 - 07FFFF | 38000 - 3FFFF |
| SA15 | 64K/32K | 080000 - 08FFFF | 40000 - 47FFF |
| SA16 | 64K/32K | 090000 - 09FFFF | 48000 - 4FFFF |
| SA17 | 64K/32K | 0A0000 - 0AFFFF | 50000 - 57FFF |
| SA18 | 64K/32K | 0B0000 - 0BFFFF | 58000 - 5FFFF |
| SA19 | 64K/32K | 0C0000 - 0CFFFF | 60000 - 67FFF |
| SA20 | 64K/32K | 0D0000 - 0DFFFF | 68000 - 6FFFF |
| SA21 | 64K/32K | 0E0000 - 0EFFFF | 70000 - 77FFF |
| SA22 | 64K/32K | 0F0000 - 0FFFFF | 78000 - 7FFFF |

## AT49BV/LV801T – Sector Address Table

| Sector | Size (Bytes/Words) | x8<br>Address Range (A18 - A-1) | x16<br>Address Range (A18 - A0) |
|---|---|---|---|
| SA0 | 64K/32K | 000000 - 00FFFF | 00000 - 07FFF |
| SA1 | 64K/32K | 010000 - 01FFFF | 08000 - 0FFFF |
| SA2 | 64K/32K | 020000 - 02FFFF | 10000 - 17FFF |
| SA3 | 64K/32K | 030000 - 03FFFF | 18000 - 1FFFF |
| SA4 | 64K/32K | 040000 - 04FFFF | 20000 - 27FFF |
| SA5 | 64K/32K | 050000 - 05FFFF | 28000 - 2FFFF |
| SA6 | 64K/32K | 060000 - 06FFFF | 30000 - 37FFF |
| SA7 | 64K/32K | 070000 - 07FFFF | 38000 - 3FFFF |
| SA8 | 64K/32K | 080000 - 08FFFF | 40000 - 47FFF |
| SA9 | 64K/32K | 090000 - 09FFFF | 48000 - 4FFFF |
| SA10 | 64K/32K | 0A0000 - 0AFFFF | 50000 - 57FFF |
| SA11 | 64K/32K | 0B0000 - 0BFFFF | 58000 - 5FFFF |
| SA12 | 64K/32K | 0C0000 - 0CFFFF | 60000 - 67FFF |
| SA13 | 64K/32K | 0D0000 - 0DFFFF | 68000 - 6FFFF |
| SA14 | 64K/32K | 0E0000 - 0EFFFF | 70000 - 77FFF |
| SA15 | 8K/4K | 0F0000 - 0F1FFF | 18000 - 18FFF |
| SA16 | 8K/4K | 0F2000 - 0F3FFF | 79000 - 79FFF |
| SA17 | 8K/4K | 0F4000 - 0F5FFF | 7A000 - 7AFFF |
| SA18 | 8K/4K | 0F6000 - 0F7FFF | 7B000 - 7BFFF |
| SA19 | 8K/4K | 0F8000 - 0F9FFF | 7C000 - 7CFFF |
| SA20 | 8K/4K | 0FA000 - 0FBFFF | 7D000 - 7DFFF |
| SA21 | 8K/4K | 0FC000 - 0FDFFF | 7E000 - 7EFFF |
| SA22 | 8K/4K | 0FE000 - 0FFFFF | 7F000 - 7FFFF |

## DC and AC Operating Range

| | | AT49BV/LV801(T)-70 | AT49BV/LV801(T)-90 |
|---|---|---|---|
| Operating Temperature (Case) | Ind. | -40°C - 85°C | -40°C - 85°C |
| $V_{CC}$ Power Supply | | 2.65V to 3.3V/3.0V to 3.6V | 2.65V to 3.3V/3.0V to 3.6V |

## Operating Modes

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{RESET}$ | $V_{PP}$ | Ai | I/O |
|---|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | Ai | $D_{OUT}$ |
| Program/Erase[2] | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IHPP}$[6] | Ai | $D_{IN}$ |
| Standby/Program Inhibit | $V_{IH}$ | X[1] | X | $V_{IH}$ | X | X | High-Z |
| Program Inhibit | X | X | $V_{IH}$ | $V_{IH}$ | X | | |
| | X | $V_{IL}$ | X | $V_{IH}$ | X | | |
| | X | X | X | $V_{IH}$ | $V_{ILPP}$[7] | | |
| Output Disable | X | $V_{IH}$ | X | $V_{IH}$ | X | | High-Z |
| Reset | X | X | X | $V_{IL}$ | X | X | High-Z |
| Product Identification | | | | | | | |
| Hardware | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | | A1 - A19 = $V_{IL}$, A9 = $V_H$[3], A0 = $V_{IL}$ | Manufacturer Code[4] |
| | | | | | | A1 - A19 = $V_{IL}$, A9 = $V_H$[3], A0 = $V_{IH}$ | Device Code[4] |
| Software[5] | | | | $V_{IH}$ | | A0 = $V_{IL}$, A1 - A19 = $V_{IL}$ | Manufacturer Code[4] |
| | | | | | | A0 = $V_{IH}$, A1 - A19 = $V_{IL}$ | Device Code[4] |

Notes:
1. X can be $V_{IL}$ or $V_{IH}$.
2. Refer to AC programming waveforms on page 22.
3. $V_H$ = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH (x8); 001FH (x16), Device Code: C7H (x8)-AT49BV/LV801; 00C7H (x16)-AT49BV/LV801; C6H (x8)-AT49BV/LV801T; 00C6H (x16)-AT49BV/LV801T.
5. See details under “Software Product Identification Entry/Exit” on page 23.
6. $V_{IHPP}$ (min) = 1.65V; $V_{IHPP}$ (max) = 3.6V. For faster erase/program operations, $V_{PP}$ can be set to 5.0V ± 0.5V or 12V ± 0.5V.
7. $V_{ILPP}$ (max) = 0.8V.

## DC Characteristics

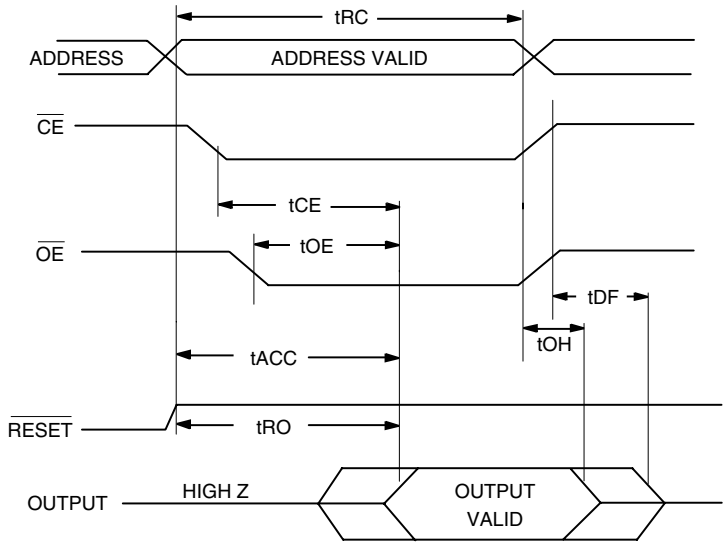
| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to $V_{CC}$ | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{I/O}$ = 0V to $V_{CC}$ | | 10 | µA |
| $I_{SB1}$ | $V_{CC}$ Standby Current CMOS | $\overline{CE}$ = $V_{CC}$ - 0.3V to $V_{CC}$ | | 10 | µA |
| $I_{SB2}$ | $V_{CC}$ Standby Current TTL | $\overline{CE}$ = 2.0V to $V_{CC}$ | | 1 | mA |
| $I_{SB3}$ | $V_{CC}$ Standby Current TTL | $\overline{CE}$ = 2.0V to $V_{CC}$, $V_{CC}$ = 2.85V | | 10 | µA |
| $I_{CC}$ [1][2] | $V_{CC}$ Active Read Current | f = 5 MHz; $I_{OUT}$ = 0 mA, 3.3V≤ $V_{CC}$ | | 30 | mA |
| $I_{CC1}$ | $V_{CC}$ Programming Current ($V_{PP}$ = $V_{CC}$) | | | 45 | mA |
| $I_{PP1}$ | $V_{PP}$ Input Load Current | $V_{PP}$ = 0V, $V_{CC}$ = 3.0V | | 10 | µA |
| | | $V_{PP}$ = $V_{CC}$ = 3.0V | | 10 | µA |
| $I_{CC2}$ | $V_{CC}$ Programming Current ($V_{PP}$ = 5.0V ± 0.5V) | | | 40 | mA |
| $I_{PP2}$ | $V_{PP}$ Programming Current ($V_{PP}$ = 5.0V ± 0.5V) | | | 5 | mA |
| $I_{CC3}$ | $V_{CC}$ Programming Current ($V_{PP}$ = 12.0V ± 0.5V) | | | 40 | mA |
| $I_{PP3}$ | $V_{PP}$ Programming Current ($V_{PP}$ = 12.0V ± 0.5V) | | | 6 | mA |
| $V_{IL}$ | Input Low Voltage | | | 0.6 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | V |
| $V_{OL1}$ | Output Low Voltage | $I_{OL}$ = 2.1 mA | | 0.45 | V |
| $V_{OL2}$ | Output Low Voltage | $I_{OL}$ = 1.0 mA | | 0.20 | V |
| $V_{OH1}$ | Output High Voltage | $I_{OH}$ = -400 µA | 2.4 | | V |
| $V_{OH2}$ | Output High Voltage | $I_{OH}$ = -100 µA | 2.5 | | V |

Notes: 1. In the erase mode, $I_{CC}$ is 50 mA.
2. For 3.3V < $V_{CC}$ < 3.6V, $I_{CC}$ (max) = 35 mA

## AC Read Characteristics

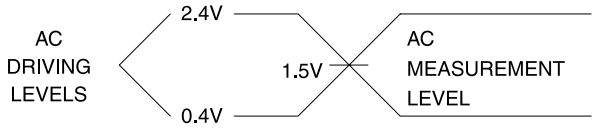
| Symbol | Parameter | AT49BV/LV801(T)-70 | | AT49BV/LV801(T)-90 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | | 70 | | 90 | ns |
| $t_{ACC}$ | Address to Output Delay | | 70 | | 90 | ns |
| $t_{CE}$[1] | $\overline{CE}$ to Output Delay | | 70 | | 90 | ns |
| $t_{OE}$[2] | $\overline{OE}$ to Output Delay | 0 | 35 | 0 | 40 | ns |
| $t_{DF}$[3][4] | $\overline{CE}$ or $\overline{OE}$ to Output Float | 0 | 25 | 0 | 25 | ns |
| $t_{OH}$ | Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first | 0 | | 0 | | ns |
| $t_{RO}$ | $\overline{RESET}$ to Output Delay | | 100 | | 100 | ns |

## AC Read Waveforms[1][2][3][4]

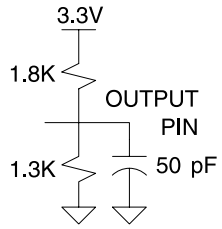



Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on $t_{ACC}$.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{CE}$ or by $t_{ACC} - t_{OE}$ after an address change without impact on $t_{ACC}$.
3. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level




## Output Test Load




## Pin Capacitance

f = 1 MHz, T = 25°C[1]

| Symbol | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 4 | 6 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 8 | 12 | pF | $V_{OUT}$ = 0V |

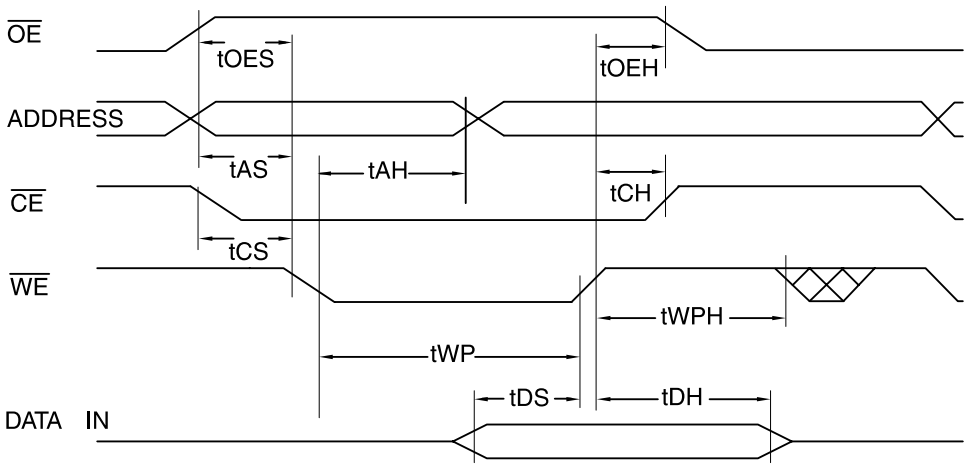
Note: 1. This parameter is characterized and is not 100% tested

## AC Byte/Word Load Characteristics

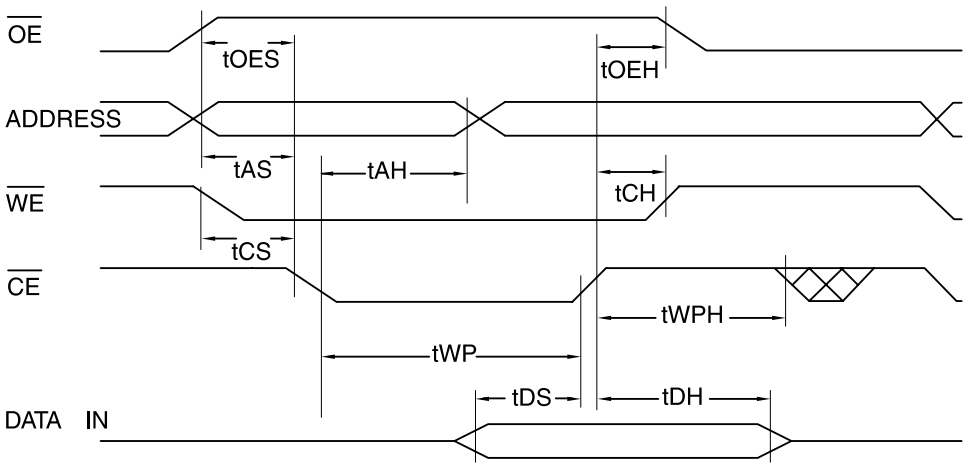
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{AS}$, $t_{OES}$ | Address, $\overline{OE}$ Setup Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 40 | | ns |
| $t_{CS}$ | Chip Select Setup Time | 0 | | ns |
| $t_{CH}$ | Chip Select Hold Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width ($\overline{WE}$ or $\overline{CE}$) | 40 | | ns |
| $t_{DS}$ | Data Setup Time | 30 | | ns |
| $t_{DH}$, $t_{OEH}$ | Data, $\overline{OE}$ Hold Time | 0 | | ns |
| $t_{WPH}$ | Write Pulse Width High | 30 | | ns |

## AC Byte/Word Load Waveforms

### $\overline{WE}$ Controlled



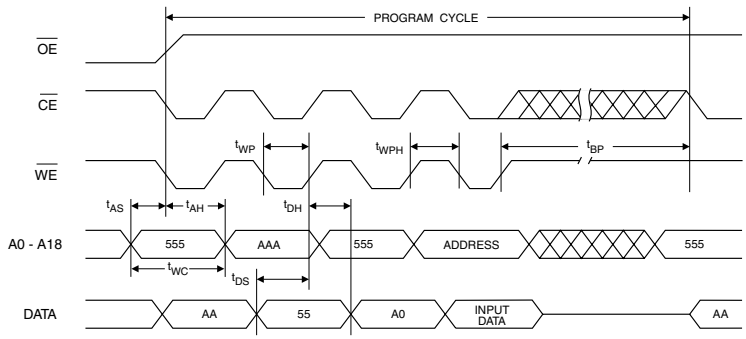

### $\overline{CE}$ Controlled



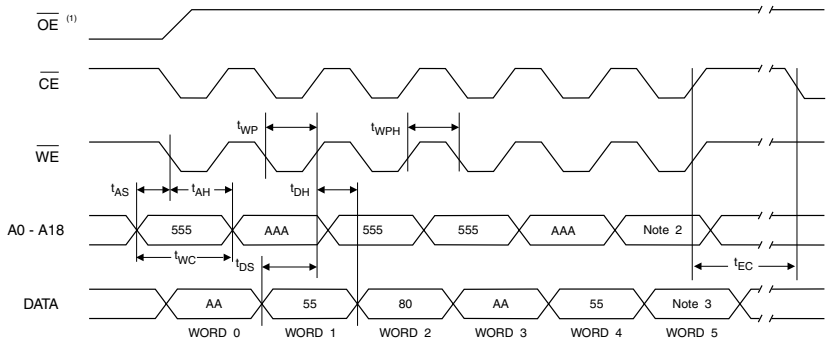
## Program Cycle Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{BP}$ | Byte/Word Programming Time ($V_{IHPP} < V_{PP} < 4.5V$) | | 20 | 200 | µs |
| $t_{BPVPP}$ | Byte/Word Programming Time ($V_{PP} \geq 4.5V$) | | 10 | 100 | µs |
| $t_{AS}$ | Address Setup Time | 0 | | | ns |
| $t_{AH}$ | Address Hold Time | 40 | | | ns |
| $t_{DS}$ | Data Setup Time | 30 | | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | | ns |
| $t_{WP}$ | Write Pulse Width | 40 | | | ns |
| $t_{WPH}$ | Write Pulse Width High | 30 | | | ns |
| $t_{WC}$ | Write Cycle Time | 70 | | | ns |
| $t_{RP}$ | $\overline{\text{Reset}}$ Pulse Width | 500 | | | ns |
| $t_{RH}$ | $\overline{\text{Reset}}$ High Time before Read | 50 | | | ns |
| $t_{EC}$ | Chip Erase Cycle Time ($V_{PP} < 4.5V$) | | | 12 | seconds |
| $t_{ECVPP}$ | Chip Erase Cycle Time ($V_{PP} \geq 4.5V$) | | | 6 | seconds |
| $t_{SEC}$ | Sector Erase Cycle Time | | 300 | 400 | ms |
| $t_{EPS}$ | Erase or Program Suspend Time | | | 15 | µs |

## Program Cycle Waveforms




## Sector or Chip Erase Cycle Waveforms



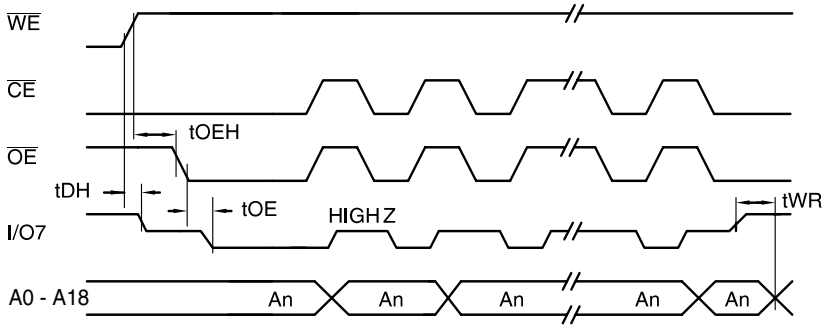

Notes:
1. $\overline{\text{OE}}$ must be high only when $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are both low.
2. For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 3 under Command Definitions.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

## $\overline{\text{Data}}$ Polling Characteristics[1]

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{DH}$ | Data Hold Time | 10 | | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time | 10 | | | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay[2] | | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.
2. See $t_{OE}$ spec in "AC Read Characteristics" on page 18.

## $\overline{\text{Data}}$ Polling Waveforms

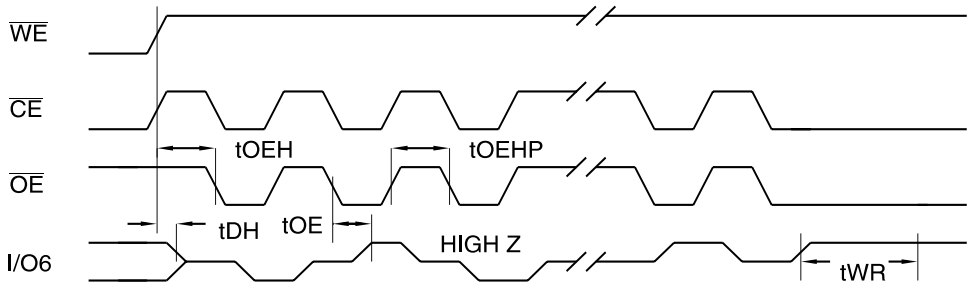



## Toggle Bit Characteristics[1]

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{DH}$ | Data Hold Time | 10 | | | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time | 10 | | | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Delay[2] | | | | ns |
| $t_{OEHP}$ | $\overline{OE}$ High Pulse | 50 | | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | | ns |

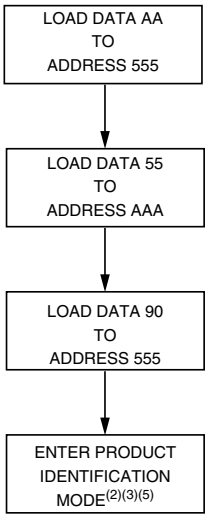
Notes: 1. These parameters are characterized and not 100% tested.
2. See $t_{OE}$ spec in "AC Read Characteristics" on page 18.

## Toggle Bit Waveforms[1][2][3]

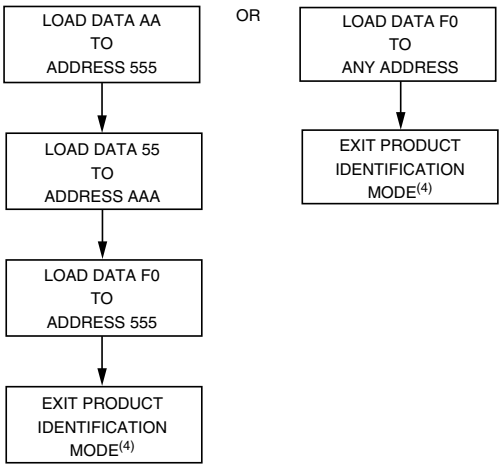



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
The $t_{OEHP}$ specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

## Software Product Identification Entry[1]

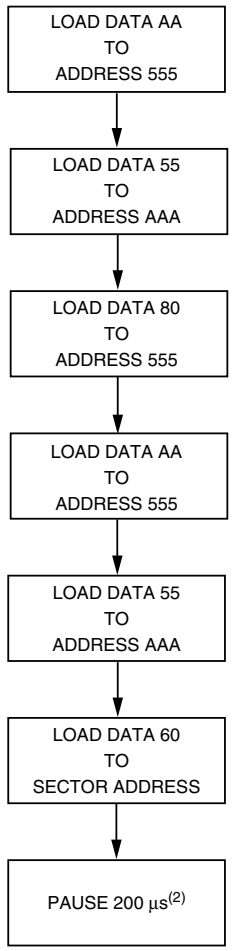



## Software Product Identification Exit[1][6]




Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex), A-1, and A11 - A18 (Don't Care).
2. A1 - A18 = $V_{IL}$. Manufacturer Code is read for A0 = $V_{IL}$; Device Code is read for A0 = $V_{IH}$.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH(x8); 001FH(x16)
   Device Code: C7H (x8) - AT49BV/LV801;
   00C7H (x16) - AT49BV/LV801;
   C6H (x8) - AT49BV/LV801T;
   00C6H (x16) - AT49BV/LV801T.
6. Either one of the Product ID Exit commands can be used.

## Sector Lockdown Enable Algorithm[1]




Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex), A-1, and A11 - A18 (Don't Care).
2. Sector Lockdown feature enabled.

## AT49BV801(T) Ordering Information

| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 70 | 25 | 0.01 | AT49BV801-70CI<br>AT49BV801-70TI | 48C5<br>48T | Industrial<br>(-40° to 85°C) |
| 90 | 25 | 0.01 | AT49BV801-90CI<br>AT49BV801-90TI | 48C5<br>48T | Industrial<br>(-40° to 85°C) |
| 70 | 25 | 0.01 | AT49BV801T-70CI<br>AT49BV801T-70TI | 48C5<br>48T | Industrial<br>(-40° to 85°C) |
| 90 | 25 | 0.01 | AT49BV801T-90CI<br>AT49BV801T-90TI | 48C5<br>48T | Industrial<br>(-40° to 85°C) |

## AT49LV801(T) Ordering Information

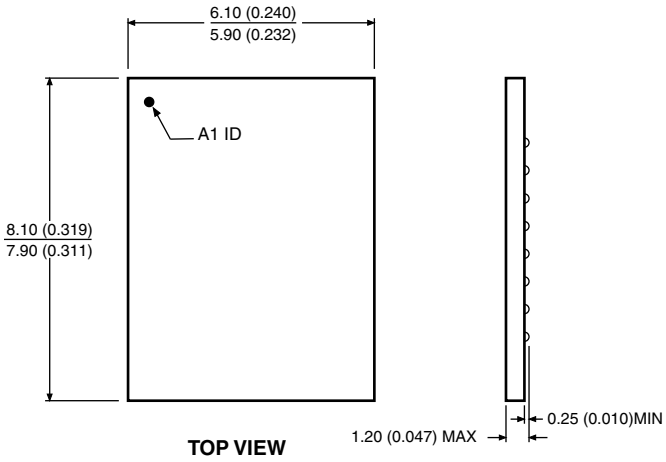
| $t_{ACC}$ (ns) | $I_{CC}$ (mA) | | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| | Active | Standby | | | |
| 70 | 25 | 0.01 | AT49LV801-70CI<br>AT49LV801-70TI | 48C5<br>48T | Industrial<br>(-40° to 85°C) |
| 70 | 25 | 0.01 | AT49LV801T-70CI<br>AT49LV801T-70TI | 48C5<br>48T | Industrial<br>(-40° to 85°C) |

| Package Type | |
|---|---|
| **48C5** | 48-ball, Plastic Chip-size Ball Grid Array Package (CBGA) |
| **48T** | 48-lead, Plastic Thin Small Outline Package (TSOP) |

# Packaging Information

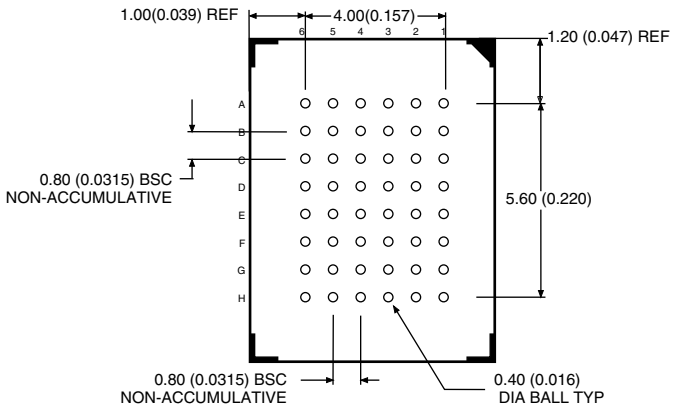
## 48C5 – CBGA

Dimensions in Millimeters and (Inches).
Controlling dimension: millimeters.




**TOP VIEW**

**SIDE VIEW**

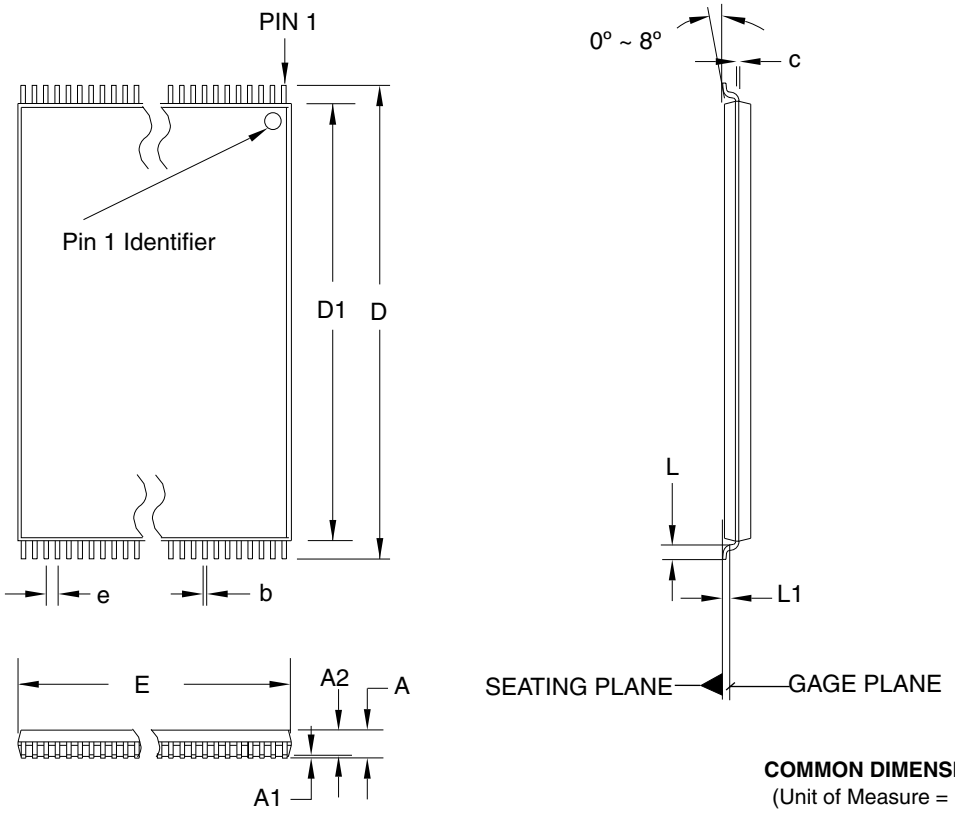



**BOTTOM VIEW**

10/18/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **48C5**, 48-ball (6 x 8 Array), 0.80 mm Pitch, 6 x 8 x 1.2 mm<br>Chip-scale Ball Grid Array Package (CBGA) | 48C5 | A |

## 48T – TSOP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 19.80 | 20.00 | 20.20 | |
| D1 | 18.30 | 18.40 | 18.50 | Note 2 |
| E | 11.90 | 12.00 | 12.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **48T**, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP) | 48T | B |

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