PAM8012

Mono 2.0W Anti-saturation Class D Audio Power Amplifier with Power Limit

Key Features

- 1.0W/2.0W@<1% THD Output with a 8Ω /4Ω Load at 5V Supply
- Maximum Output Power Can Be Set by One External Resistor
- Minimized ON/OFF Pop Noise
- Superior Low Noise
- High PSRR
- Supply Voltage from 2.5V to 5.5 V
- Auto Recovering Short Circuit Protection
- Over Temperature Protection
- 9 Ball, 1.3mm x 1.3mm, 0.4mm Pitch WCSP and eMSOP10 Packages

Applications

- Wireless or Cellular Handsets and PDAs
- Portable Navigation Devices
- General Portable Audio Devices

General Description

The PAM8012 is a 2.0W mono filterless class-D amplifier with high PSRR and differential input that reduce noise.

Features like 90% efficiency and small PCB area make the PAM8012 Class-D amplifier ideal for cellular handsets. The filterless architecture requires no external output filter, fewer external components, less PCB area and lower system costs, and simplifies application design.

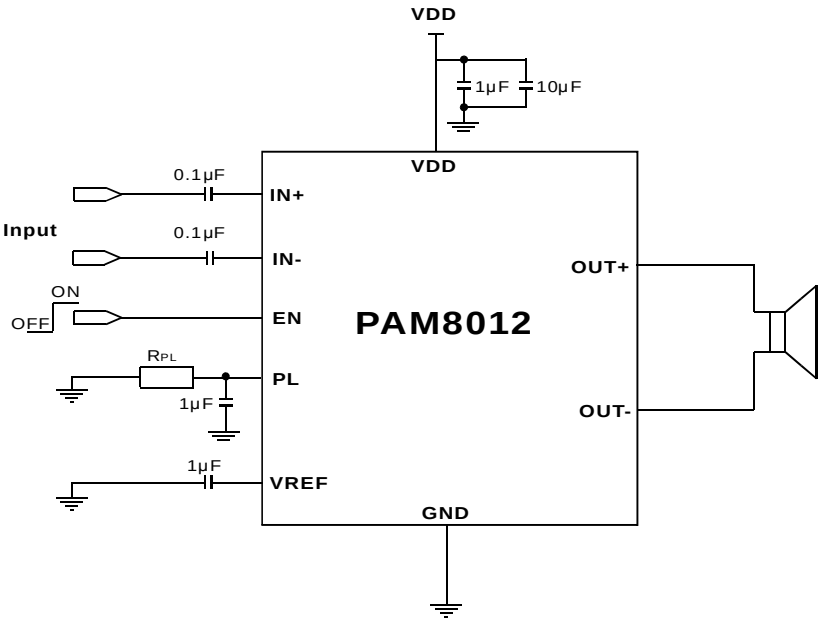
The PAM8012 features anti-saturation function which detect output signal clip due to the over input level and keep the output non-saturation automatically to get the excellent sound quality.

The maximum output power without clip can be set by one resistor at PL pin that to prevent the speaker to be damaged..

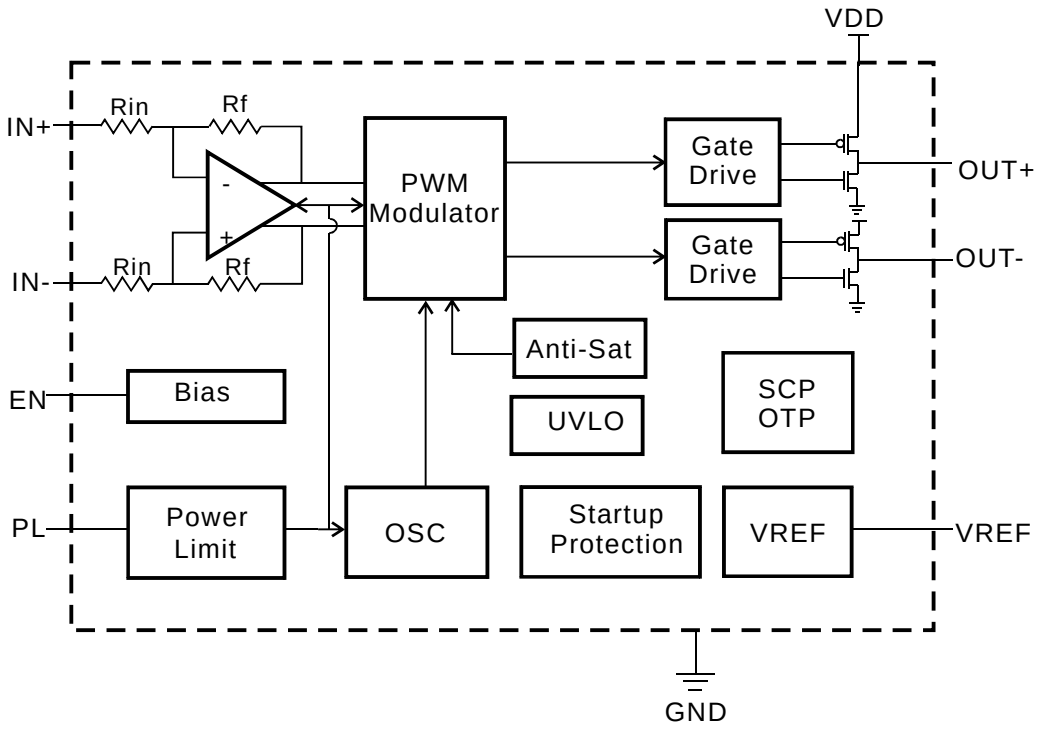
The PAM8012 features short circuit protection and over temperature protection.

The PAM8012 is available in tiny WCSP9 (1.3mm x 1.3mm) and eMSOP10 packages.

Typical Application Circuit

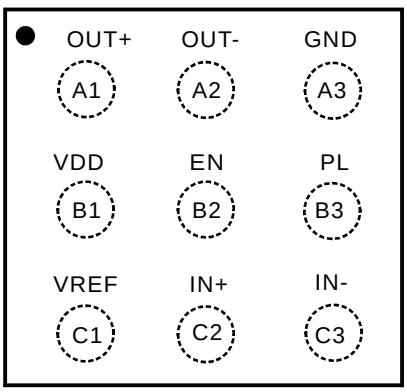


Block Diagram

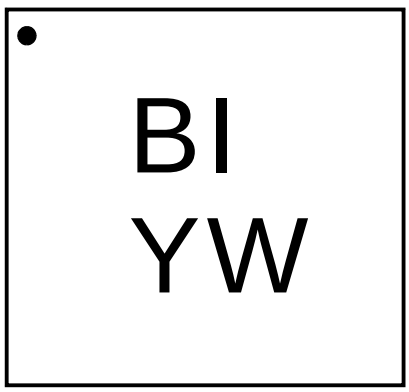


Pin Configuration & Marking Information

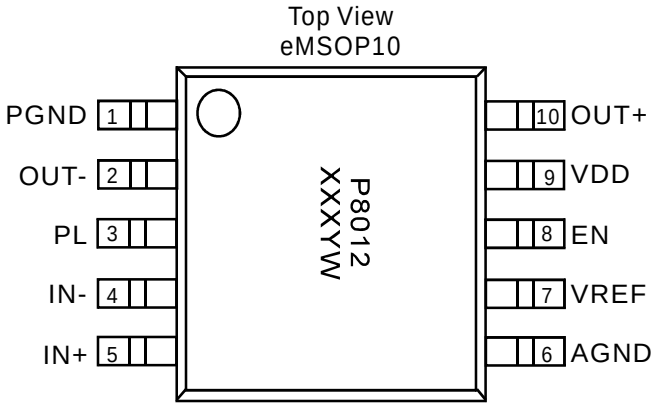
9 Ball 0.4mm pitch WCSP
Top View of PCB



9 Ball 0.4mm pitch WCSP
Top View of Marking



BI: Product Code of PAM8012
Y: Year
W: Week



X: Internal Code
Y: Year
W: Week

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage, VDD.....6.0V
Input Voltage,IN+,IN-.....-0.3V to VDD+0.3V
Minimum load resistance, R_L.....3.2Ω
Storage Temperature.....-65°C to 150°C
Maximum Junction Temperature.....150°C
Soldering Temperature.....260°C,10 sec

Recommended Operating Conditions

Supply voltage Range.....2.5V to 5.5V
Ambient Temperature Range.....-40°C to 85°C
Junction Temperature Range.....-40°C to 125°C

Thermal Information

Parameter	Symbol	Package	Maximum	Unit
Thermal Resistance (Junction to ambient)	θ_{JA}	WCSP9 1.3x1.3	100	°C/W
		eMSOP10	60	
Thermal Resistance (Junction to case)	θ_{JC}	WCSP9 1.3x1.3	40	°C/W
		eMSOP10	30	

Electrical Characteristic

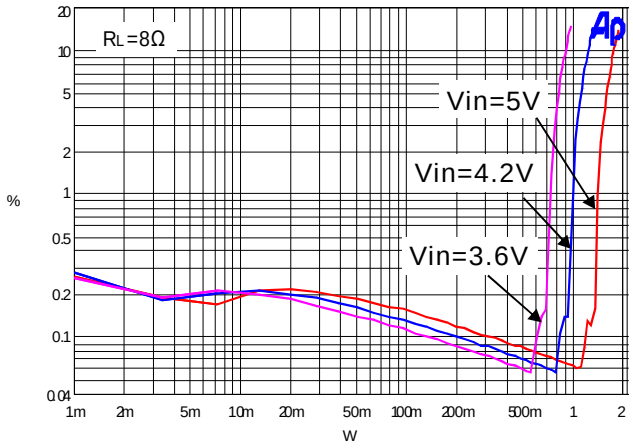
T_A=25°C, VDD=5.0V, R_L=8Ω, unless otherwise noted.

Symbol	Parameter	Test Conditions		MIM	TYP	MAX	UNIT
VDD	Supply Voltage			2.5		5.5	V
Po	Output Power	RPL=110KΩ,f=1kHz, R=4Ω	VDD=5.0V		2.0		W
		RPL=110KΩ,f=1kHz, R=8Ω	VDD=5.0V		1.0		
THD+N	Total Harmonic Distortion Plus Noise	VDD=5.0V,Po=2.0W,R=4Ω	f=1kHz		0.08		%
		VDD=3.6V,Po=1.0W,R=4Ω			0.08		
		VDD=5.0V,Po=1.0W,R=8Ω	f=1kHz		0.08		%
		VDD=3.6V,Po=0.5W,R=8Ω			0.08		
PSRR	AC Power Supply Ripple Rejection	f=217Hz, Inputs ac-grounded with Cin=0.1μF	VDD=5.0V		-75		dB
			VDD=3.6V		-75		
SNR	Signal to Noise Ratio	THD=1%, f=1KHz	VDD=5.0V		95		
			VDD=3.6V		95		
Vn	Output Noise	Cin=0.1uF, Inputs ac-grounded	No A-weighting		60		μV
			A-weighting		40		
η	Peak Efficiency	R_L=8Ω	f=1kHz		90		%
		R_L=4Ω			87		
IQ	Quiescent Current	VEN=5.0V,VDD=5.0V,PL=0V	No Load		4.2		mA
Isd	Shutdown Current	VDD=2.5V to 5.5V,VEN=0V	No Load			1	uA
|VOS|	Offset Voltage	VDD=5V		-20		20	mV
RIN	Input Resistor	VDD=5V			31		KΩ
GV	Closed Loop Gain	VDD=5V			18		dB
fSW	Switching Frequency	VDD=5V			250		KHz
TON	Turn-on Time	VDD=5V			45		mS
OTP	Over Temperature Protection	VDD=5V	No Load		150		℃
OTH	Over Temperature Hysterisis	VDD=5V	No Load		40		℃
VENH	High-level EN voltage	VDD=5V		1.4			V
VENL	Low-level EN voltage	VDD=5V				0.4	V
AR	Maximum Attenuation Range	Anti-saturation Active,from +18dB to -8dB			26		dB

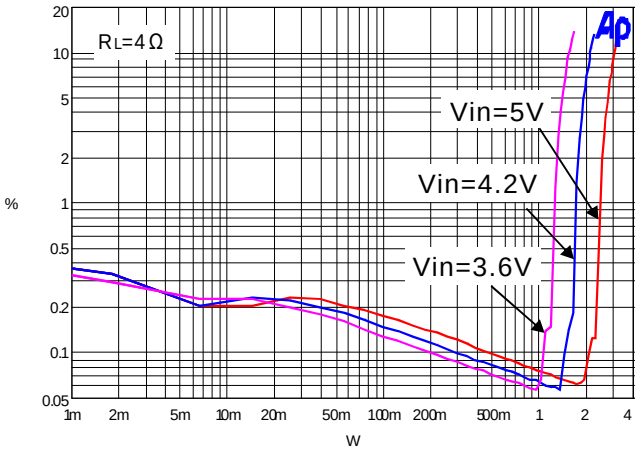
Typical Operating Characteristics

T_A=25°C, V_{DD}=5V, unless otherwise noted.

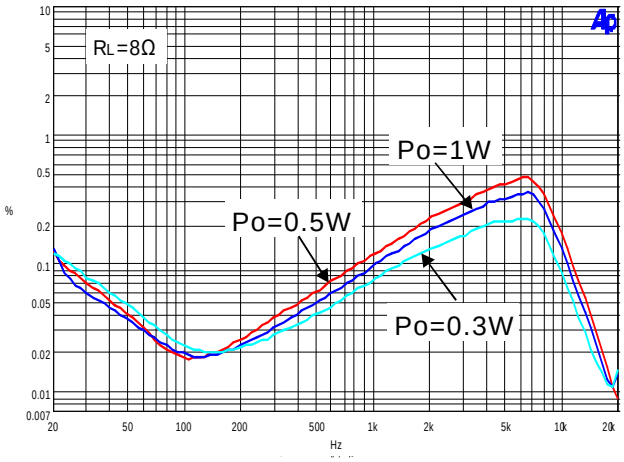
1. THD+N VS Output Power



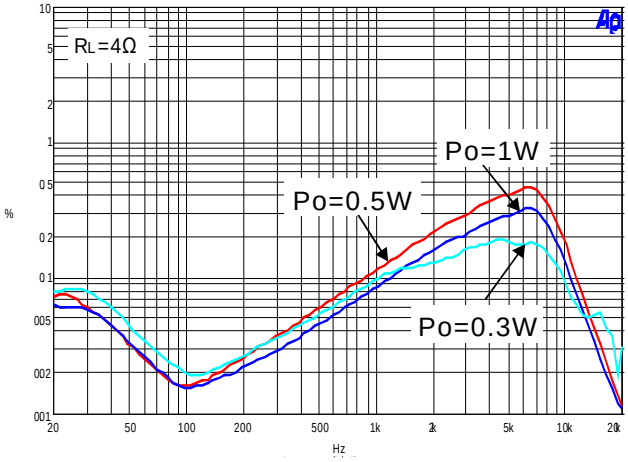
2. THD+N VS Output Power



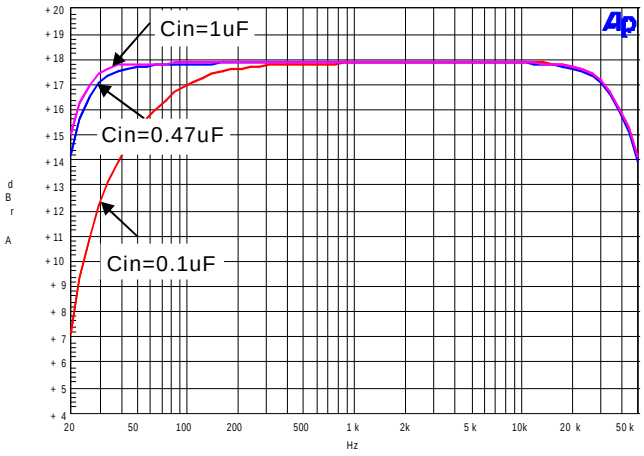
3. THD+N VS Frequency



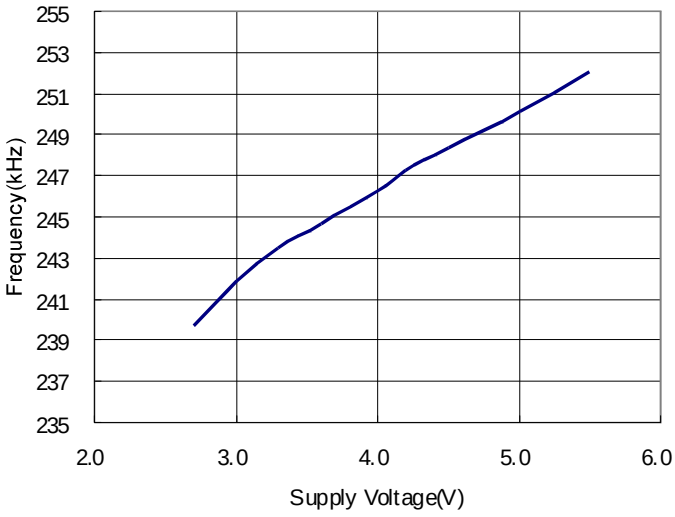
4. THD+N VS Frequency



5. Frequency Response



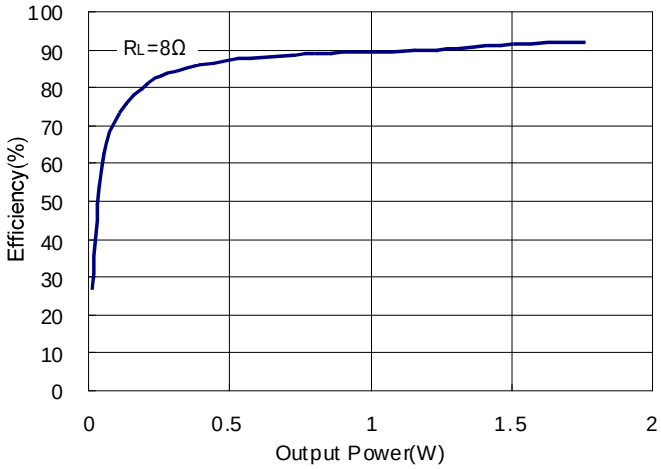
6. Frequency VS Supply Voltage



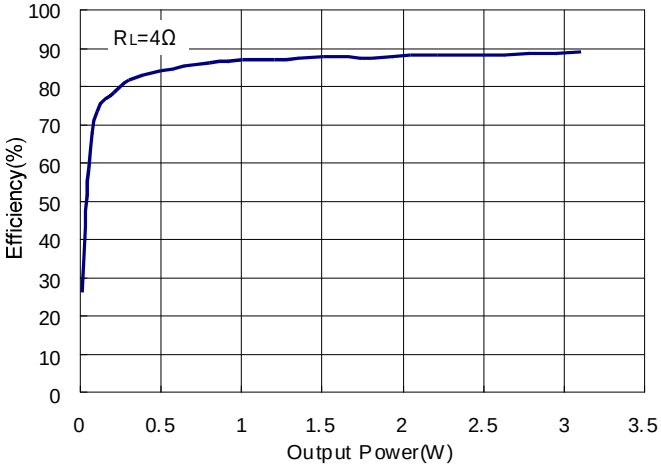
Typical Operating Characteristics

T_A=25°C, V_{DD}=5V, unless otherwise noted.

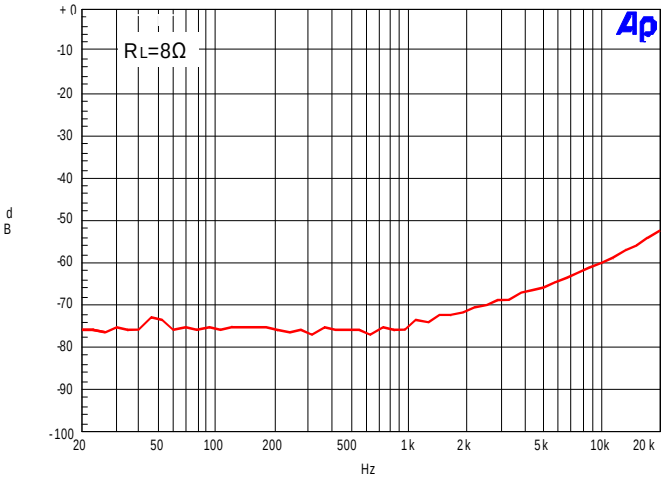
7. Efficiency VS Output Power



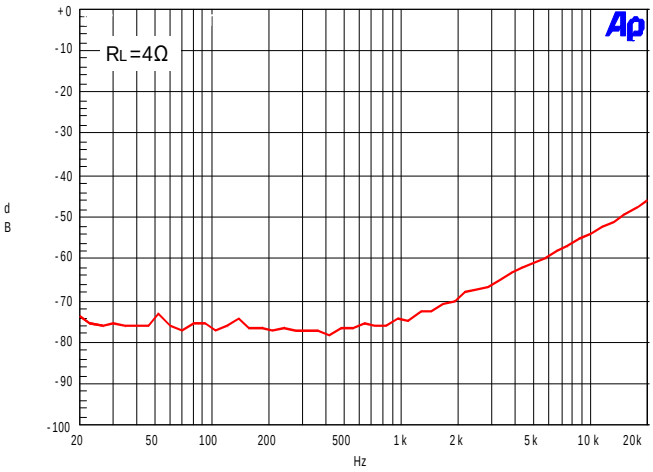
8. Efficiency VS Output Power



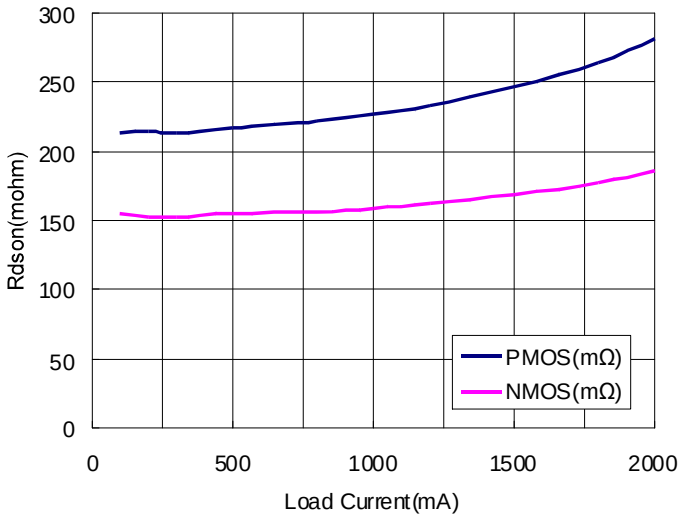
9. PSRR VS Frequency



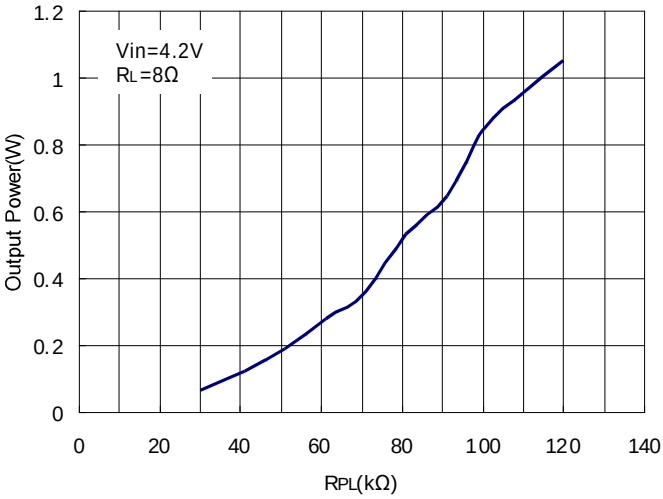
10. PSRR VS Frequency



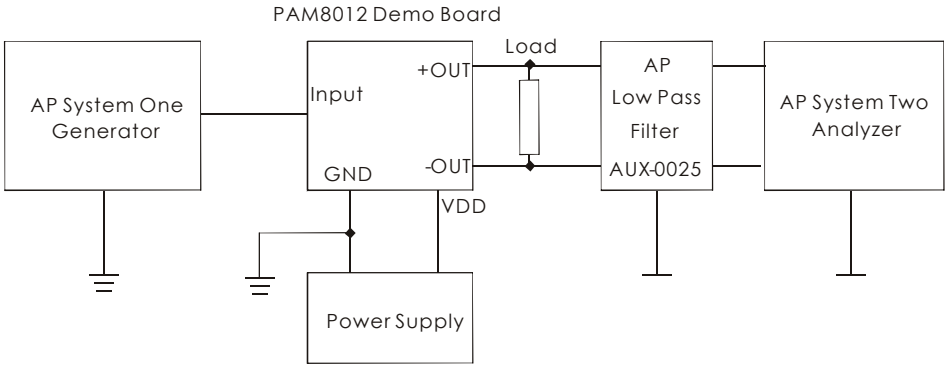
11. Rdson VS Load Current



12. RPL VS Output Power



Test Setup for Performance Testing



Notes

1. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
2. Two 33µH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Application Information

Anti-saturation

The Anti-saturation feature provides continuous automatic gain adjustment to the amplifiier through an internal circuit. This feature enhances the perceived audio loudness and at the same time prevents speaker damage from occurring.

The Anti-saturation works by detecting the output. The gain changes depending on the supply voltage , and the attack and release time. The gain changes constantly as the audio signal increases and/or decreases. The gain step size for the Anti-saturation is 0.4 dB. If the audio signal has near-constant amplitude, the gain does not change. Table 1 shows the Anti-saturation variable description.

Table 1. PAM8012 Anti-saturation Variable Description

VARIABLE	DESCRIPTION	Value
Gain	The pre-set gain of the device when the Anti-saturation is inactive. The fixed gain is also the initial gain when the device comes out of shutdown mode or when the Anti-saturation is disabled	18dB (Maximum)
Attack Time	The minimum time between two gain decrements.	128uS
Release Time	The minimum time between two gain increments.	256mS

PL Terminal Function

The voltage value of PL sets the PAM8012 maximum output by an external resistor. Refer to table 2 for anti-saturation and power limit selection.

Table 2. PAM8012 Anti-saturation and Power Limit Variable Description

		Rpl		
		0	30K<Rpl<120K	Open
EN	VDD	PL: OFF Anti-sat: OFF	PL: ON Anti-sat: ON	PL: OFF Anti-sat: ON
	VDD/2	PL: OFF Anti-sat: OFF	PL: ON Anti-sat: OFF	PL: ON Anti-sat: OFF

Application Information

Input Capacitors (Ci)

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form is a high-pass filter with the corner frequency determined in the follow equation:

$$fc = \frac{1}{2\pi RiCi}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example,the specification calls for a flat bass response are down to 150Hz. Equation is reconfigured as followed:

$$Ci = \frac{1}{2\pi Rifc}$$

When input resistance variation is considered, the Ci is 34nF, so one would likely choose a value of 33nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at $V_{DD}/2$, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_s)

The PAM8012 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, is placed as close as possible to VDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure 1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

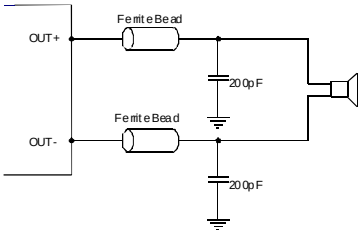


Figure 1: Ferrite Bead Filter to Reduce EMI

Shutdown operation

In order to reduce power consumption while not in use, the PAM8012 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the EN pin. By switching the EN pin connected to GND, the PAM8012 supply current draw will be minimized in idle mode.

Short Circuit Protection (SCP)

The PAM8012 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorts or output-to-GND shorts occur. When a short circuit occurs, the device immediately goes into shutdown state. Once the short is removed, the device will be reactivated.

Over Temperature Protection (OTP)

Thermal protection on the PAM8012 prevents the device from damage when the internal die temperature exceeds 150°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 40°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

POP and Click Circuitry

The PAM8012 contains circuitry to minimize turn-on and turn-off transients or “click and pops”, where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage, 1/2 VDD. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

PCB Layout Guidelines

Grounding

It is recommended to use plane grounding. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. When these currents circulate elsewhere, they may get into the power supply, or the signal ground, etc, even worse, they may form a loop and radiate noise. Any of these instances results in degraded amplifier performance. The output noise ground that the logical returns for the output noise currents associated with class D switching must tie to system ground at the power exclusively. Signal currents for the inputs, reference need to be returned to quite ground. This ground only ties to the signal components and the GND pin. GND then ties to system ground.

Power Supply Line

It is recommended that all the trace could be routed as short and thick as possible. For the power line layout, just imagine water stream, any barricade placed in the trace (shown in figure 2) could result in the bad performance of the amplifier.

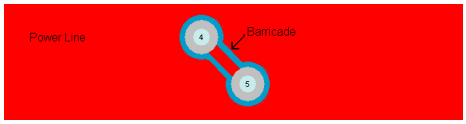


Figure 2: Power Line

Components Placement

Decoupling capacitors as previously described, the high-frequency 1μF decoupling capacitors should be placed as close to the power supply terminals VDD as possible. Large bulk power supply decoupling capacitors (10μF or greater) should be placed near the PAM8012 on the VDD terminal.

Input resistors and capacitors need to be placed very close to input pins.

Output filter - The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance, and the capacitors used in the filters should be grounded to system ground.

Ordering Information

PAM8012 X X X

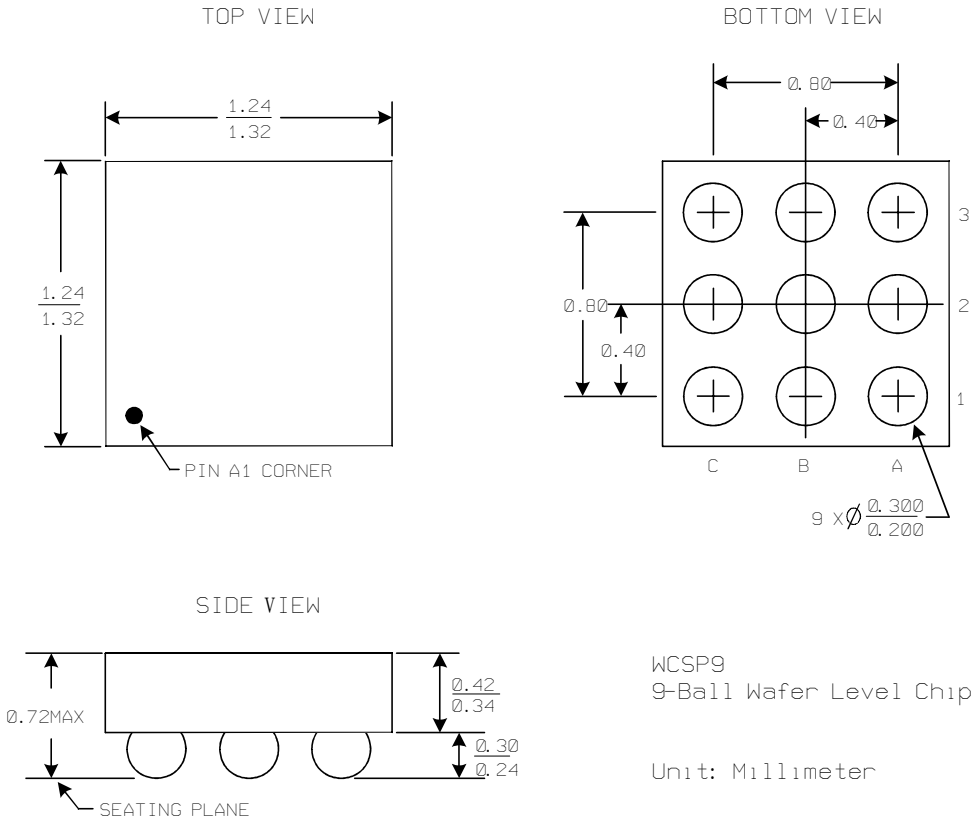
- Number of pins
- Package Type
- Pin Configuration

Pin Configuration		Package Type	Number of pins
A:	B:	Z: WCSP9	N: 9
A1: OUT+	1. PGND	S: eMSOP10	M: 10
A2: OUT-	2. OUT-		
A3: GND	3. PL		
B1: VDD	4. IN-		
B2: EN	5. IN+		
B3: PL	6. AGND		
C1: VREF	7. VREF		
C2: IN+	8. EN		
C3: IN-	9. VDD		
	10.OUT+		

Part Number	Marking	Package Type	MOQ
PAM8012AZN	BI YW	WCSP9(1.3mm x 1.3mm)	3,000 Units/ Tape & Reel
PAM8012BSM	P8012 XXXYW	eMSOP10	2,500 Units/ Tape & Reel

Outline Dimensions

WCSP9

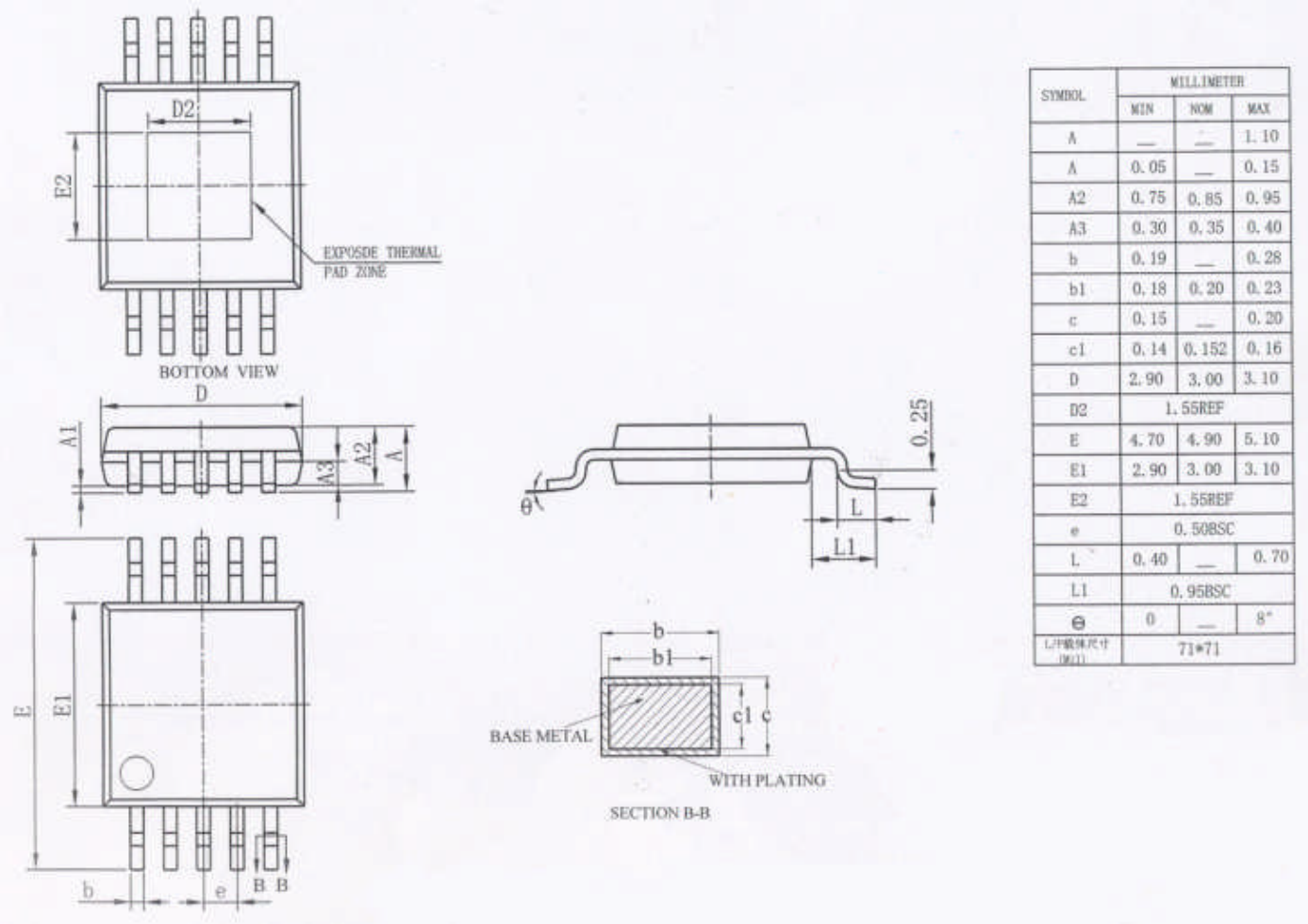


WCSP9
9-Ball Wafer Level Chip Scale Package

Unit: Millimeter

Outline Dimensions

eMSOP10



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.19	—	0.28
b1	0.18	0.20	0.23
c	0.15	—	0.20
c1	0.14	0.152	0.16
D	2.90	3.00	3.10
D2	1.55REF		
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
E2	1.55REF		
e	0.50BSC		
L	0.40	—	0.70
L1	0.95BSC		
θ	0	—	8°
模具尺寸	71*71		

Datasheet Revision History

Date	Revision	Description	Comment
03/10/2011	Advanced	Initially Version.	
08/30/2011	Preliminary	Add silicon test data.	
09/19/2011	Rev1.0	Initially released.	
02/06/2012	Rev1.1	Add eMSOP10 package and update the "RPL vs Po" curve.	
05/23/2012	Rev1.2	Update the "Pin Configuration" of eMSOP10 package and thermal info; Add "Datasheet Revision History" form.	
06/06/2012	Rev1.3	Update "Table 2" in "Application Information"	