



# FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

**IDT54/74FCT299T/AT/CT**

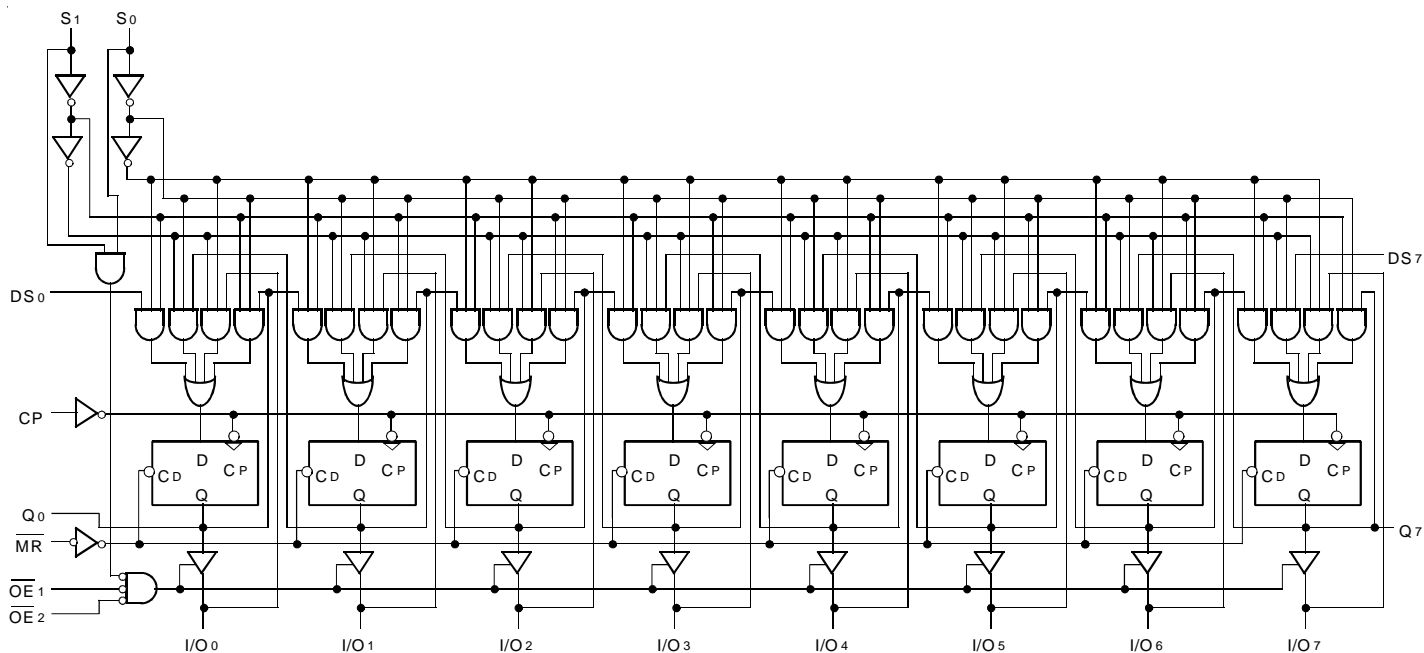
## FEATURES:

- Std., A, and C grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - $V_{OH} = 3.3V$  (typ.)
  - $V_{OL} = 0.3V$  (typ.)
- High Drive outputs (-15mA  $I_{OH}$ , 48mA  $I_{OL}$ )
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Power off disable outputs permit "live insertion"
- Available in the following packages:
  - Industrial: SOIC, QSOP
  - Military: CERDIP, LCC

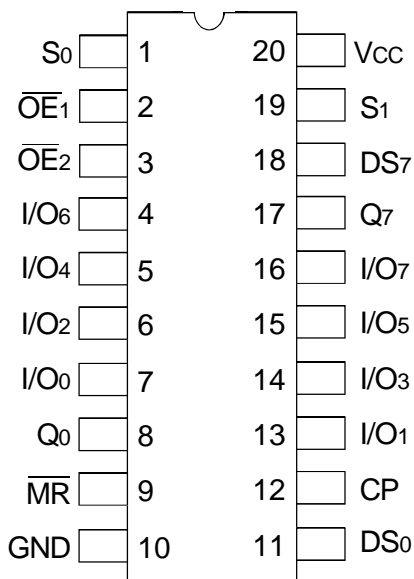
## DESCRIPTION:

The FCT299T is built using an advanced dual metal CMOS technology. The FCT299T is an 8-input universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q<sub>0</sub> and Q<sub>7</sub> to allow easy serial cascading. A separate active low Master Reset is used to reset the register.

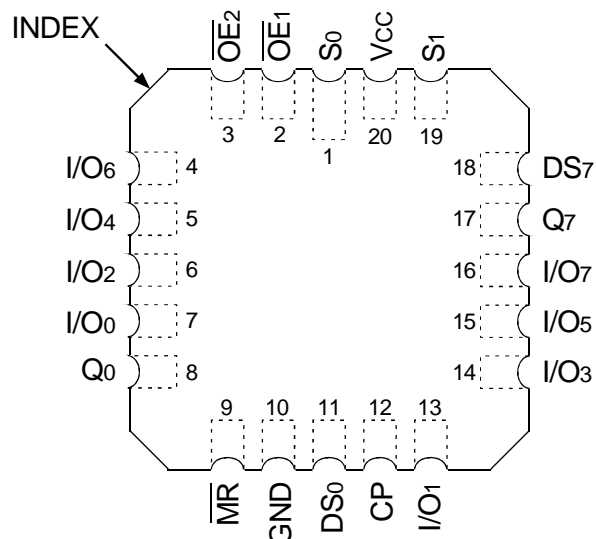
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



CERDIP/ SOIC/ QSOP  
TOP VIEW



LCC  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Output and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS <sub>0</sub>	Serial Data Input for Right Shift
DS <sub>7</sub>	Serial Data Input for Left Shift
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$ , $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O <sub>0</sub> -I/O <sub>7</sub>	Parallel Data Inputs or 3-State Parallel Outputs
O <sub>0</sub> , O <sub>7</sub>	Serial Outputs

## FUNCTION TABLE<sup>(1)</sup>

Inputs				Response
$\overline{MR}$	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	X	Asynchronous Reset Q <sub>0</sub> -Q <sub>7</sub> = LOW
H	H	H	↑	Parallel Load; I/O <sub>x</sub> → Q <sub>x</sub>
H	L	H	↑	Shift Right; DS <sub>0</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> , etc.
H	H	L	↑	Shift Left; DS <sub>7</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> , etc.
H	L	L	X	Hold

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW-to-HIGH clock transition

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -6\text{mA MIL}$ $I_{OH} = -8\text{mA IND}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL}$ $I_{OH} = -15\text{mA IND}$	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 32\text{mA MIL}$ $I_{OL} = 48\text{mA IND}$	—	0.3	0.5	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$
$V_H$	Input Hysteresis	—		—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	0.01	1	$\mu\text{A}$

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .
5. This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1 = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7 = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2	5.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = \text{GND}$ $\overline{MR} = V_{CC}$ $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7 = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6	16.3 <sup>(5)</sup>	

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.

3. Per TTL driven input; ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of  $\Delta I_{CC}$  formula. These limits are guaranteed but not tested.

6.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL Inputs High

$N_T$  = Number of TTL Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_i$  = Output Frequency

$N_i$  = Number of Outputs at  $f_i$

All currents are in milliamperes and all frequencies are in megahertz.

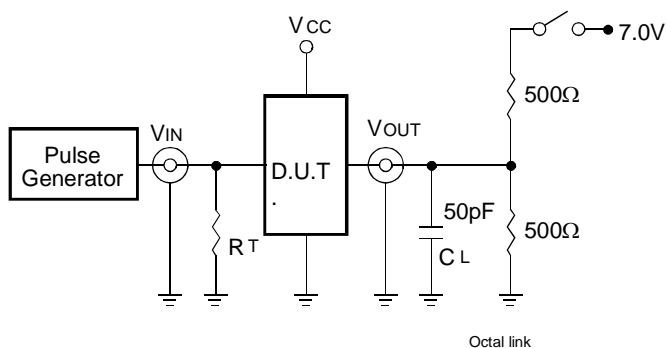
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54FCT299T		IDT54/74FCT299AT		IDT54/74FCT299CT				Unit		
			Mil.		Ind.		Mil.		Ind.			Mil.	
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.		Min. <sup>(2)</sup>	Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>0</sub> or Q <sub>7</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	2	14	2	7.2	2	9.5	2	6.5	2	7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to I/O <sub>x</sub>		2	12	2	7.2	2	9.5	2	6.5	2	7.5	ns
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to Q <sub>0</sub> or Q <sub>7</sub>		2	10.5	2	7.2	2	9.5	2	6.5	2	7.5	ns
t <sub>PHL</sub>	Propagation Delay $\overline{MR}$ to I/O <sub>x</sub>		2	15	2	8.7	2	11.5	2	6.5	2	7.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OE}_x$ to I/O <sub>x</sub>		1.5	15	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OE}_x$ to I/O <sub>x</sub>		1.5	9	1.5	6	1.5	6.5	1.5	6	1.5	6.5	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP		7.5	—	3.5	—	4	—	3.5	—	4	—	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW I/O <sub>n</sub> , DS <sub>0</sub> or DS <sub>7</sub> to CP		5.5	—	4	—	4.5	—	4	—	4.5	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP		1	—	1	—	1	—	1	—	1	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW I/O <sub>x</sub> , DS <sub>0</sub> or DS <sub>7</sub> to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t <sub>w</sub>	CP Pulse Width, HIGH or LOW		7	—	5	—	6	—	5	—	6	—	ns
t <sub>w</sub>	$\overline{MR}$ Pulse Width LOW		7	—	5	—	6	—	5	—	6	—	ns
t <sub>REM</sub>	Recovery Time	7	—	5	—	6	—	5	—	6	—	ns	

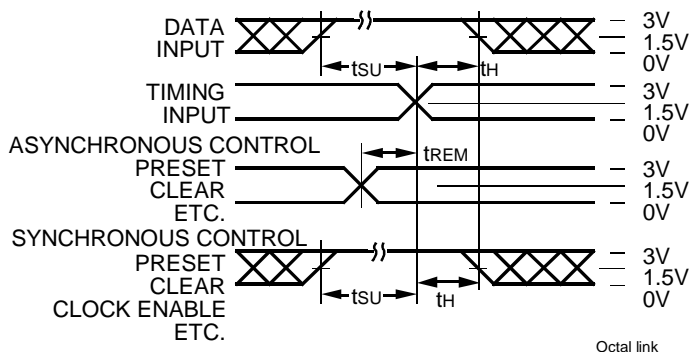
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

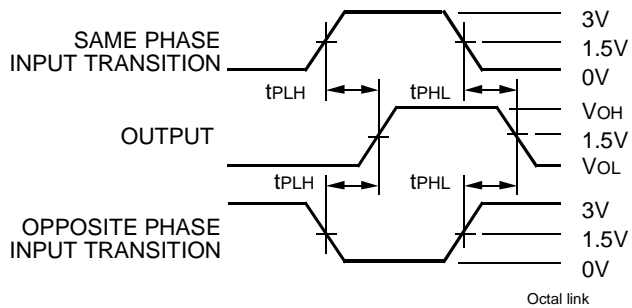
## TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



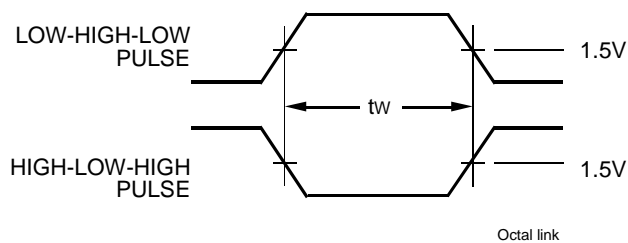
Propagation Delay

## SWITCH POSITION

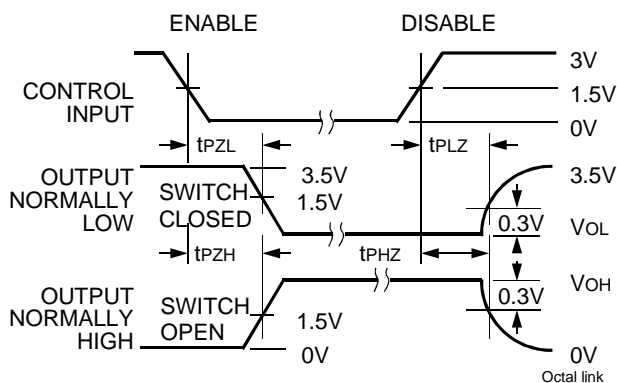
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

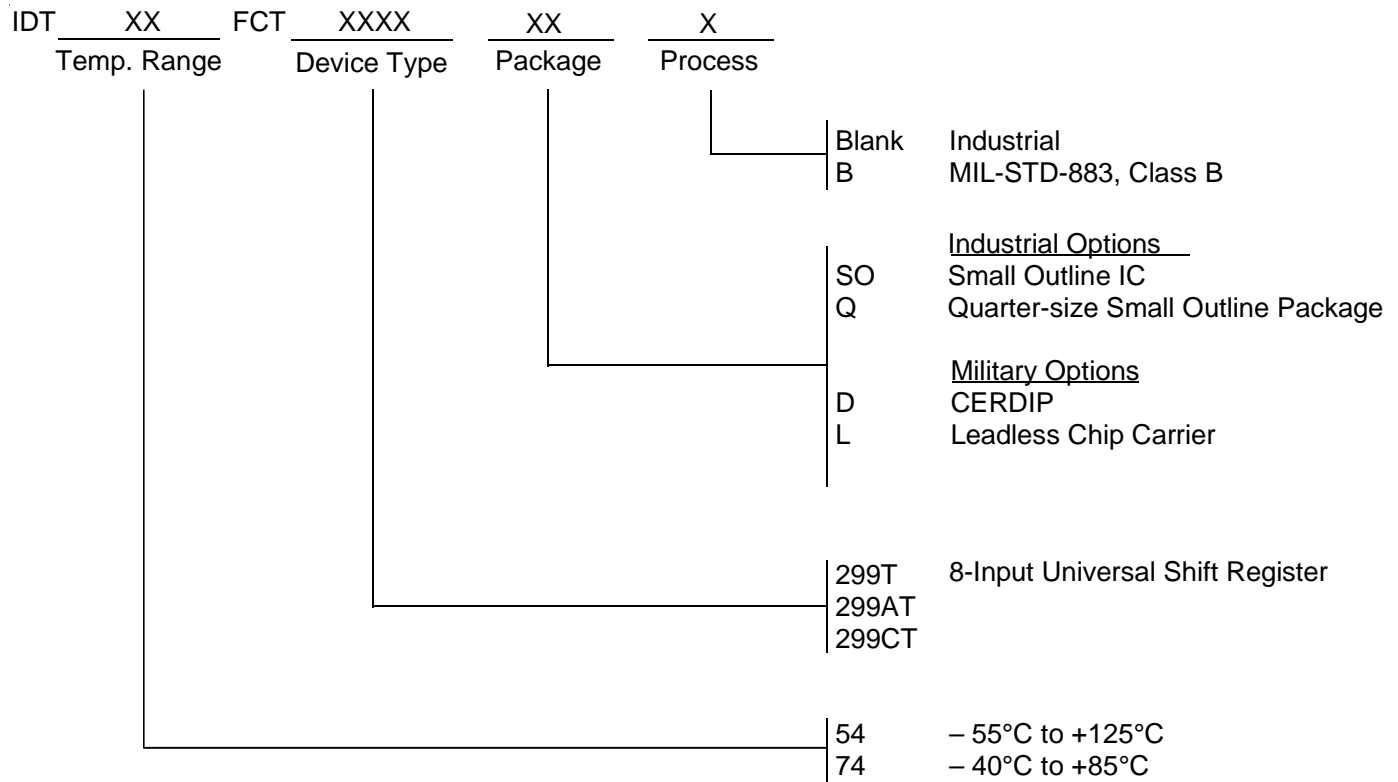


Enable and Disable Times

### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/24/2002 Updated as per PDNs Logic-00-07 and Logic-01-04



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