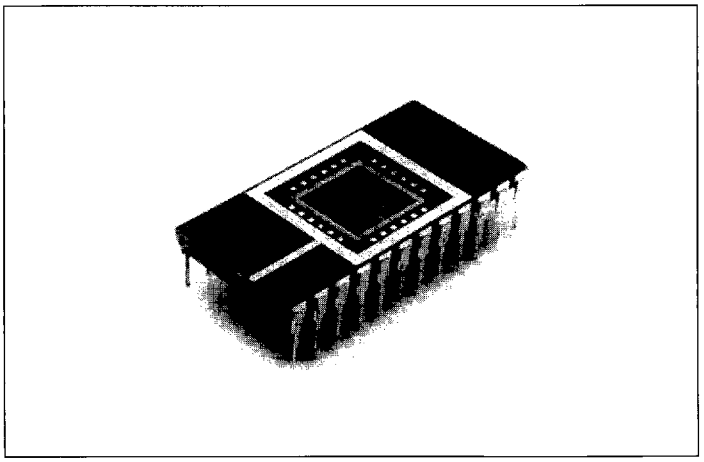
LORAL
Fairchild Imaging Sensors

CCD412A
512 x 512 Element
Full Frame Image Sensor

FEATURES

- **512 x 512 Photosite Array**
- **15μm x 15μm Pixel**
- **7.68mm x 7.68 mm Image Area**
- **100% Fill Factor**
- **Multi-Pinned Phase (MPP) Option**
- **Readout Noise Less Than 7 Electrons at 250k pixels/ sec**
- **Dynamic Range 10000:1**
- **Single Output Channel**
- **Three Phase Buried Channel NMOS**



GENERAL DESCRIPTION

The CCD412A is a 512 x512 element solid state Charge Coupled Device (CCD) Full Frame area image sensor which is intended for use in high-resolution scientific, industrial, and commercial electro-optical systems. The CCD412A is organized as a matrix array of 512 horizontal by 512 vertical CCD photosites. The pixel pitch and spacing is 15μm.

The imaging array may be operated in one of three modes, Buried Channel, Multi-Pinned Phase (MPP) and Surface Channel. The Buried Channel operation offers low-noise performance and excellent charge transfer efficiencies. An additional implant under one vertical phase creates a virtual well which collects the photo-electrons with all Vertical clocks low during integration. This MPP mode decreases dark current down to 25 pA/cm² @ 25°C. The CCD412A may be operated in a Surface Channel mode to increase full well capacity.

Excellent low noise performance is achieved by use of the buried channel CCD structure and a single stage low noise output amplifier.

Device processing uses 2.5 micron design rules. The single metal, triple-poly process allows a photosite layout with smaller pixel geometries and fewer array blemishes.

FUNCTIONAL DESCRIPTION

The CCD412A consists of the following functional elements illustrated in the block diagram.

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photo-electrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be covered during readout.

Vertical Charge Shifting: The Full Frame architecture of the CCD412A provides video information as a single sequential readout of 512 lines containing 512 photosite elements. At the end of an integration period the ϕV_1, ϕV_2, and ϕV_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The Vertical Transfer Gate (ϕVTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ϕVTG may be tied to ϕV_3.

Horizontal Charge Shifting: ϕH_1, ϕH_2, and ϕH_3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. With binning the array can be operated normally at full resolution as a 256 x 512, 256 x 256 or some other resolution.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 16 additional register cells between the first pixel of each line and the output amplifer. The output from these locations contain no signal and may be used as a dark level reference. The output video is available following the high-to-low transition of ϕH_1.

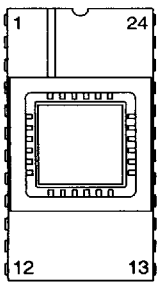
The reset FET in the horizontal readout, clocked appropriately with ϕR, allows binning of adjacent pixels.

Output Amplifier: The CCD412A has one output amplifier at the end of the horizontal transport register. It is a two-stage FET floating diffusion amplifier with a reset MOSFET tied to its input gate.

Charge packets are clocked to a precharged capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{OUT} pin. The capacitor is reset with ϕR to a precharge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOFSET.

PIN NUMBER/NAME			
1	ϕV1	24	ϕV2
2		23	
3	ϕV3	22	
4		21	ϕVTG
5		20	
6	ϕVTG	19	ϕH3
7	VOG	18	ϕH2
8		17	
9	ϕR	16	ϕH1
10	VRD	15	VSS
11	VRT	14	VSS
12	$VIDEO_{OUT}$	13	VDD

PIN CONNECTIONS



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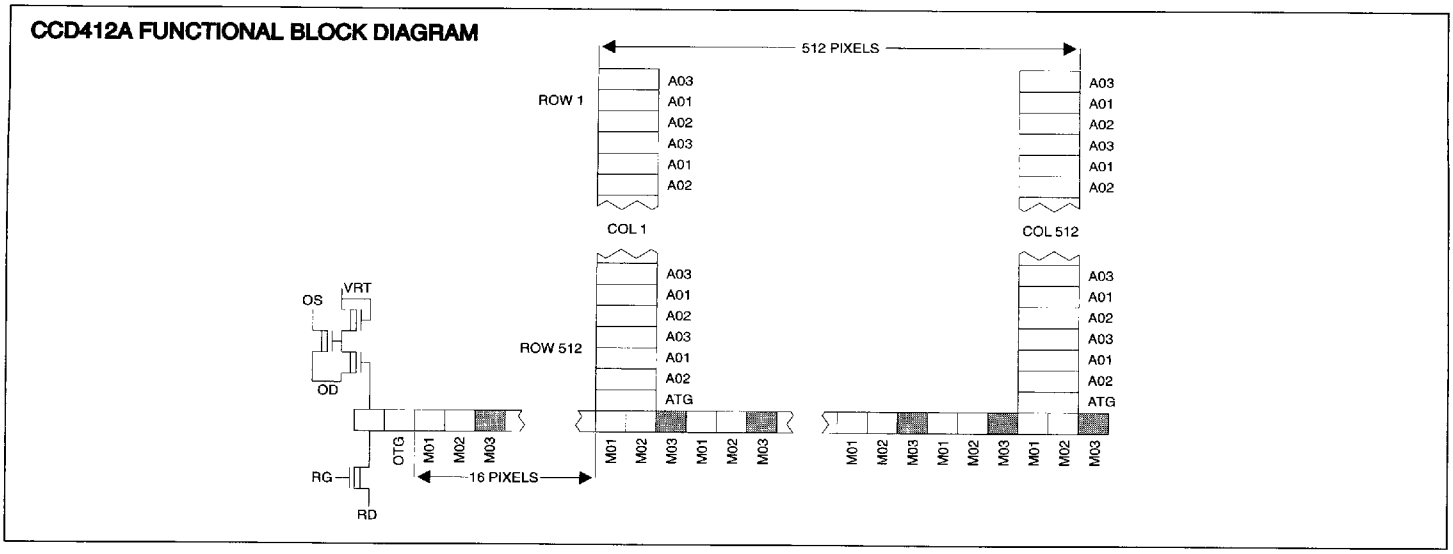
CCD412A FUNCTIONAL BLOCK DIAGRAM



The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

Multi-Pinned Phase: MPP is a CCD technology which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an implant during the semiconductor manufacturing process.

This implant creates a virtual well in the array which allows charge integration while maintaining pixel integrity with the Vertical clocks in the low state. Leaving the Vertical clocks in the low state during the integration cycle is the method used to implement MPP mode.

A drawback to utilizing the MPP mode is reduced full well capacity. The virtual well created by the MPP implant does not hold as much charge as the normal buried channel operating mode which leaves one Vertical clock in the high state during integration.

The CCD412A may be operated in the conventional buried channel mode with an increase in charge capacity.

DEFINITION OF TERMS

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

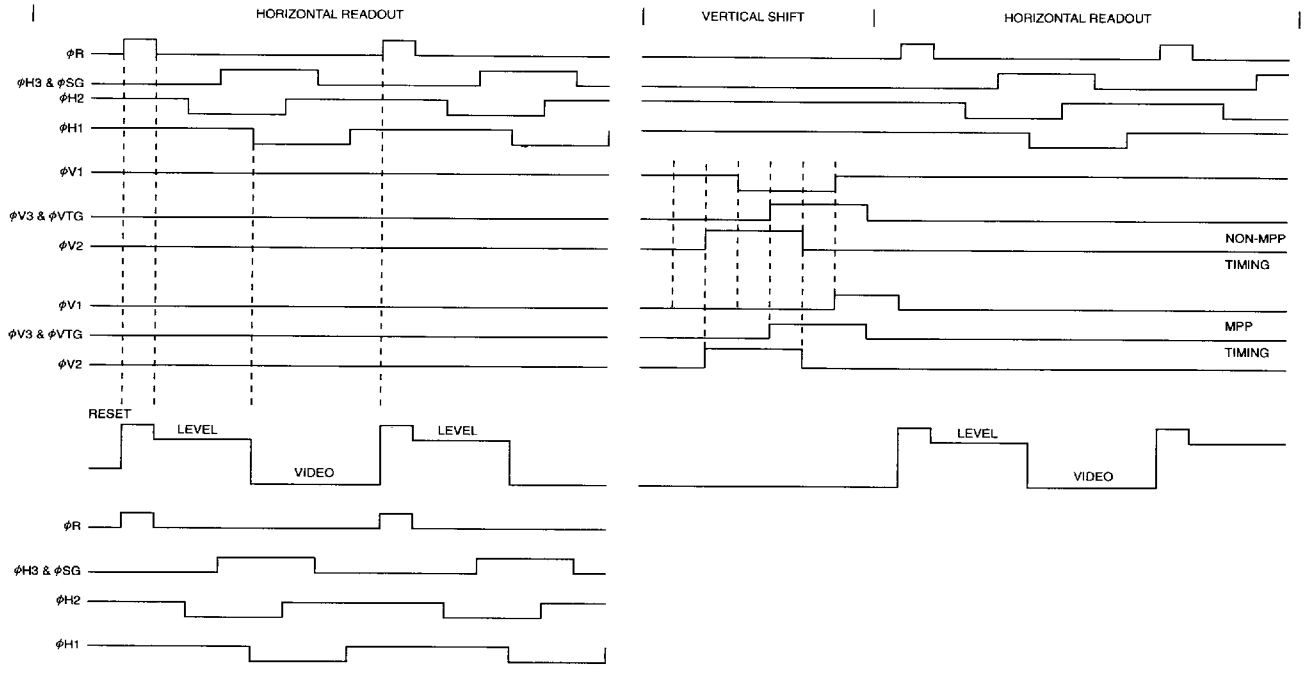
Vertical Transport Clocks ϕV_1, ϕV_2, ϕV_3 The clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕH_1, ϕH_2, ϕH_3 The clock signals applied to the horizontal transport registers.

Reset Clock ϕR The clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

TIMING DIAGRAM



Saturation Exposure The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Spectral Response Range The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Pixel Picture element or sensor element, also called photoelement or photosite.

Dark Signal The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ϕVTG Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V_{DD}	DC Supply Voltage		20.0		V	
V_{RD}	Reset Drain Voltage		13.0		V	
V_{OG}	Output Gate Voltage		1.0		V	
V_{SS}	Substrate Ground		0.0		V	

TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	BURIED CHANNEL		SURFACE CHANNEL		UNIT	REMARKS
		HIGH	LOW	HIGH	LOW		
$V_{\phi H(1,2,3)}$	Horizontal Clock	+5.0	-5.0	+16.0	0.0	V	Note 1
$V_{\phi V(1,2,3)}$	Vertical Clock	+4	-8.0	+14.0	0.0	V	Note 1
$V_{\phi R}$	Reset Clock	+10	0.0	+12.0	0.0	V	Note 1
$V_{\phi VTG}$	Vertical Transfer Gate Clock	+4	-8.0	+14.0	0.0	V	Note 1

Note 1: ϕH = 150pF, ϕV=5000pF. All clock rise and fall times should be > 10ns.

AC CHARACTERISTICS

Standard test conditions are nominal MPP clocks and DC operating Voltages, 1 MHz Horizontal Data Rate, 6μSec Vertical shift cycle.

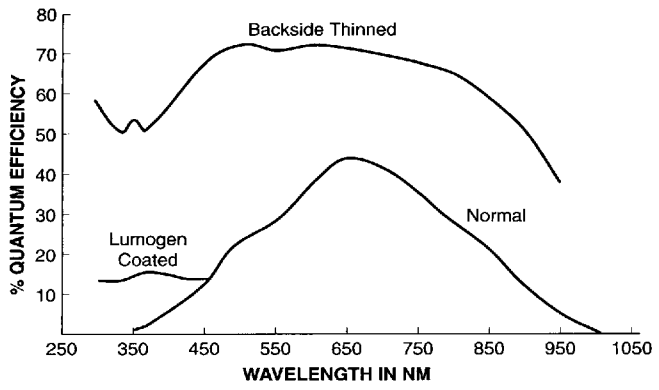
SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V_{ODC}	Output DC Level		14.0		V	
Z	Suggested Load Register	1.0	5.0	20	kΩ	

PERFORMANCE SPECIFICATIONS

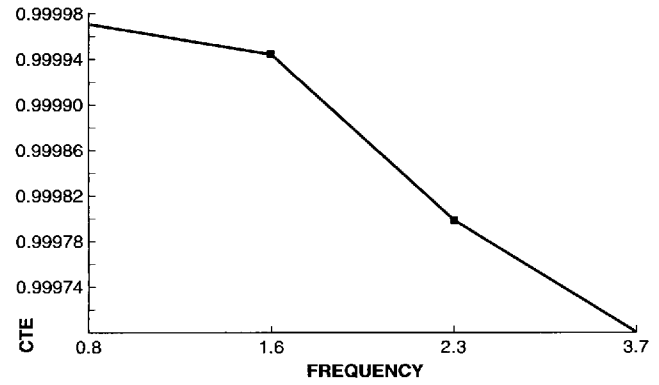
SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V_{SAT}	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity	200 100,000	 3.0	600 200,000	mV e- μV/e-	Note 1
PRNU	Photo Response Non-Uniformity Peak-to-Peak		10		%V_{SAT}	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025		2.0	nA/cm^2	Note 2
R	Responsivity		1.0		Vμj/cm^2	

Note 1: Maximum well capacity is achieved operating in Buried Channel Mode, minimum capacity is in MPP mode.
Note 2: Values shown are for 25°C. Dark current doubles for every 5° - 7°C.

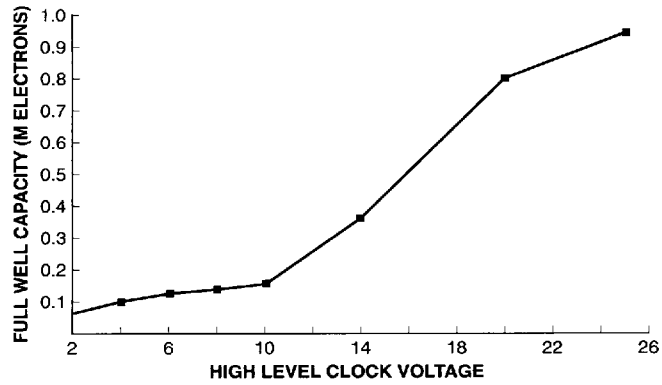
TYPICAL CCD QUANTUM EFFICIENCY



SURFACE CHANNEL MODE



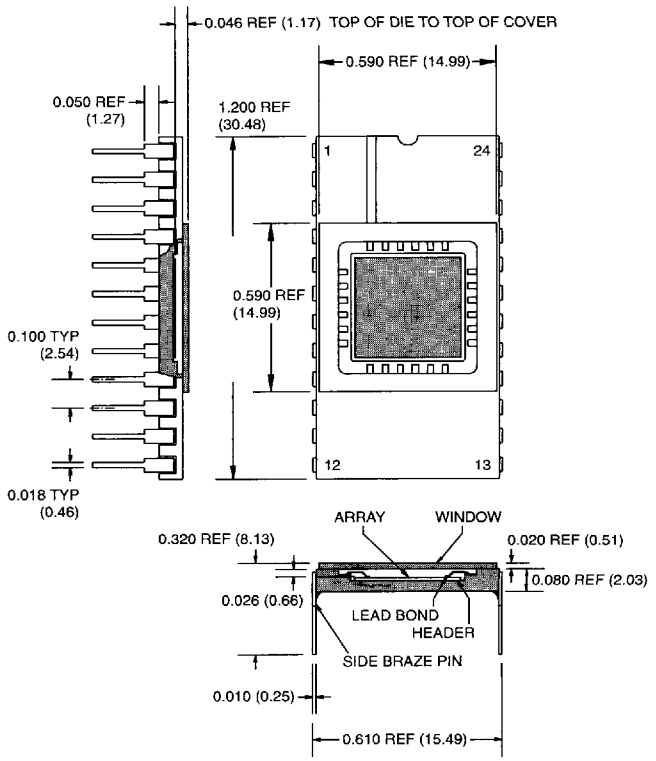
FULL WELL CAPACITY VS. HIGH LEVEL CLOCK VOLTAGE



QUANTUM EFFICIENCY ENHANCEMENTS

On a custom basis, our large area CCDs can be backside thinned for increased QE. The CCD is bump mated to a fanout and thinned to approximately 15 microns. The incident illumination enters through the backside of the array. Since no photons are absorbed in the polysilicon gate structures, the QE increases. We can also coat frontside illuminated devices with a fluorescent dye that absorbs UV light and fluoresces in the visible range. This provides CCD response at wavelengths less than 400nm.

CCD412A PACKAGE OUTLINE
24-PIN DUAL INLINE CERAMIC PACKAGE



All dimensions are in inches and millimeters (parentheses). Header is black ceramic (Al_2O_3). Window is glass.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and for different device temperatures.

The CCD412A is available in various standard grades, as well as custom selected grades. Consult the factory for available grading information and custom selections.

WARRANTY

Within twelve months of delivery to the end customer, Loral Fairchild will repair or replace, at our option, any Loral Fairchild camera product if any part is found to be defective in materials or workmanship. Contact factory for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Loral Fairchild Division certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.

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