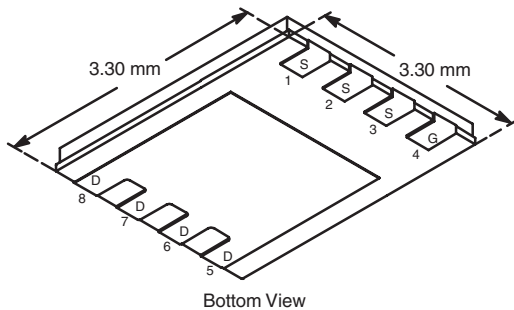




N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
30	0.024 at V _{GS} = 10 V	12	3.8 nC
	0.030 at V _{GS} = 4.5 V	12	

PowerPAK 1212-8



Bottom View

FEATURES

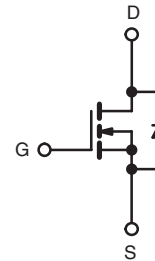
- Halogen-free According to IEC 61249-2-21
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook PC
- System Power
- Load Switch



N-Channel MOSFET

Ordering Information: SiS412DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	± 20	V
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	12 ^a
		T _C = 70 °C	12 ^a
		T _A = 25 °C	8.7 ^{b, c}
		T _A = 70 °C	7 ^{b, c}
Pulsed Drain Current	I _{DM}	30	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	12 ^a
		T _A = 25 °C	2.7 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	5	A
Single Pulse Avalanche Energy	E _{AS}	1.25	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	15.6
		T _C = 70 °C	10
		T _A = 25 °C	3.2 ^{b, c}
		T _A = 70 °C	2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{e, f}		260	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	32	39	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	6.5	8	

Notes:

- Package Limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 81 °C/W.
- See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 7.8\text{ A}$		0.020	0.024	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 7.0\text{ A}$		0.024	0.030	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 7.8\text{ A}$		17		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		435		pF
Output Capacitance	C_{oss}			95		
Reverse Transfer Capacitance	C_{rss}			42		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 7.8\text{ A}$		8	12	nC
				3.8	6	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 7.8\text{ A}$		1.4		
Gate-Drain Charge	Q_{gd}			1.1		
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.5	3.2	4.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 2.4\text{ }\Omega$ $I_D \cong 6.3\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			13	20	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 2.4\text{ }\Omega$ $I_D \cong 6.3\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		5	10	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			4.2	A
Pulse Diode Forward Current	I_{SM}				30	
Body Diode Voltage	V_{SD}	$I_S = 6.3\text{ A}$, $V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 6.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$		15	25	ns
Body Diode Reverse Recovery Charge	Q_{rr}			7	12	nC
Reverse Recovery Fall Time	t_a			9		ns
Reverse Recovery Rise Time	t_b			6		

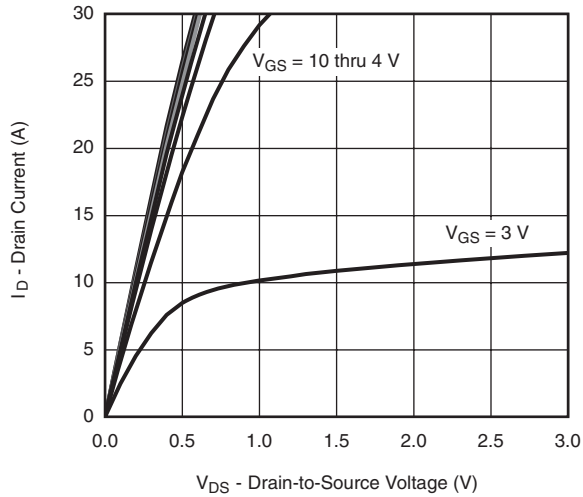
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

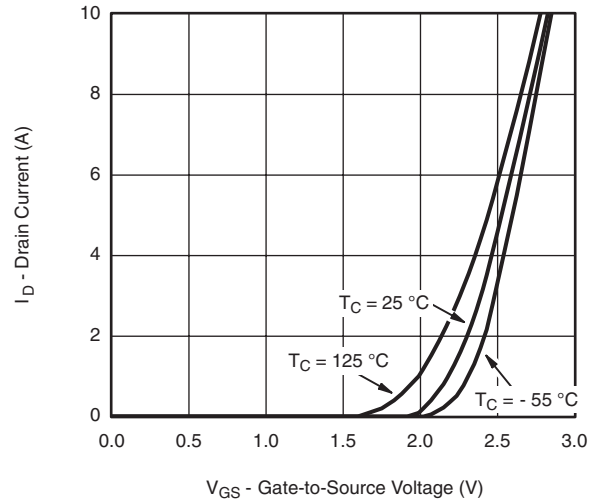
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



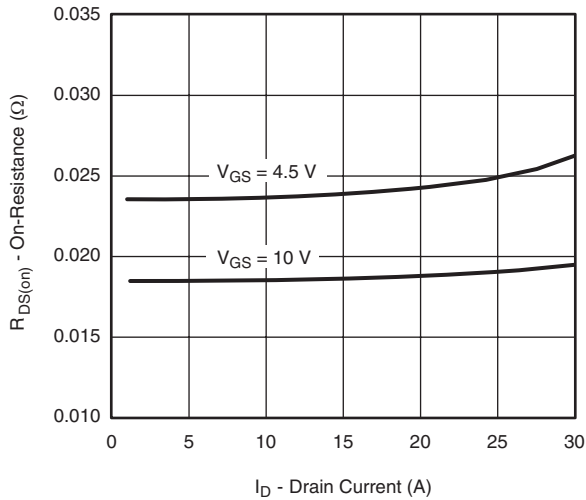
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



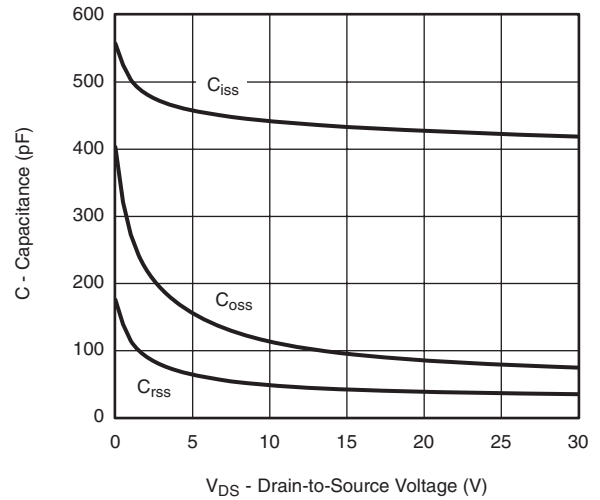
Output Characteristics



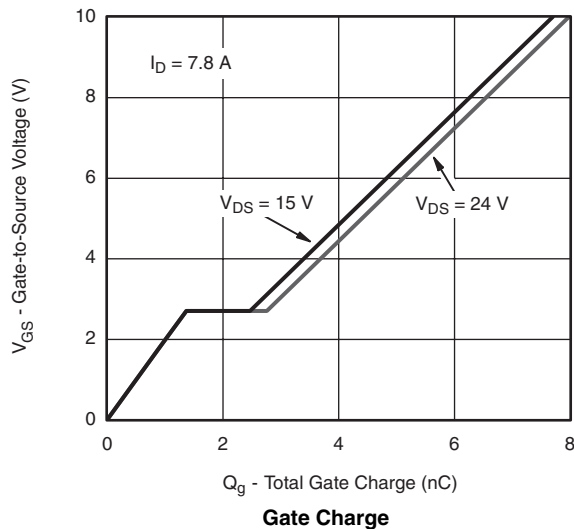
Transfer Characteristics



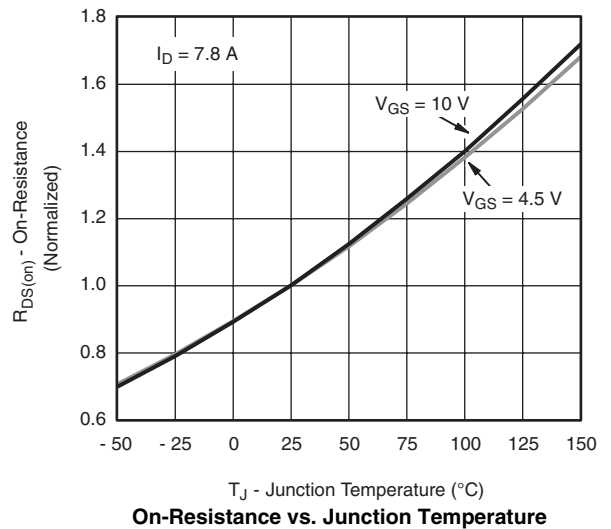
On-Resistance vs. Drain Current



Capacitance



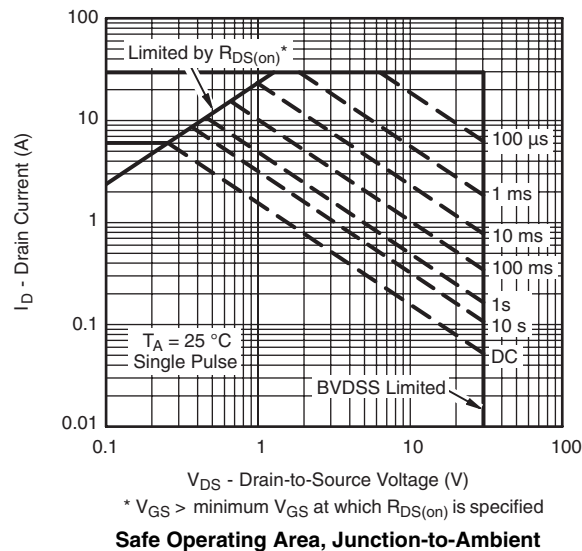
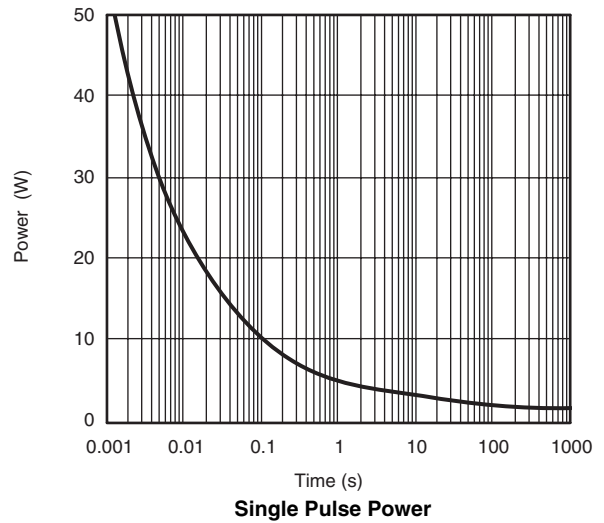
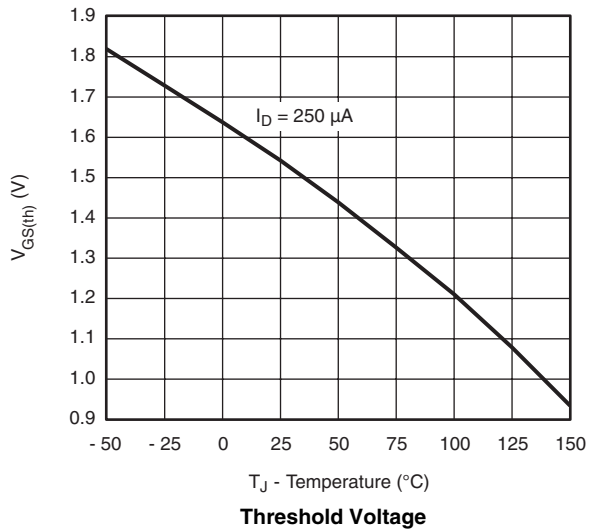
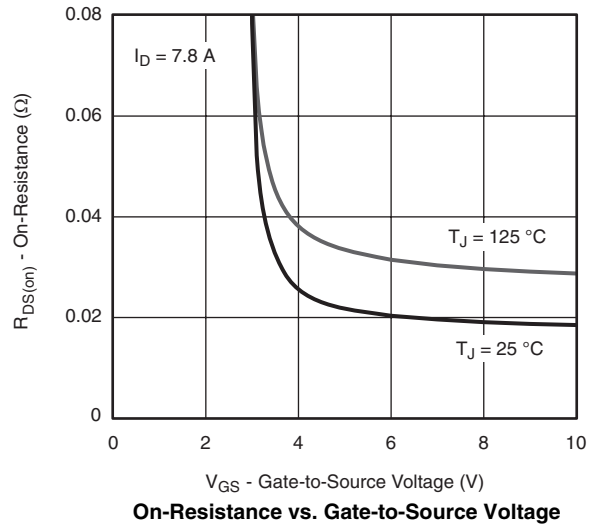
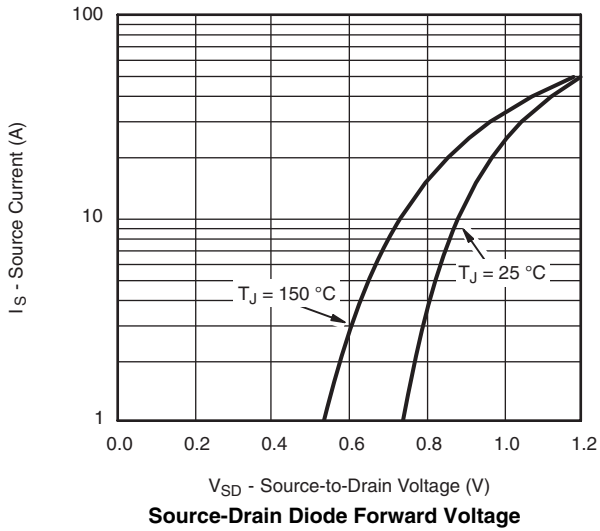
Gate Charge



On-Resistance vs. Junction Temperature

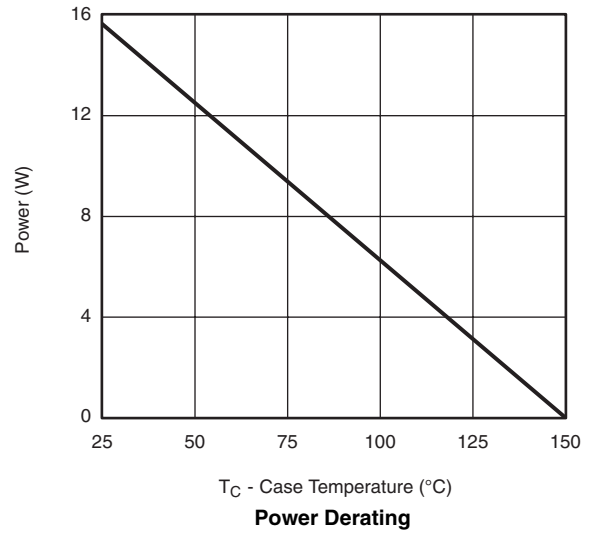
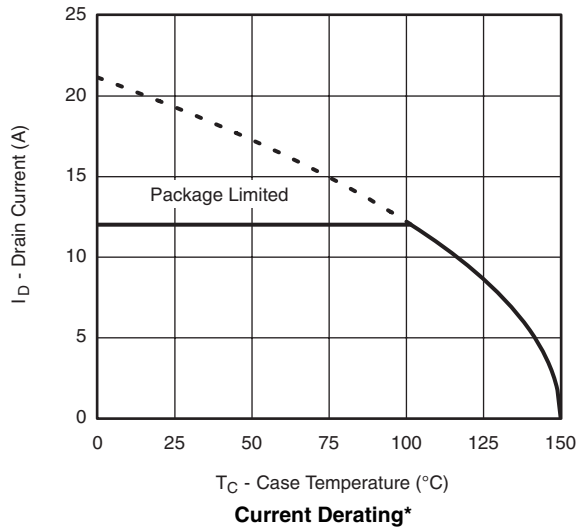


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





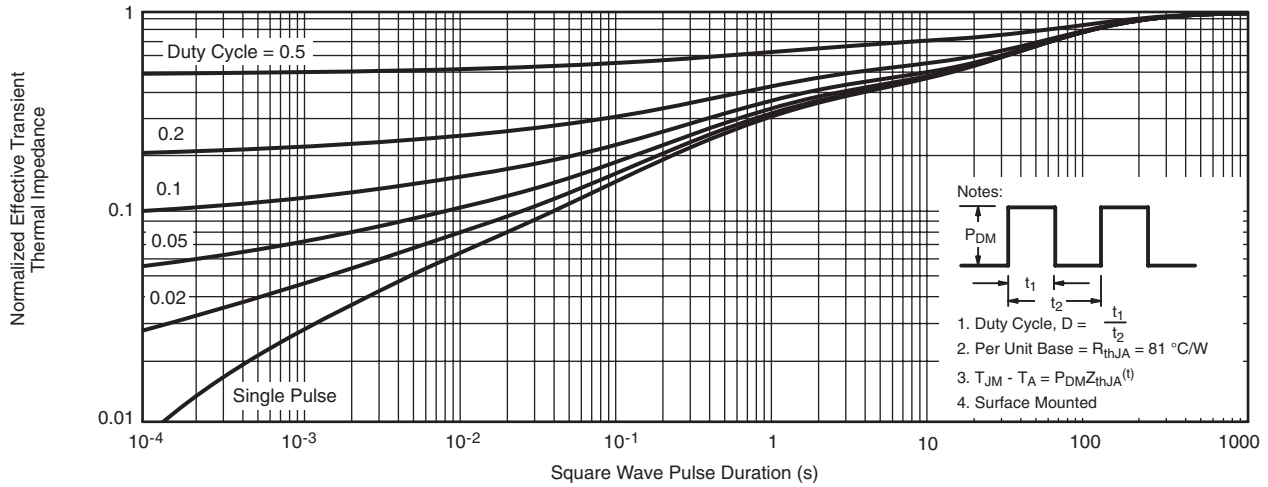
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



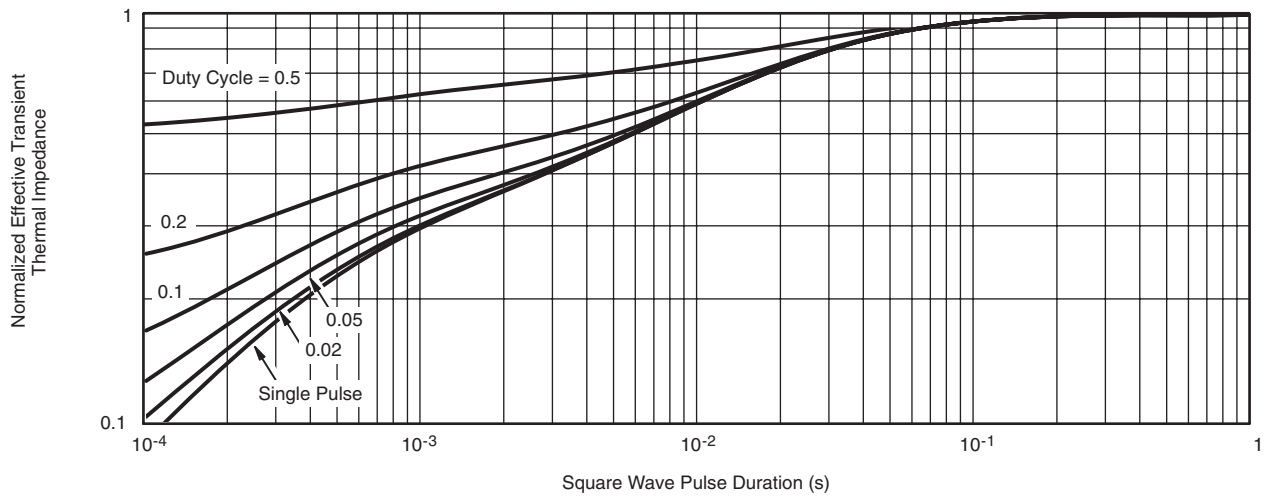
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69006.



Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.