IC for System Reset
Monolithic IC PST591~595 Series

October 15, 2004

Outline

This IC functions in a variety of CPU systems and other logic systems, to detect supply voltage and reset the system accurately when the power is turned on or interrupted. It incorporates a fixed-delay time generation circuit. These are other system reset ICs such as PST574 and PST575 (both conventional). In particular, this IC is a low-reset type system reset IC having a counter timer comprising of analog/digital mixed circuits. PST591- 595 have a different delay time respectively.

Features

1. Fixed delay time setting by counter timer
   Excellent delay time temperature characteristics ±800ppm/℃
2. Low operating limit voltage 0.65V typ.
3. Hysteresis voltage provided for detection voltage 50mV typ.
4. No-load current consumption I_{CCL}=300μA typ. I_{CCH}=200μA typ.
5. 5 models are available for different delay times.

	PST591 50ms	PST594 400ms
	PST592 100ms	PST595 800ms
	PST593 200ms	

6. Each model has 9 detection voltage ranks.

C : 4.5V typ.	H : 3.1V typ.
D : 4.2V typ.	I : 2.9V typ.
E : 3.9V typ.	J : 2.7V typ.
F : 3.6V typ.	K : 2.5V typ.
G : 3.3V typ.	

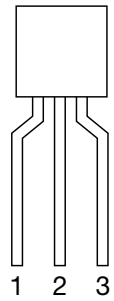
Packages

MMP-4A (PST59×□M)
TO-92A (PST59×□)
*The box represents a rank of detection voltage.
(MMP-4A has a manual reset pin, which should be connected to GND or NC during normal operation.)

Applications

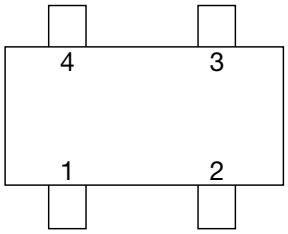
1. Reset circuits for microcomputers, CPUs and MPUs
2. Reset circuits for logic circuits
3. Battery voltage check circuits
4. Back-up power supply switching circuits
5. Level detection circuits
6. Mechanical reset circuits

Pin Assignment



TO-92A

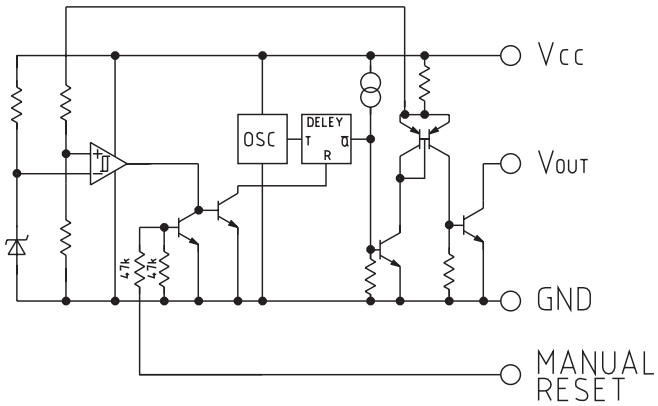
1	VCC
2	GND
3	VOUT



MMP-4A
(TOP VIEW)

1	VOUT
2	Manual Reset
3	VCC
4	GND

Equivalent Circuit Diagram



Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Units
Storage temperature	TSTG	–40~+125	℃
Operating temperature	TOPR	–20~+75	℃
Power supply voltage	VCC max.	–0.3~10	V
Manual reset input voltage	VRES max.	–0.3~10	V
Allowable loss	Pd	200 (MMP-4P) 300 (TO-92)	mW

Electrical Characteristics (Ta=25℃) (Except where noted otherwise, resistance unit is Ω)

Item		Symbol	Measuring circuit	Measurement conditions		Min.	Typ.	Max.	Unit
Detection voltage		Vs	1	RL=470 VOL ≦ 0.4V VCC=H→L	C	4.3	4.5	4.7	V
					D	4.0	4.2	4.4	
					E	3.7	3.9	4.1	
					F	3.4	3.6	3.8	
					G	3.1	3.3	3.5	
					H	2.9	3.1	3.3	
					I	2.75	2.90	3.05	
					J	2.55	2.70	2.85	
					K	2.35	2.50	2.65	
Hysteresis voltage		⊿Vs	1	RL=470, VCC=L→H→L		30	50	100	mV
Detection voltage temperature coefficient		Vs/⊿T	1	RL=470, Ta=–20℃~+75℃			±0.01		%/℃
Low-level output voltage		VOL	1	VCC=Vs min.–0.05V, RL=470			0.1	0.4	V
Output leakage current		IOH	1	VCC=10V				±0.1	μA
Circuit current while on		ICCL	1	VCC=Vs min.–0.05V, RL=∞			300	600	μA
Circuit current while off		ICCH	1	VCC=Vs typ./0.85V, RL=∞			200	350	μA
"H" transport delay time		tPLH	2	RL=4.7k CL=100PF ✶1	PST591	30	50	75	ms
					PST592	60	100	150	
					PST593	120	200	300	
					PST594	240	400	600	
					PST595	480	800	1200	
"L" transport delay time		tPHL	2	RL=4.7k, CL=100PF ✶1			10		μs
Operating power supply voltage		VOPL	1	RL=4.7k, VOL ≦ 0.4V			0.65	0.85	V
Output current while on 1		IOL1	1	VCC=Vs min.–0.05V, RL=0		8			mA
Output current while on 2		IOL2	1	Ta=–20℃~+75℃, RL=0 ✶2		6			mA
Manual reset pin	Input high voltage	VRESH				2.0			V
	Input high current	VRESH		VRES=2V				80	μA
	Input low voltage	VRESL						0.8	V

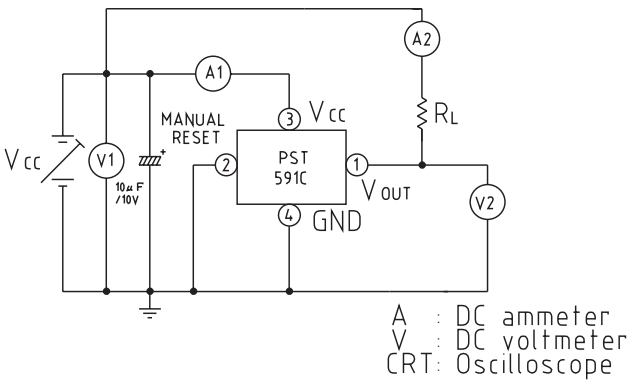
✶1 tpLH : VCC= (Vs typ.–0.4V) → (Vs typ.+0.4V), tpHL : VCC= (Vs typ.+0.4V) → (Vs typ.–0.4V)

✶2 VCC=Vs min.–0.15V

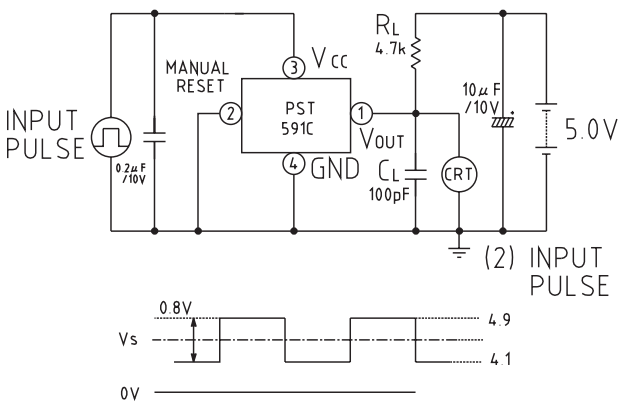
Note 3: VOUT pin is low when manual reset pin is high.
VOUT pin is high when manual reset pin is low.

Measuring Circuit

[1]



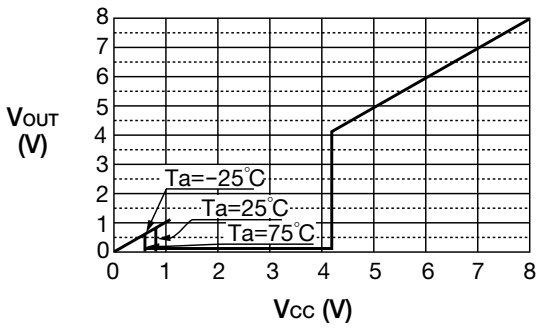
[2]



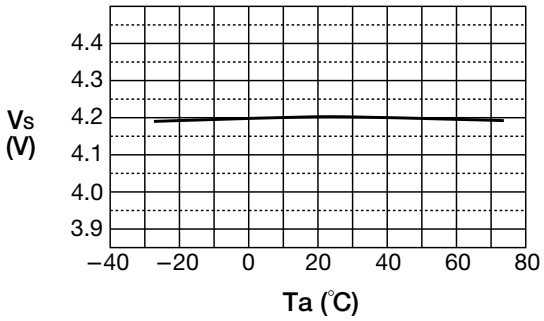
Note: Input model is an example for PST591C.

Characteristics (Example: PST591D)

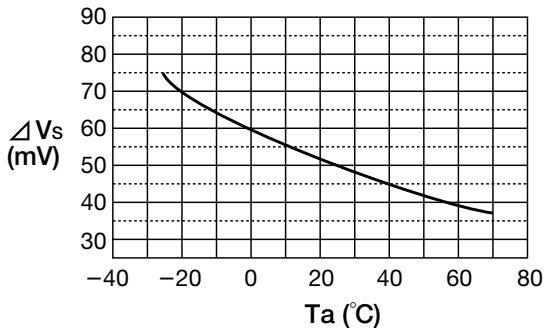
VCC vs. VOUT



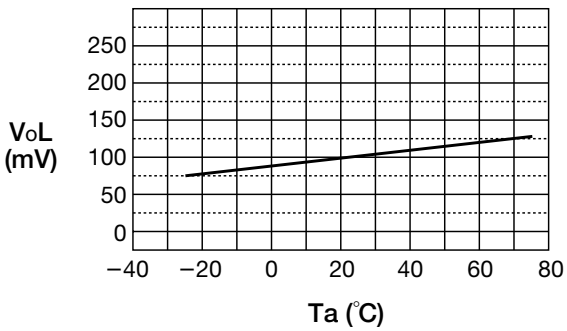
VS vs. Ta



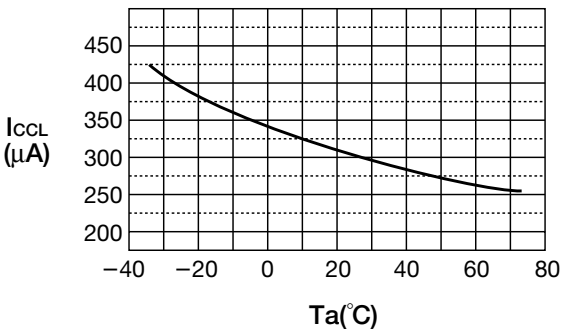
⊿VS vs. Ta



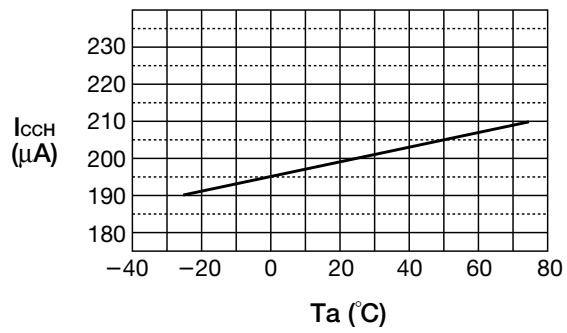
VOL vs. Ta



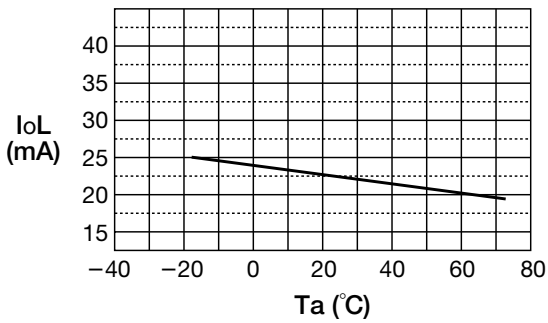
ICCL vs. Ta



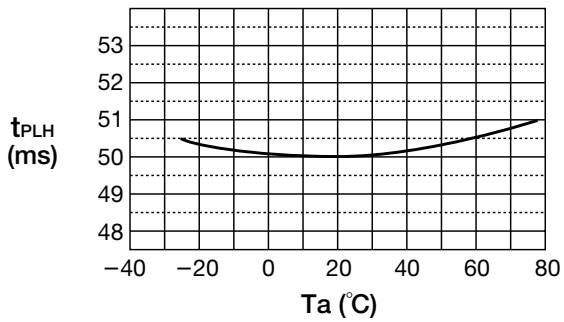
ICCH vs. Ta



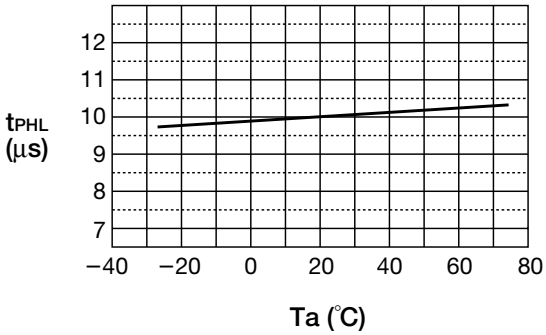
IOL vs. Ta



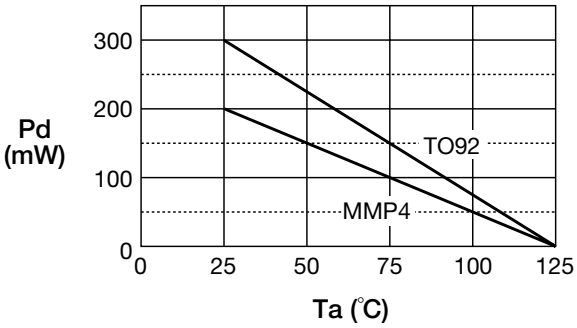
tPLH vs. Ta



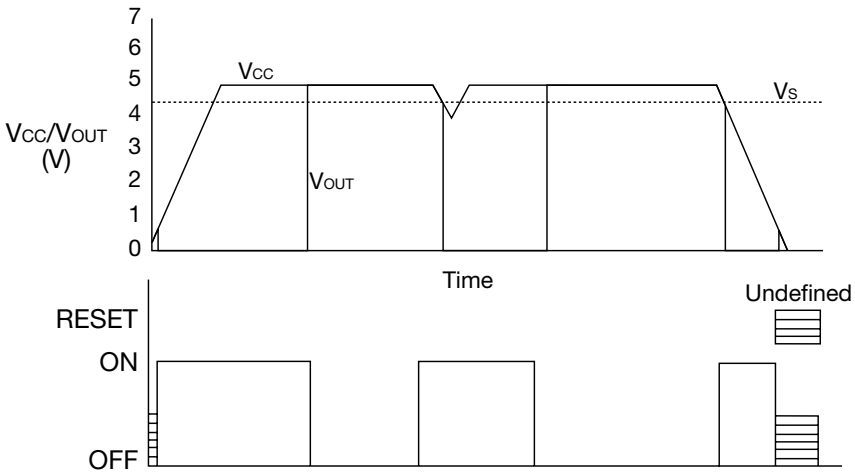
tPHL vs. Ta



Pd vs. Ta

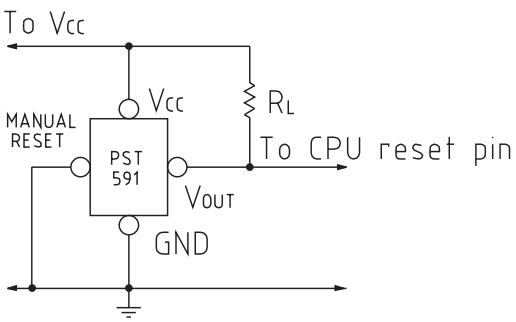


Timing Chart



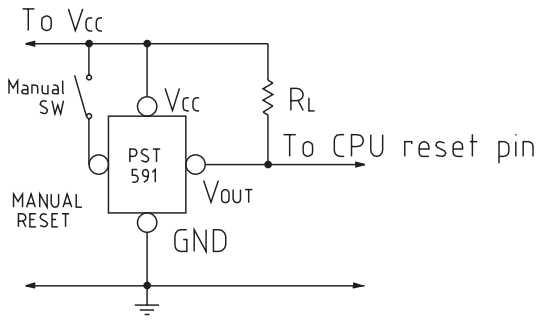
Application circuits

1. Normal hard reset



Note: Connect a capacitor between IC Vcc and GND pins if Vcc line impedance is high.

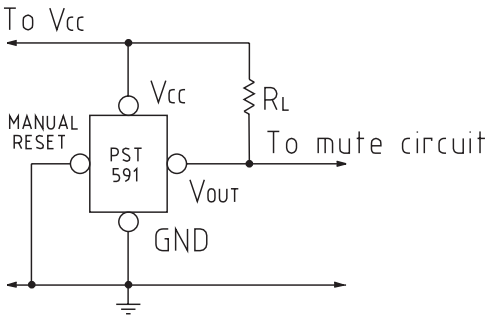
2. Manual reset



V_{OUT} pin low for manual switch ON.
V_{OUT} pin high for manual switch OFF.

Note1: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.
Note2: Thoroughly check the actual operation of the circuit, then set the manual reset when pressing the manual switch ON to about 2μs.

3. Mute circuit



Note: Connect a capacitor between IC V_{CC} and GND pins if V_{CC} line impedance is high.