

# P4C198/P4C198L, P4C198A/P4C198AL

## ULTRA HIGH SPEED 16K x 4

### STATIC CMOS RAMS (SCRAMS)



#### FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 12/15/20/25/35 ns (Commercial)
  - 15/20/25/35/45/55 ns (Military)
- Low Power Operation (Commercial/Military)
  - 715 mW Active – 12/15
  - 550/660 mW Active – 20/25/35/45/55
  - 193/220 mW Standby (TTL Input)
  - 83/110 mW Standby (CMOS Input) P4C198/198A
  - 9 mW Standby (CMOS Input) P4C198L/198AL (Military)
- 5V ± 10% Power Supply
- Data Retention, 10 μA Typical Current from 2.0V P4C198L/198AL (Military)
- Output Enable & Chip Enable Control Functions
  - Single Chip Enable P4C198
  - Dual Chip Enable P4C198A
- Common Inputs and Outputs
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE Technology™
- Standard Pinout (JEDEC Approved)
  - 24-Pin 300 mil DIP, SOJ (P4C198/198A)
  - 28-Pin 350 x 550 mil LCC (P4C198 only)



#### DESCRIPTION

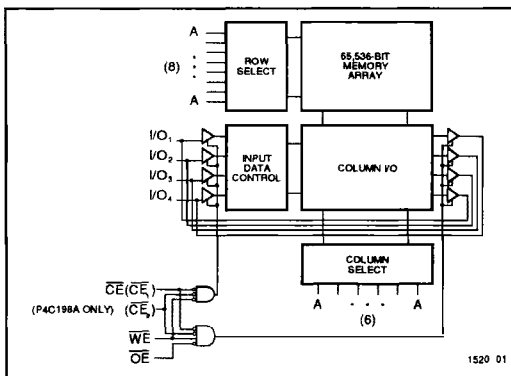
The P4C198/L and P4C198A/L are 65,536-bit ultra high-speed static RAMs organized as 16K x 4. Each device features an active low Output Enable control to eliminate data bus contention. The P4C198/L also have an active low Chip Enable (the P4C198A/L have two Chip Enables, both active low) for easy system expansion. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V ± 10% tolerance power supply. Data integrity is maintained with supply voltages down to 2.0V. Current drain is typically 10 μA from a 2.0V supply.

Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption to a low 715 mW active, 193 mW standby. The P4C198/L and P4C198A/L, are manufactured with PACE Technology, and are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies.

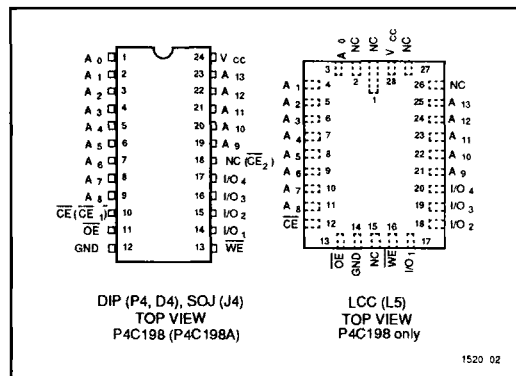
The P4C198/L and P4C198A/L are available in 24-pin 300 mil DIP and SOJ, and 28-pin 350 x 550 mil LCC packages providing excellent board level densities.



#### FUNCTIONAL BLOCK DIAGRAM



#### PIN CONFIGURATIONS



4



Means Quality, Service and Speed

©1992 Performance Semiconductor Corporation



### MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Pin with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub>	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>A</sub>	Operating Temperature	-55 to +125	°C

1520 Tbl 01

Symbol	Parameter	Value	Unit
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	DC Output Current	50	mA

1520 Tbl 02

### RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade <sup>(2)</sup>	Ambient Temperature	GND	V <sub>CC</sub>
Military	-55 to +125°C	0V	5.0V ± 10%

1520 Tbl 03

Grade <sup>(2)</sup>	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 10%

1520 Tbl 04

### DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

Symbol	Parameter	Test Conditions	P4C198 P4C198A		P4C198L P4C198AL		Unit	
			Min	Max	Min	Max		
V <sub>IH</sub>	Input High Voltage		2.2	V <sub>CC</sub> +0.5	2.2	V <sub>CC</sub> +0.5	V	
V <sub>IL</sub>	Input Low Voltage		-0.5 <sup>(3)</sup>	0.8	-0.5 <sup>(3)</sup>	0.8	V	
V <sub>HC</sub>	CMOS Input High Voltage		V <sub>CC</sub> -0.2	V <sub>CC</sub> +0.5	V <sub>CC</sub> -0.2	V <sub>CC</sub> +0.5	V	
V <sub>LC</sub>	CMOS Input Low Voltage		-0.5 <sup>(3)</sup>	0.2	-0.5 <sup>(3)</sup>	0.2	V	
V <sub>CD</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA		-1.2		-1.2	V	
V <sub>OL</sub>	Output Low Voltage (TTL Load)	I <sub>OL</sub> = +10 mA, V <sub>CC</sub> = Min. I <sub>OL</sub> = +8 mA, V <sub>CC</sub> = Min.		0.5 0.4		0.5 0.4	V	
V <sub>OH</sub>	Output High Voltage (TTL Load)	I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.	2.4		2.4		V	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max. V <sub>IN</sub> = GND to V <sub>CC</sub>	Mil. Com'l.	-10 -5	+10 +5	-5 n/a	+5 n/a	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., CE = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	Mil. Com'l.	-10 -5	+10 +5	-5 n/a	+5 n/a	μA

1520 Tbl 05

### CAPACITANCES<sup>(4)</sup>

(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	pF

1520 Tbl 06

Symbol	Parameter	Conditions	Typ.	Unit
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	pF

1520 Tbl 07

#### Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V<sub>IL</sub> and I<sub>IL</sub> not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20 ns.
- This parameter is sampled and not 100% tested.



## POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

Symbol	Parameter	Test Conditions	P4C198 P4C198A		P4C198L P4C198AL		Unit
			Min	Max	Min	Max	
$I_{CC}$	Dynamic Operating Current – 12, 15	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. — Com'l.	— n/a 130	— — —	n/a n/a n/a	mA
$I_{CC}$	Dynamic Operating Current – 20, 25, 35, 45, 55	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. — Com'l.	— 120 100	— — —	n/a n/a n/a	mA
$I_{SB}$	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1, \overline{CE}_2 \geq V_{IH},$ $V_{CC} = \text{Max.},$ $f = \text{Max.},$ Outputs Open	Mil. — Com'l.	— 40 35	— — —	40 n/a n/a	mA
$I_{SB1}$	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1, \overline{CE}_2 \geq V_{HC},$ $V_{CC} = \text{Max.},$ $f = 0,$ Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Mil. — Com'l.	— 20 15	— — —	1.5 n/a n/a	mA

n/a = Not Applicable

1520 Tbl 08

4

## DATA RETENTION CHARACTERISTICS (P4C198L/P4C198AL Military Temperature Only)

Symbol	Parameter	Test Condition	Min	Typ.* $V_{CC} =$		Max $V_{CC} =$		Unit
				2.0V	3.0V	2.0V	3.0V	
$V_{DR}$	$V_{CC}$ for Data Retention		2.0					V
$I_{CCDR}$	Data Retention Current			10	15	600	900	$\mu\text{A}$
$t_{CDR}$	Chip Deselect to Data Retention Time	$\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	0					ns
$t_R^\dagger$	Operation Recovery Time		$t_{RC}^\ddagger$					ns

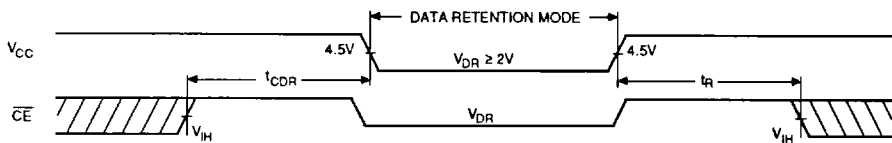
\* $T_A = +25^\circ\text{C}$

1520 Tbl 09

$^\ddagger t_{RC}$  = Read Cycle Time

$^\dagger$ This parameter is guaranteed but not tested.

## DATA RETENTION WAVEFORM



( $\overline{CE}_1$ , or  $\overline{CE}_2$ , for the P4C198AL)

1520 03

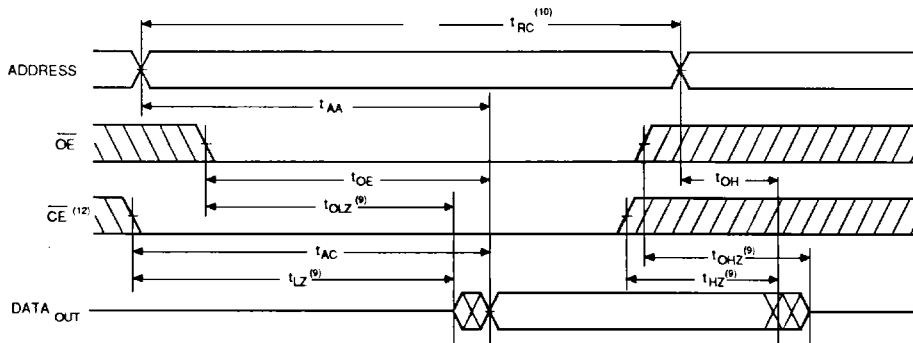
### AC CHARACTERISTICS—READ CYCLE

( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{RC}$	Read Cycle Time	12		15		20		25		35		45		55		ns
$t_{AA}$	Address Access Time		12		15		20		25		35		45		55	ns
$t_{AC}$	Chip Enable Access Time		12		15		20		25		35		45		55	ns
$t_{OH}$	Output Hold from Address Change	1		2		3		3		3		3		3		ns
$t_{LZ}$	Chip Enable to Output in Low Z	2		2		2		2		3		3		3		ns
$t_{HZ}$	Chip Disable to Output in High Z		6		7		10		10		14		15		20	ns
$t_{OE}$	Output Enable Low to Data Valid		7		9		12		15		25		30		35	ns
$t_{OLZ}$	Output Enable to Output in Low Z	2		2		2		2		3		3		3		ns
$t_{OHZ}$	Output Disable to Output in High Z		6		6		8		10		14		15		20	ns
$t_{PU}$	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
$t_{PD}$	Chip Disable to Power Down Time		12		15		20		25		35		45		55	ns

1520 Tbl 10

#### READ CYCLE NO.1 ( $\overline{OE}$ controlled)<sup>(5)</sup>

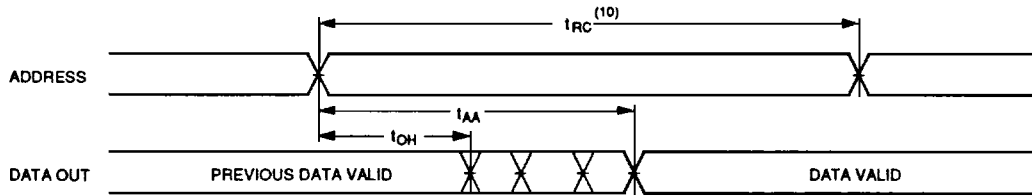


Notes:  
5.  $\overline{WE}$  is HIGH for READ cycle.

1520 04

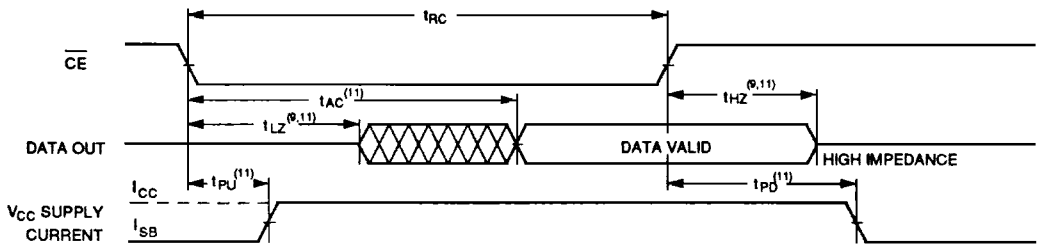


### READ CYCLE NO. 2 (ADDRESS Controlled)<sup>(5,6)</sup>



1520 05

### READ CYCLE NO. 3 ( $\overline{CE}^{(12)}$ Controlled)<sup>(5,7,8)</sup>



1520 06

#### Notes:

6.  $\overline{CE}$  ( $\overline{CE}_1$ ,  $\overline{CE}_2$  for P4C198A/L) and  $\overline{OE}$  are LOW READ cycle.
7.  $\overline{OE}$  is LOW for the cycle.
8. ADDRESS must be valid prior to, or coincident with  $\overline{CE}$  ( $\overline{CE}_1$  and  $\overline{CE}_2$  for P4C198A/L) transition LOW.
9. Transition is measured  $\pm 200\text{mV}$  from steady state voltage prior to change, with loading as specified in Figure 1.
10. Read Cycle Time is measured from the last valid address to the first transitioning address.
11. Transitions caused by a chip enable control have similar delays irrespective of whether  $\overline{CE}_1$  or  $\overline{CE}_2$  causes them (P4C198A/L).
12.  $\overline{CE}_1$ ,  $\overline{CE}_2$  for P4C198A/L.

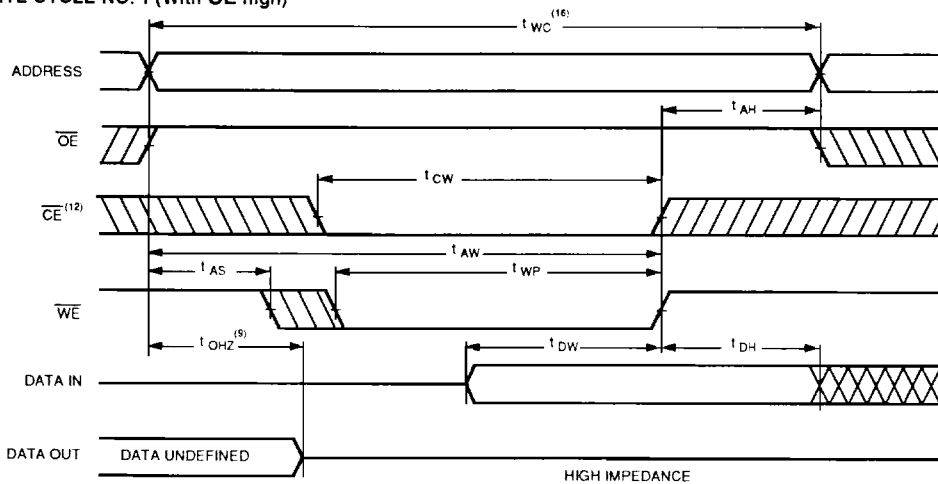
### AC CHARACTERISTICS—WRITE CYCLE

( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

Sym.	Parameter	-12		-15		-20		-25		-35		-45		-55		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{WC}$	Write Cycle Time	12		13		15		20		30		40		50		ns
$t_{CW}$	Chip Enable Time to End of Write	8		10		15		20		30		35		40		ns
$t_{AW}$	Address Valid to End of Write	8		10		15		20		25		35		40		ns
$t_{AS}$	Address Set-up Time	0		0		0		0		0		0		0		ns
$t_{WP}$	Write Pulse Width	9		10		12		20		25		35		40		ns
$t_{AH}$	Address Hold Time from End of Write	0		0		0		0		0		0		0		ns
$t_{DW}$	Data Valid to End of Write	6		7		10		13		15		20		25		ns
$t_{DH}$	Data Hold Time	0		0		0		0		0		0		0		ns
$t_{WZ}$	Write Enable to Output in High Z		6		7		8		10		10		15		20	ns
$t_{OW}$	Output Active from End of Write	2		2		2		3		3		3		3		ns

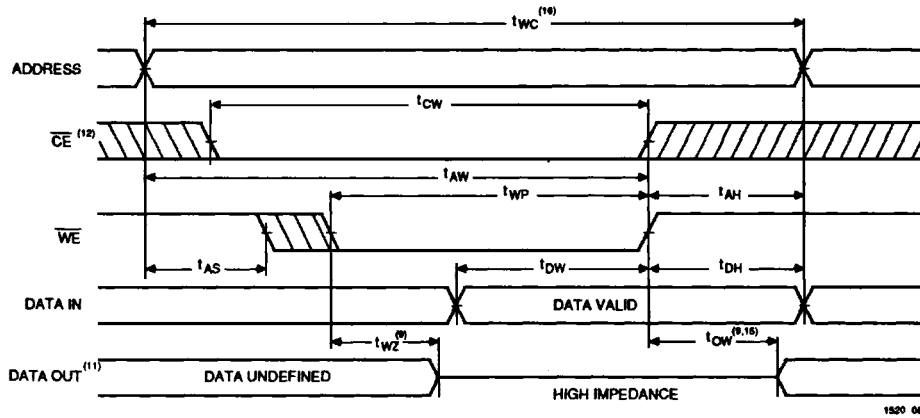
1520 TB 11

WRITE CYCLE NO. 1 (With  $\overline{OE}$  high)

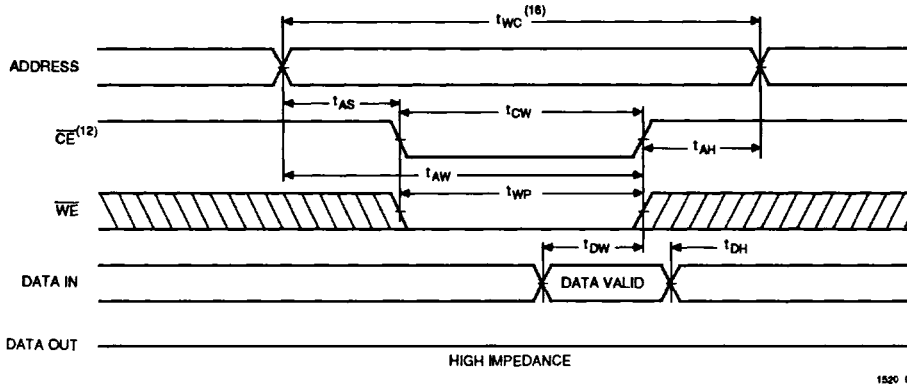


1520 07

WRITE CYCLE NO. 2 ( $\overline{WE}$  CONTROLLED) <sup>(13,14)</sup>



WRITE CYCLE NO. 3 ( $\overline{CE}^{(12)}$  CONTROLLED) <sup>(13,14)</sup>



Notes:

- 13.  $\overline{CE}$  ( $\overline{CE}_1$ ,  $\overline{CE}_2$  for P4C198A/L) and  $\overline{WE}$  must be LOW for WRITE cycle.
- 14.  $\overline{OE}$  is LOW for this WRITE cycle.

- 15. If  $\overline{CE}$  ( $\overline{CE}_1$  or  $\overline{CE}_2$  for P4C198A/L) goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.
- 16. Write Cycle Time is measured from the last valid address to the first transitioning address.

**TRUTH TABLES**

**P4C198/L**

CE	WE	OE	Mode	Output
H	X	X	Standby	High Z
L	H	H	Output Inhibit	High Z
L	H	L	READ	D <sub>OUT</sub>
L	L	X	WRITE	D <sub>IN</sub>

1520 Tbl 13

**P4C198A/L**

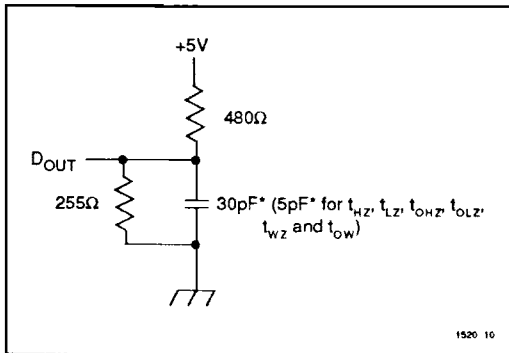
CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	Mode	Output
H	X	X	X	Standby	High Z
X	H	X	X	Standby	High Z
L	L	H	H	Output Inhibit	High Z
L	L	H	L	READ	D <sub>OUT</sub>
L	L	L	X	WRITE	D <sub>IN</sub>

1520 Tbl 14

**AC TEST CONDITIONS**

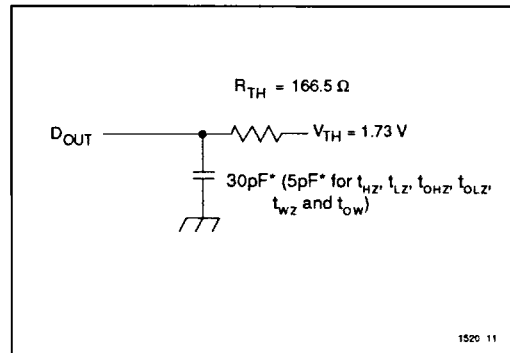
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

1520 Tbl 12



1520 10

Figure 1. Output Load



1520 11

Figure 2. Thevenin Equivalent

\* including scope and test fixture.

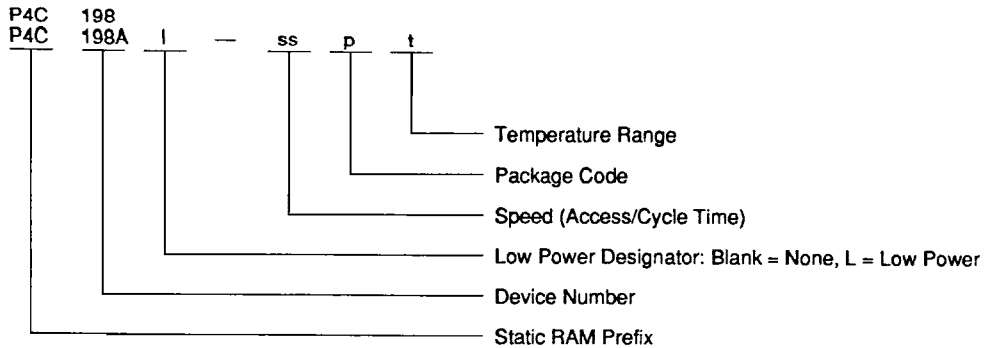
**Note:**

Because of the ultra-high speed of the P4C198/L and P4C198A/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V<sub>cc</sub> and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between

V<sub>cc</sub> and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D<sub>OUT</sub> to match 166Ω (Thevenin Resistance).



### ORDERING INFORMATION



- l = Ultra-low standby power designator L, if needed.
- ss = Speed (access/cycle time in ns), e.g., 25, 35
- p = Package code, i.e., P, J, L, D.
- t = Temperature range, i.e., C, M, MB.

1520 12

4

### PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide
L	Leadless Chip Carrier (ceramic)
D	CERDIP, 300 mil wide standard

1520 Tbx 14

### TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
M	Military Temperature Range, -55°C to +125°C.
MB	Mil. Temp. with MIL-STD-883D Class B compliance

1520 Tbx 15

### SELECTION GUIDE

The P4C198 and P4C198A are available in the following temperature, speed and package options. The P4C198L and P4C198AL are only available with access times 25ns and slower for military temperatures. The P4C198/198L and P4C198A/198AL are available to Standardized Military Drawings 5962-86859, 5962-89891 and 5962-89892. Check Mil-Bul-103 for current listing of part types.

Temperature Range	Package	Speed (ns)						
		12	15	20	25	35	45	55
Commercial	Plastic DIP	-12PC	-15PC	-20PC	-25PC	-35PC	N/A	N/A
	Plastic SOJ	-12JC	-15JC	-20JC	-25JC	-35JC	N/A	N/A
	CERDIP	N/A	-15CC	-20CC	-25CC	-35CC	N/A	N/A
	LCC	N/A	-15LC	-20LC	-25LC	-35LC	N/A	N/A
Military Temp.	CERDIP	N/A	N/A	-20DM	-25DM	-35DM	-45DM	-55DM
	LCC	N/A	N/A	-20LM	-25LM	-35LM	-45LM	-55LM
Military Processed*	CERDIP	N/A	N/A	-20DMB	-25DMB	-35DMB	-45DMB	-55DMB
	LCC	N/A	N/A	-20LMB	-25LMB	-35LMB	-45LMB	-55LMB

\* Military temperature range with MIL-STD-883 Revision D, Class B processing.  
N/A = Not available

1520 Tbx 16

