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MC68HC908QL4
MC68HC908QL3
MC68HC908QL2

Data Sheet

M68HC08
Microcontrollers

MC68HC908QL4/D
Rev. 0
9/2003

MOTOROLA.COM/SEMICONDUCTORS

MC68HC908QL4
MC68HC908QL3
MC68HC908QL2

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
September, 2003	N/A	Initial release	N/A

List of Sections

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Section 1. General Description

1.1 Introduction

The MC68HC908QL4 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is a Complex Instruction Set Computer (CISC) with a Von Neumann architecture. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Device Variations

Device	Memory Size	Analog-to-Digital Converter	Pin Count
MC68HC908QL4	4096 bytes FLASH	6 ch, 10 bit	16 pins
MC68HC908QL3	4096 bytes FLASH	—	16 pins
MC68HC908QL2	2048 bytes FLASH	6 ch, 10 bit	16 pins

1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- 5-V and 3.3-V operating voltages (V_{DD})
- 8-MHz internal bus operation at 5 V, 4-MHz at 3.3 V
- Trimmable internal oscillator
  - Selectable 3.2 or 6.4 MHz internal bus operation
  - 8-bit trim capability allows 0.4% accuracy(1)
  - ± 25% untrimmed

1. ±5% guaranteed accuracy over entire temperature and voltage range after trimming. LIN communication easily maintained under all conditions using SLIC module.

- Slave LIN interface Controller (SLIC) module
  - Full LIN messaging buffering of Identifier and 8 data bytes
  - Automatic baud rate and LIN message frame synchronization:
    - No prior programming of bit rate required, 1–20 kbps LIN bus speed operation
    - All LIN messages will be received (no message loss due to synchronization process)
    - Input clock tolerance as high as ±50%, allowing internal oscillator to remain untrimmed
    - Incoming break symbols allowed to be 10 to 20 bit times without message loss
    - Supports automatic software trimming of internal oscillator using LIN synchronization data
  - Automatic processing and verification of LIN SYNCH BREAK and SYNCH BYTE
  - Automatic checksum calculation and verification with error reporting
  - Maximum of 2 interrupts per LIN message frame
  - Full LIN error checking and reporting
  - High-speed LIN capability up to 83.33 kbps to 120.00 kbps
  - Configurable digital receive filter
- Auto wakeup from STOP capability
- In-system FLASH programming
- FLASH security(1)
- On-chip in-application programmable FLASH memory (with internal program/erase voltage generation)
  - MC68HC908QL4, MC68HC908QL3 — 4096 bytes
  - MC68HC908QL2 — 2048 bytes
- Read-only memory (ROM)
  - MC68HC908QL4, MC68HC908QL3 — 4096 bytes
  - MC68HC908QL2 — 2048 bytes
- 128 bytes of on-chip random-access memory (RAM)
- 2-channel, 16-bit timer interface module (TIM) with external clock source input
- 6-channel, 10-bit analog-to-digital converter (ADC) on MC68HC908QL4 and MC68HC908QL2
- 13 bidirectional input/output (I/O) lines and one input only:
  - Six shared with keyboard interrupt function
  - Six shared with ADC
  - Two shared with TIM
  - Two shared with SLC

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

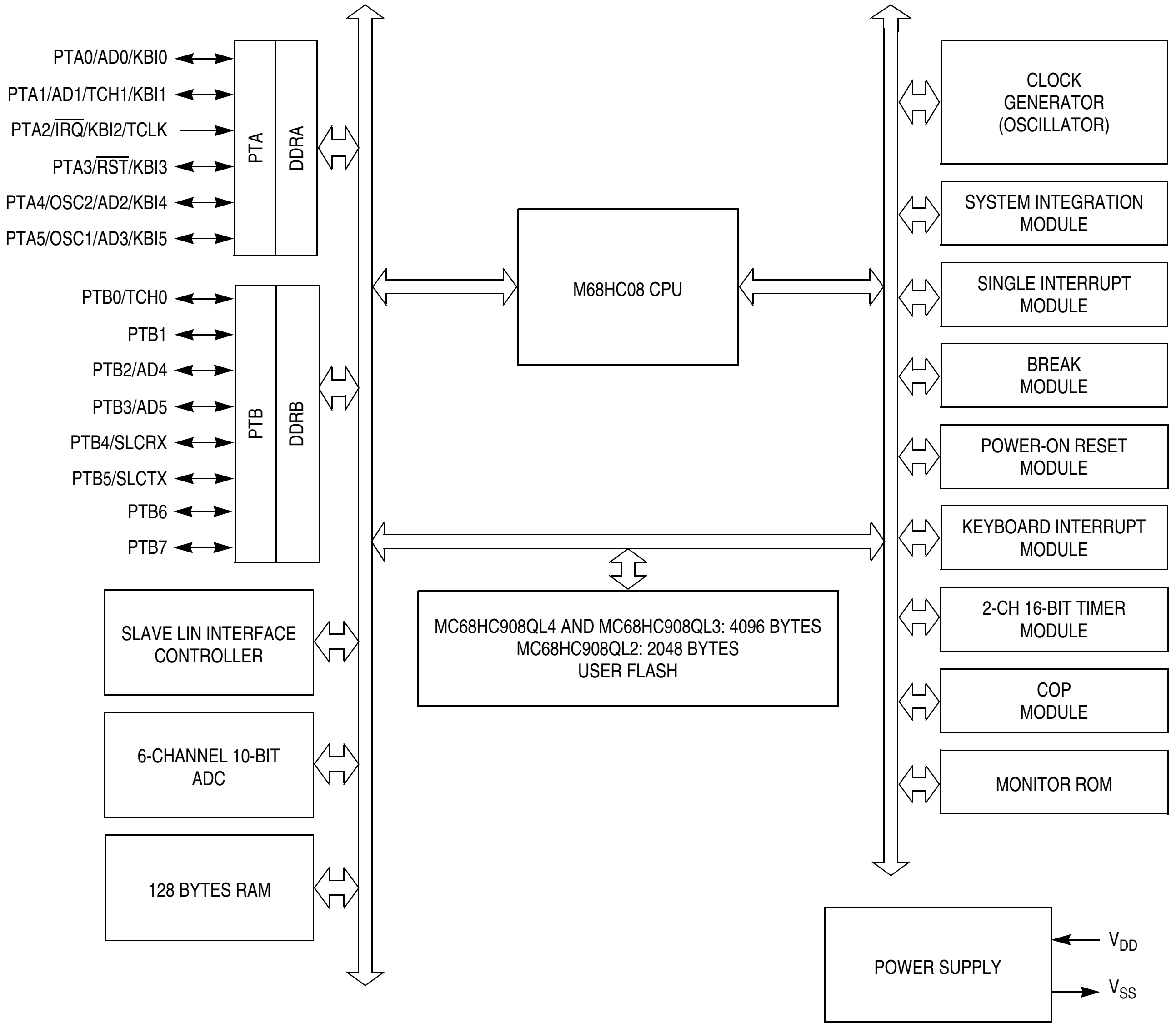
  - One shared with reset
  - One input only shared with external interrupt (IRQ)
  - High current sink/source capability
  - Selectable pullups on all ports, selectable on an individual bit basis
  - Three-state ability on all port pins
- 6-bit keyboard interrupt with wakeup feature (KBI)
- Low-voltage inhibit (LVI) module features:
  - Software selectable trip point in CONFIG register
- System protection features:
  - Computer operating properly (COP) watchdog
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ}}$) shared with general-purpose input pin
- Master asynchronous reset pin ($\overline{\text{RST}}$) shared with general-purpose input/output (I/O) pin
- Power-on reset
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce external components
- Memory mapped I/O registers
- Power saving stop and wait modes
- Available packages:
  - 16-pin plastic dual in-line package (PDIP)
  - 16-pin small outline integrated circuit (SOIC) package
  - 16-pin thin shrink small outline package (TSSOP)

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908QL4.



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30 kΩ) pull up
PTA0, PTA1, PTA3–PTA5: High current sink and source capability
PTA0–PTA5: Pins have programmable keyboard interrupt and pull up
ADC pins only available on MC68HC908QL4 and MC68HC908QL2

Figure 1-1. Block Diagram

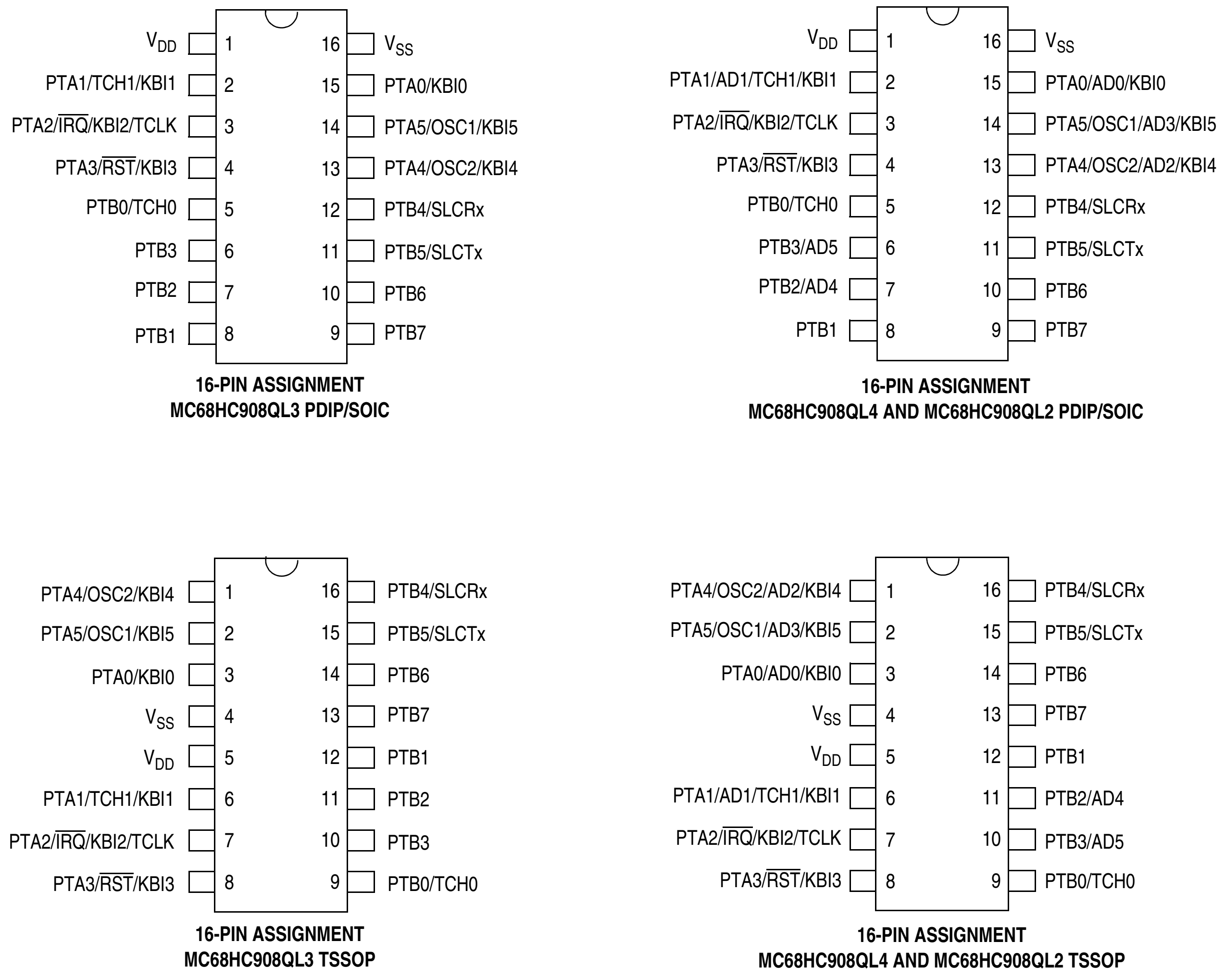


Figure 1-2. MCU Pin Assignments

1.4 Pin Functions

Table 1-2 provides a description of the pin functions.

Table 1-2. Pin Functions

Pin Name	Description	Input/Output
V$_{DD}$	Power supply	Power
V$_{SS}$	Power supply ground	Power
PTA0	PTA0 — General purpose I/O port	Input/Output
	AD0 — A/D channel 0 input	Input
	KBI0 — Keyboard interrupt input 0	Input

Table 1-2. Pin Functions (Continued)

Pin Name	Description	Input/Output
PTA1	PTA1 — General purpose I/O port	Input/Output
	AD1 — A/D channel 1 input	Input
	TCH1 — Timer Channel 1 I/O	Input/Output
	KBI1— Keyboard interrupt input 1	Input
PTA2	PTA2 — General purpose input-only port	Input
	$\overline{\text{IRQ}}$ — External interrupt with programmable pullup and Schmitt trigger input	Input
	KBI2 — Keyboard interrupt input 2	Input
	TCLK — External clock source input for the TIM module	Input
PTA3	PTA3 — General purpose I/O port	Input/Output
	$\overline{\text{RST}}$ — Reset input, active low with internal pullup and Schmitt trigger input	Input
	KBI3 — Keyboard interrupt input 3	Input
PTA4	PTA4 — General purpose I/O port	Input/Output
	OSC2 — XTAL oscillator output (XTAL option only) RC or internal oscillator output (OSC2EN = 1 in PTAPUE register)	Output Output
	AD2 — A/D channel 2 input	Input
	KBI4 — Keyboard interrupt input 4	Input
PTA5	PTA5 — General purpose I/O port	Input/Output
	OSC1 — XTAL, RC, or external oscillator input	Input
	AD3 — A/D channel 3 input	Input
	KBI5 — Keyboard interrupt input 5	Input
PTB0	PTB0 — General purpose I/O port	Input/Output
	TCH0 — Timer Channel 0 I/O	Input/Output
PTB1	PTB1 — General purpose I/O port	Input/Output
PTB2	PTB2 — General purpose I/O port	Input/Output
	AD4 — A/D channel 4 input	Input
PTB3	PTB3 — General purpose I/O port	Input/Output
	AD5 — A/D channel 5 input	Input
PTB4	PTB4 — General purpose I/O port	Input/Output
	SLCRx — SLC receive input	Input
PTB5	PTB5 — General purpose I/O port	Input/Output
	SLCTx — SLC transmit output	Output
PTB6, PTB7	General-purpose I/O port	Input/Output

1.5 Pin Function Priority

Table 1-3 is meant to resolve the priority if multiple functions are enabled on a single pin.

NOTE: *Upon reset all pins come up as input ports regardless of the priority table.*

Table 1-3. Function Priority in Shared Pins

Pin Name	Highest-to-Lowest Priority Sequence
PTA0	AD0 → TCH1 → KBI0 → PTA0
PTA1	AD1 → KBI1 → PTA1
PTA2	$\overline{\text{IRQ}}$ → KBI2 → TCLK → PTA2
PTA3	$\overline{\text{RST}}$ → KBI3 → PTA3
PTA4	OSC2 → AD2 → KBI4 → PTA4
PTA5	OSC1 → AD3 → KBI5 → PTA5
PTB0	TCH0 → PTB0
PTB1	PTB1
PTB2	AD4 → PTB2
PTB3	AD5 → PTB3
PTB4	SLCRx → PTB4
PTB5	SLCTx → PTB5

Section 2. Memory

2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in **Figure 2-1**, includes:

- 4096 bytes of user FLASH for MC68HC908QL4 and MC68HC908QL3
- 2048 bytes of user FLASH for MC68HC908QL2
- 128 bytes of random access memory (RAM)
- 48 bytes of user-defined vectors, located in FLASH
- 350 bytes of monitor read-only memory (ROM)
- 674 bytes of FLASH program and erase routines, located in auxiliary ROM

2.2 Unimplemented Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In **Figure 2-1** and in register figures in this document, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In **Figure 2-1** and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.

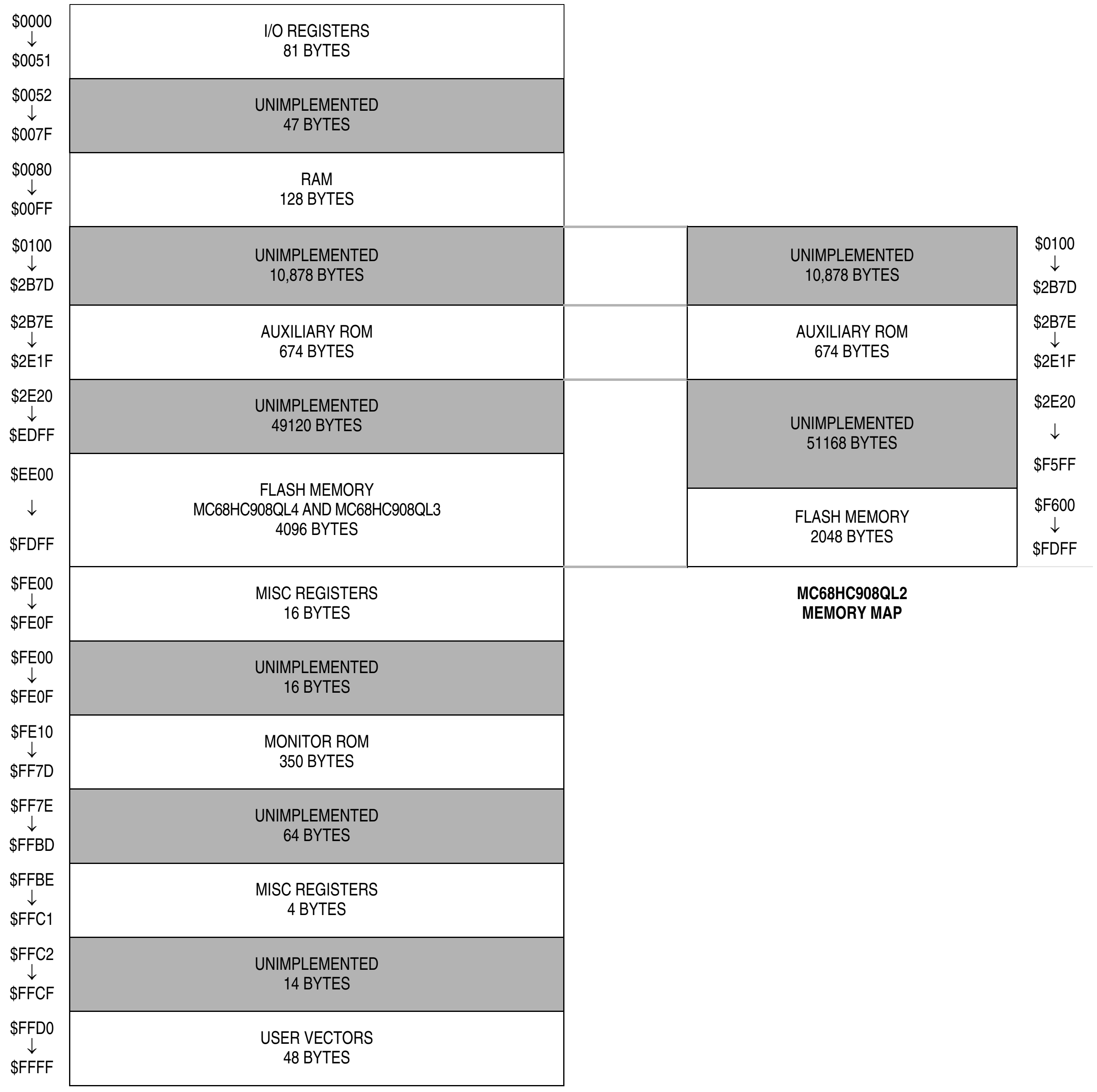


Figure 2-1. Memory Map

2.4 Input/Output (I/O) Section

Addresses $0000–$0051, shown in **Figure 2-2**, contain most of the control, status, and data registers. Additional miscellaneous registers have these addresses:

- $FE00 — Break status register, BSR
- $FE01 — Reset status register, SRSR
- $FE02 — Break auxiliary register, BRKAR
- $FE03 — Break flag control register, BFCR
- $FE04 — Interrupt status register 1, INT1
- $FE05 — Interrupt status register 2, INT2
- $FE06 — Interrupt status register 3, INT3
- $FE07 — Reserved
- $FE08 — FLASH control register, FLCR
- $FE09 — Break address register high, BRKH
- $FE0A — Break address register low, BRKL
- $FE0B — Break status and control register, BRKSCR
- $FE0C — LVI status register, LVISR
- $FE0D–$FE0F — Reserved
- $FFBE — FLASH block protect register, FLBPR
- $FFBF — Reserved
- $FFC0 — Internal OSC trim value — Optional
- $FFC1 — Reserved
- $FFFF — COP control register, COPCTL

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 114.	Read:	0	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:	▨	▨	PTA5	PTA4	PTA3	▨	PTA1	PTA0
		Reset:	U	0	U	U	U	U	U	U
$0001	Port B Data Register (PTB) See page 117.	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Reset:	Unaffected by reset							
$0002	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0003	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0004	Data Direction Register A (DDRA) See page 115.	Read:	0	0	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
		Write:	▨	▨	DDRA5	DDRA4	DDRA3	▨	DDRA1	DDRA0
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 117.	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Reset:	0	0	0	0	0	0	0	0
$0006 ↓ $000A	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$000B	Port A Input Pullup Enable Register (PTAPUE) See page 116.	Read:	OSC2EN	0	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:	OSC2EN	▨	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Reset:	0	0	0	0	0	0	0	0
$000C	Port B Input Pullup Enable Register (PTBPUE) See page 119.	Read:	PTBPUE7	PTBPUE6	PTBPUE5	PTBPUE4	PTBPUE3	PTBPUE2	PTBPUE1	PTBPUE0
		Write:	PTBPUE7	PTBPUE6	PTBPUE5	PTBPUE4	PTBPUE3	PTBPUE2	PTBPUE1	PTBPUE0
		Reset:	0	0	0	0	0	0	0	0
$000D ↓ $0019	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$001A	Keyboard Status and Control Register (KBSCR) See page 96.	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:	▨	▨	▨	▨	▨	ACKK	IMASKK	MODEK
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (KBIER) See page 97.	Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:	▨	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Reset:	0	0	0	0	0	0	0	0
$001C	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨

▨ = Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 7)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001D	IRQ Status and Control Register (INTSCR) See page 89.	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:	▨	▨	▨	▨	▨	ACK		
		Reset:	0	0	0	0	0	0	0	0
$001E	Configuration Register 2 (CONFIG2)(1) See page 64.	Read:	R	R	R	OSCOPT1	OSCOPT0	IRQPUD	IRQEN	RSTEN
		Write:								
		Reset:	0	0	0	0	0	0	0	0(2)

1. One-time writable register after each reset.
2. RSTEN reset to 0 by a power-on reset (POR) only.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001F	Configuration Register 1 (CONFIG1)(1) See page 64.	Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVI5OR3	SSREC	STOP	COPD
		Write:								
		Reset:	0	0	0	0	0(2)	0	0	0

1. One-time writable register after each reset.
2. LVI5OR3 reset to 0 by a power-on reset (POR) only.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0020	TIM Status and Control Register (TSC) See page 197.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST	▨			
		Reset:	0	0	1	0	0	0	0	0
$0021	TIM Counter Register High (TCNTH) See page 199.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$0022	TIM Counter Register Low (TCNTL) See page 199.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$0023	TIM Counter Modulo Register High (TMODH) See page 199.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0024	TIM Counter Modulo Register Low (TMODL) See page 199.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0025	TIM Channel 0 Status and Control Register (TSC0) See page 200.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	TIM Channel 0 Register High (TCH0H) See page 203.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							

▨ = Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 2 of 7)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0027	TIM Channel 0 Register Low (TCH0L) See page 203.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$0028	TIM Channel 1 Status and Control Register (TSC1) See page 200.	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0		▨					
		Reset:	0	0	0	0	0	0	0	0
$0029	TIM Channel 1 Register High (TCH1H) See page 203.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$002A	TIM Channel 1 Register Low (TCH1L) See page 203.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$002B ↓ $0035	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0036	Oscillator Status and Control Register (OSCSTAT) See page 111.	Read:	R	R	R	R	R	BFS	ECGON	ECGST
		Write:								▨
		Reset:	0	0	0	0	0	0	0	0
$0037	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0038	Oscillator Trim Register (OSCTRIM) See page 112.	Read:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
		Write:								
		Reset:	1	0	0	0	0	0	0	0
$0039 ↓ $003B	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$003C	ADC Status and Control Register (ADSCR) See page 52.	Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
		Write:								
		Reset:	0	0	0	1	1	1	1	1
$003D	ADC Data High Register (ADRH) See page 53.	Read:	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	Unaffected by reset							
$003E	ADC Data Low Register (ADRL) See page 53.	Read:	AD1	AD0	0	0	0	0	0	0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	Unaffected by reset							

▨ = Unimplemented   R = Reserved   U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 7)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003F	ADC Clock Register (ADCLK) See page 55.	Read:	ADIV2	ADIV1	ADIV0	ADICLK	MODE1	MODE0	R	0
		Write:	ADIV2	ADIV1	ADIV0	ADICLK	MODE1	MODE0	R	▨
		Reset:	0	0	0	0	0	1	0	0
$0040	SLIC Control Register 1 (SLCC1) See page 147.	Read:	0	0	INITREQ	0	WAKETX	TXABRT	IMSG	SLCIE
		Write:	▨	▨	INITREQ	▨	WAKETX	TXABRT	IMSG	SLCIE
		Reset:	0	0	1	0	0	0	0	0
$0041	SLIC Control Register 2 (SLCC2) See page 148.	Read:	0	0	0	0	SLCWCM	BTM	0	SLCE
		Write:	▨	▨	▨	▨	SLCWCM	BTM	▨	SLCE
		Reset:	0	0	0	0	0	0	0	0
$0042	SLIC Status Register (SLCS) See page 149.	Read:	SLCACT	0	INITACK	0	0	0	0	SLCF
		Write:	▨	▨	▨	▨	▨	▨	▨	SLCF
		Reset:	0	0	1	0	0	0	0	0
$0043	SLIC Prescale Register (SLCP) See page 150.	Read:	RXFP1	RXFP0	0	0	0	0	0	0
		Write:	RXFP1	RXFP0	▨	▨	▨	▨	▨	▨
		Reset:	1	0	0	0	0	0	0	0
$0044	SLIC Bit Time Register High (SLCBTH) See page 152.	Read:	0	0	0	BT12	BT11	BT10	BT9	BT8
		Write:	▨	▨	▨	BT12	BT11	BT10	BT9	BT8
		Reset:	0	0	0	0	0	0	0	0
$0045	SLIC Bit Time Register Low (SLCBTL) See page 152.	Read:	BT7	BT6	BT5	BT4	BT3	BT2	BT1	0
		Write:	BT7	BT6	BT5	BT4	BT3	BT2	BT1	▨
		Reset:	0	0	0	0	0	0	0	0
$0046	SLIC State Vector Register (SLCSV) See page 152.	Read:	0	0	I3	I2	I1	I0	0	0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$0047	SLIC Data Length Code Register (SLCDLC) See page 157.	Read:	TXGO	CHKMOD	DLC5	DLC4	DLC3	DLC2	DLC1	DLC0
		Write:	TXGO	CHKMOD	DLC5	DLC4	DLC3	DLC2	DLC1	DLC0
		Reset:	0	0	0	0	0	0	0	0
$0048	SLIC Identifier Register (SLCID) See page 158.	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0
		Reset:	0	0	0	0	0	0	0	0
$0049	SLIC Data Register 7 (SLCD7) See page 159.	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0
		Reset:	0	0	0	0	0	0	0	0
$004A	SLIC Data Register 6 (SLCD6) See page 159.	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 7)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
	SLIC Data Register 5	Read:	R7	R6	R5	R4	R3	R2	R1	R0
$004B	(SLCD5)	Write:	T7	T6	T5	T4	T3	T2	T1	T0
	See page 159.	Reset:	0	0	0	0	0	0	0	0
	SLIC Data Register 4	Read:	R7	R6	R5	R4	R3	R2	R1	R0
$004C	(SLCD4)	Write:	T7	T6	T5	T4	T3	T2	T1	T0
	See page 159.	Reset:	0	0	0	0	0	0	0	0
	SLIC Data Register 3	Read:	R7	R6	R5	R4	R3	R2	R1	R0
$004D	(SLCD3)	Write:	T7	T6	T5	T4	T3	T2	T1	T0
	See page 159.	Reset:	0	0	0	0	0	0	0	0
	SLIC Data Register 2	Read:	R7	R6	R5	R4	R3	R2	R1	R0
$004E	(SLCD2)	Write:	T7	T6	T5	T4	T3	T2	T1	T0
	See page 159.	Reset:	0	0	0	0	0	0	0	0
	SLIC Data Register 1	Read:	R7	R6	R5	R4	R3	R2	R1	R0
$004F	(SLCD1)	Write:	T7	T6	T5	T4	T3	T2	T1	T0
	See page 160.	Reset:	0	0	0	0	0	0	0	0
	SLIC Data Register 0	Read:	R7	R6	R5	R4	R3	R2	R1	R0
$0050	(SLCD0)	Write:	T7	T6	T5	T4	T3	T2	T1	T0
	See page 160.	Reset:	0	0	0	0	0	0	0	0
$0051 ↓ $005F	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
	Break Status Register	Read:	R	R	R	R	R	R	SBSW	R
$FE00	(BSR)	Write:							See note 1	
	See page 210.	Reset:							0	
	SIM Reset Status Register	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
$FE01	(SRSR)	Write:	▨	▨	▨	▨	▨	▨	▨	▨
	See page 137.	POR:	1	0	0	0	0	0	0	0
	Break Auxiliary	Read:	0	0	0	0	0	0	0	BDCOP
$FE02	Register (BRKAR)	Write:	▨	▨	▨	▨	▨	▨	▨	
	See page 209.	Reset:	0	0	0	0	0	0	0	0
	Break Flag Control	Read:	BCFE	R	R	R	R	R	R	R
$FE03	Register (BFCR)	Write:								
	See page 210.	Reset:	0							

1. Writing a 0 clears SBSW.

▨ = Unimplemented   R = Reserved   U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 5 of 7)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE04	Interrupt Status Register 1 (INT1) See page 89.	Read:	0	IF5	IF4	IF3	0	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE05	Interrupt Status Register 2 (INT2) See page 89.	Read:	IF14	0	0	IF11	IF10	IF9	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE06	Interrupt Status Register 3 (INT3) See page 89.	Read:	0	0	0	0	0	0	0	IF15
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE07	Reserved		R	R	R	R	R	R	R	R
$FE08	FLASH Control Register (FLCR) See page 37.	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:	▨	▨	▨	▨				
		Reset:	0	0	0	0	0	0	0	0
$FE09	Break Address High Register (BRKH) See page 209.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0A	Break Address low Register (BRKL) See page 209.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0B	Break Status and Control Register (BRKSCR) See page 208.	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:			▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$FE0C	LVI Status Register (LVISR) See page 101.	Read:	LVIOUT	0	0	0	0	0	0	R
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$FE0D ↓ $FE0F	Reserved for FLASH Test		R	R	R	R	R	R	R	R
$FFB0 ↓ $FFBD	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$FFBE	FLASH Block Protect Register (FLBPR) See page 43.	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	0
		Write:								▨
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 6 of 7)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FFBF	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$FFC0	Internal Oscillator Trim Value (Optional)	Read: Write:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
		Reset:	1	0	0	0	0	0	0	0
$FFC1	Reserved		R	R	R	R	R	R	R	R
$FFC2 ↓ $FFCF	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$FFFF	COP Control Register (COPCTL) See page 69.	Read:	LOW BYTE OF RESET VECTOR							
		Write:	WRITING CLEARS COP COUNTER (ANY VALUE)							
		Reset:	Unaffected by reset							

▨ = Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 7 of 7)

Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
Lowest	IF15	$FFDE	ADC conversion complete vector (high)
↑		$FFDF	ADC conversion complete vector (low)
	IF14	$FFE0	Keyboard vector (high)
		$FFE1	Keyboard vector (low)
	IF13 ↓ IF10	—	Not used
	IF9	$FFEA	SLIC vector (high)
		$FFEB	SLIC vector (low)
	IF8 ↓ IF6	—	Not used
	IF5	$FFF2	TIM overflow vector (high)
		$FFF3	TIM overflow vector (low)
	IF4	$FFF4	TIM channel 1 vector (high)
		$FFF5	TIM channel 1 vector (low)
	IF3	$FFF6	TIM channel 0 vector (high)
		$FFF7	TIM channel 0 vector (low)
	IF2	—	Not used
	IF1	$FFFA	$\overline{\text{IRQ}}$ vector (high)
		$FFFB	$\overline{\text{IRQ}}$ vector (low)
	—	$FFFC	SWI vector (high)
		$FFFD	SWI vector (low)
↓	—	$FFFE	Reset vector (high)
Highest		$FFFF	Reset vector (low)

2.5 Random-Access Memory (RAM)

Addresses $0080–$00FF are RAM locations. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64-Kbyte memory space.

NOTE: *For correct operation, the stack pointer must point only to RAM locations.*

Before processing an interrupt, the central processor unit (CPU) uses five bytes of the stack to save the contents of the CPU registers.

NOTE: *For M6805, M146805, and M68HC05 compatibility, the H register is not stacked.*

During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

NOTE: *Be careful when using nested subroutines. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.*

2.6 FLASH Memory (FLASH)

The FLASH memory consists of an array of 4096 or 2048 bytes with an additional 48 bytes for user vectors. The minimum size of FLASH memory that can be erased is 64 bytes; and the maximum size of FLASH memory that can be programmed in a program cycle is 32 bytes (a row). Program and erase operations are facilitated through control bits in the FLASH control register (FLCR). Details for these operations appear later in this section. The address ranges for the user memory and vectors are:

- $EE00 – $FDFF; user memory, 4096 bytes: MC68HC908QL4 and MC68HC908QL3
- $F600 – $FDFF; user memory, 2048 bytes: MC68HC908QL2
- $FFD0 – $FFFF; user interrupt vectors, 48 bytes.

NOTE: *An erased bit reads as 1 and a programmed bit reads as 0. A security feature prevents viewing of the FLASH contents.*[1]

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

2.6.1 FLASH Control Register

The FLASH control register (FLCR) controls FLASH program and erase operations.

Address: $FE08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
Write:	▨	▨	▨	▨				
Reset:	0	0	0	0	0	0	0	0

Figure 2-3. FLASH Control Register (FLCR)

HVEN — High Voltage Enable Bit

This read/write bit enables high voltage from the charge pump to the memory for either program or erase operation. It can only be set if either PGM =1 or ERASE =1 and the proper sequence for program or erase is followed.

1 = High voltage enabled to array and charge pump on
0 = High voltage disabled to array and charge pump off

MASS — Mass Erase Control Bit

This read/write bit configures the memory for mass erase operation.

1 = Mass Erase operation selected
0 = Mass Erase operation unselected

ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation. ERASE is interlocked with the PGM bit such that both bits cannot be equal to 1 or set to 1 at the same time.

1 = Erase operation selected
0 = Erase operation unselected

PGM — Program Control Bit

This read/write bit configures the memory for program operation. PGM is interlocked with the ERASE bit such that both bits cannot be equal to 1 or set to 1 at the same time.

1 = Program operation selected
0 = Program operation unselected

2.6.2 FLASH Page Erase Operation

Use the following procedure to erase a page of FLASH memory. A page consists of 64 consecutive bytes starting from addresses $XX00, $XX40, $XX80, or $XXC0. The 48-byte user interrupt vectors area also forms a page. Any FLASH memory page can be erased alone.

1. Set the ERASE bit and clear the MASS bit in the FLASH control register.
2. Read the FLASH block protect register.
3. Write any data to any FLASH location within the address range of the block to be erased.
4. Wait for a time, t_{NVS} (minimum 10 μs).
5. Set the HVEN bit.
6. Wait for a time, t_{Erase} (minimum 1 ms or 4 ms).
7. Clear the ERASE bit.
8. Wait for a time, t_{NVH} (minimum 5 μs).
9. Clear the HVEN bit.
10. After time, t_{RCV} (typical 1 μs), the memory can be accessed in read mode again.

NOTE: *Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.*

CAUTION: *A page erase of the vector page will erase the internal oscillator trim value at $FFC0.*

In applications that require more than 1000 program/erase cycles, use the 4 ms page erase specification to get improved long-term reliability. Any application can use this 4 ms page erase specification. However, in applications where a FLASH location will be erased and reprogrammed less than 1000 times, and speed is important, use the 1 ms page erase specification to get a shorter cycle time.

2.6.3 FLASH Mass Erase Operation

Use the following procedure to erase the entire FLASH memory to read as 1:

1. Set both the ERASE bit and the MASS bit in the FLASH control register.
2. Read from the FLASH block protect register.
3. Write any data to any FLASH address(1) within the FLASH memory address range.
4. Wait for a time, t_{NVS} (minimum 10 μs).
5. Set the HVEN bit.
6. Wait for a time, t_{Erase} (minimum 4 ms).
7. Clear the ERASE and MASS bits.

NOTE: *Mass erase is disabled whenever any block is protected (FLBPR does not equal $FF).*

8. Wait for a time, t_{NVH} (minimum 100 μs).
9. Clear the HVEN bit.
10. After time, t_{RCV} (typical 1 μs), the memory can be accessed in read mode again.

NOTE: *Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order as shown, but other unrelated operations may occur between the steps.*

CAUTION: *A mass erase will erase the internal oscillator trim value at $FFC0.*

1. When in monitor mode, with security sequence failed (see **16.3.2 Security**), write to the FLASH block protect register instead of any FLASH address.

2.6.4 FLASH Program Operation

Programming of the FLASH memory is done on a row basis. A row consists of 32 consecutive bytes starting from addresses $XX00, $XX20, $XX40, $XX60, $XX80, $XXA0, $XXC0, or $XXE0. Use the following step-by-step procedure to program a row of FLASH memory

Figure 2-4 shows a flowchart of the programming algorithm.

NOTE: *Only bytes which are currently $FF may be programmed.*

1. Set the PGM bit. This configures the memory for program operation and enables the latching of address and data for programming.
2. Read from the FLASH block protect register.
3. Write any data to any FLASH location within the address range desired.
4. Wait for a time, t_{NVS} (minimum 10 μs).
5. Set the HVEN bit.
6. Wait for a time, t_{PGS} (minimum 5 μs).
7. Write data to the FLASH address being programmed(1).
8. Wait for time, t_{PROG} (minimum 30 μs).
9. Repeat step 7 and 8 until all desired bytes within the row are programmed.
10. Clear the PGM bit(1).
11. Wait for time, t_{NVH} (minimum 5 μs).
12. Clear the HVEN bit.
13. After time, t_{RCV} (typical 1 μs), the memory can be accessed in read mode again.

NOTE: *The COP register at location $FFFF should not be written between steps 5–12, when the HVEN bit is set. Since this register is located at a valid FLASH address, unpredictable behavior may occur if this location is written while HVEN is set.*

This program sequence is repeated throughout the memory until all data is programmed.

NOTE: *Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps. Do not exceed t_{PROG} maximum, see **17.16 Memory Characteristics**.*

1. The time between each FLASH address change, or the time between the last FLASH address programmed to clearing PGM bit, must not exceed the maximum programming time, t_{PROG} maximum.

2.6.5 FLASH Protection

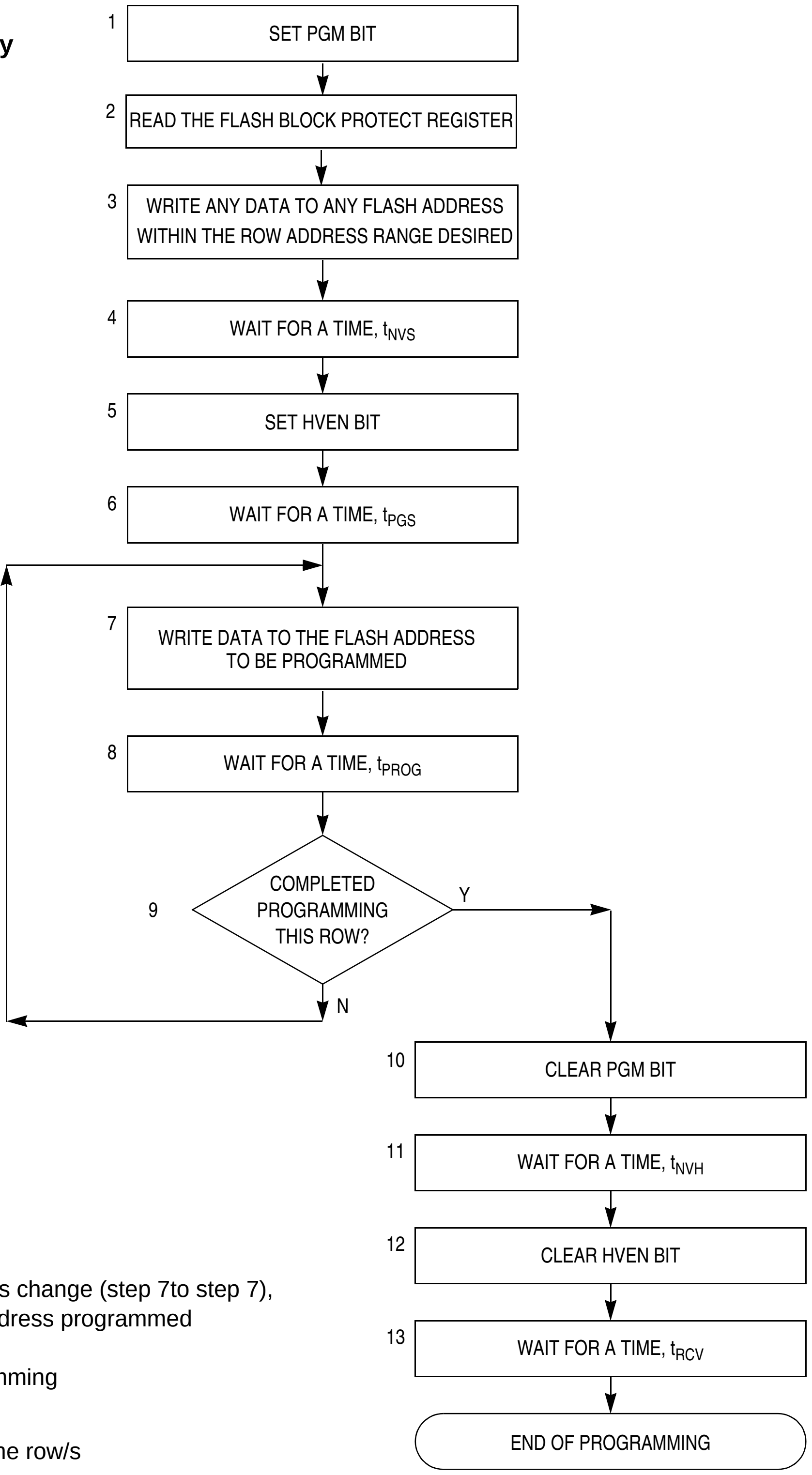
Due to the ability of the on-board charge pump to erase and program the FLASH memory in the target application, provision is made to protect blocks of memory from unintentional erase or program operations due to system malfunction. This protection is done by use of a FLASH block protect register (FLBPR). The FLBPR determines the range of the FLASH memory which is to be protected. The range of the protected area starts from a location defined by FLBPR and ends to the bottom of the FLASH memory ($FFFF). When the memory is protected, the HVEN bit cannot be set in either ERASE or PROGRAM operations.

NOTE: *In performing a program or erase operation, the FLASH block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit.*

When the FLBPR is programmed with all 0s, the entire memory is protected from being programmed and erased. When all the bits are erased (all 1s), the entire memory is accessible for program and erase.

When bits within the FLBPR are programmed, they lock a block of memory. The address ranges are shown in **2.6.6 FLASH Block Protect Register**. Once the FLBPR is programmed with a value other than $FF, any erase or program of the FLBPR or the protected block of FLASH memory is prohibited. Mass erase is disabled whenever any block is protected (FLBPR does not equal $FF). The FLBPR itself can be erased or programmed only with an external voltage, V_{TST}, present on the $\overline{IRQ}$ pin. This voltage also allows entry from reset into the monitor mode.

Algorithm for Programming a Row (32 Bytes) of FLASH Memory


1
SET PGM BIT
2
READ THE FLASH BLOCK PROTECT REGISTER
3
WRITE ANY DATA TO ANY FLASH ADDRESS WITHIN THE ROW ADDRESS RANGE DESIRED
4
WAIT FOR A TIME, t_{NVS}
5
SET HVEN BIT
6
WAIT FOR A TIME, t_{PGS}
7
WRITE DATA TO THE FLASH ADDRESS TO BE PROGRAMMED
8
WAIT FOR A TIME, t_{PROG}
9
COMPLETED PROGRAMMING THIS ROW?
Y
N
10
CLEAR PGM BIT
11
WAIT FOR A TIME, t_{NVH}
12
CLEAR HVEN BIT
13
WAIT FOR A TIME, t_{RCV}
END OF PROGRAMMING

NOTES:

The time between each FLASH address change (step 7to step 7), or the time between the last FLASH address programmed to clearing PGM bit (step 6 to step 10) must not exceed the maximum programming time, t_{PROG} max.

This row program algorithm assumes the row/s to be programmed are initially erased.

Figure 2-4. FLASH Programming Flowchart

2.6.6 FLASH Block Protect Register

The FLASH block protect register is implemented as a byte within the FLASH memory, and therefore can only be written during a programming sequence of the FLASH memory. The value in this register determines the starting address of the protected range within the FLASH memory.

Address: $FFBE

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Reset:	U	U	U	U	U	U	U	U

U = Unaffected by reset. Initial value from factory is 1.
Write to this register is by a programming sequence to the FLASH memory.

Figure 2-5. FLASH Block Protect Register (FLBPR)

BPR[7:0] — FLASH Protection Register Bits [7:0]

These eight bits in FLBPR represent bits [13:6] of a 16-bit memory address. Bits [15:14] are 1s and bits [5:0] are 0s.

The resultant 16-bit address is used for specifying the start address of the FLASH memory for block protection. The FLASH is protected from this start address to the end of FLASH memory, at $FFFF. With this mechanism, the protect start address can be XX00, XX40, XX80, or XXC0 within the FLASH memory. See **Figure 2-6** and **Table 2-2**.

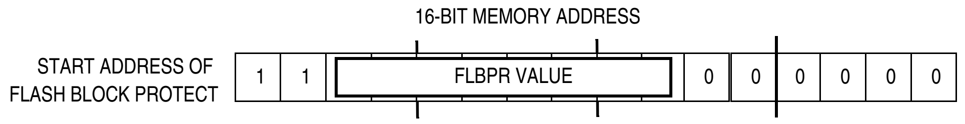


Figure 2-6. FLASH Block Protect Start Address

Table 2-2. Examples of Protect Start Address

BPR[7:0]	**Start of Address of Protect Range**
$00–$B8	The entire FLASH memory is protected.
$B9 (**1011 1001**)	$EE40 (11**10 1110 01**00 0000)
$BA (**1011 1010**)	$EE80 (11**10 1110 10**00 0000)
$BB (**1011 1011**)	$EEC0 (11**10 1110 11**00 0000)
$BC (**1011 1100**)	$EF00 (11**10 1111 00**00 0000)
and so on...	
$DE (**1101 1110**)	$F780 (11**11 0111 10**00 0000)
$DF (**1101 1111**)	$F7C0 (11**11 0111 11**00 0000)
$FE (**1111 1110**)	$FF80 (11**11 1111 10**00 0000) FLBPR, OSCTRIM, and vectors are protected
$FF	The entire FLASH memory is not protected.

2.6.7 Wait Mode

Putting the MCU into wait mode while the FLASH is in read mode does not affect the operation of the FLASH memory directly, but there will not be any memory activity since the CPU is inactive.

The WAIT instruction should not be executed while performing a program or erase operation on the FLASH, or the operation will discontinue and the FLASH will be on standby mode.

2.6.8 Stop Mode

Putting the MCU into stop mode while the FLASH is in read mode does not affect the operation of the FLASH memory directly, but there will not be any memory activity since the CPU is inactive.

The STOP instruction should not be executed while performing a program or erase operation on the FLASH, or the operation will discontinue and the FLASH will be on standby mode

NOTE: *Standby mode is the power-saving mode of the FLASH module in which all internal control signals to the FLASH are inactive and the current consumption of the FLASH is at a minimum.*

Section 3. Analog-to-Digital Converter (ADC)

3.1 Introduction

This section describes the 10-bit analog-to-digital converter (ADC).

3.2 Features

Features of the ADC module include:

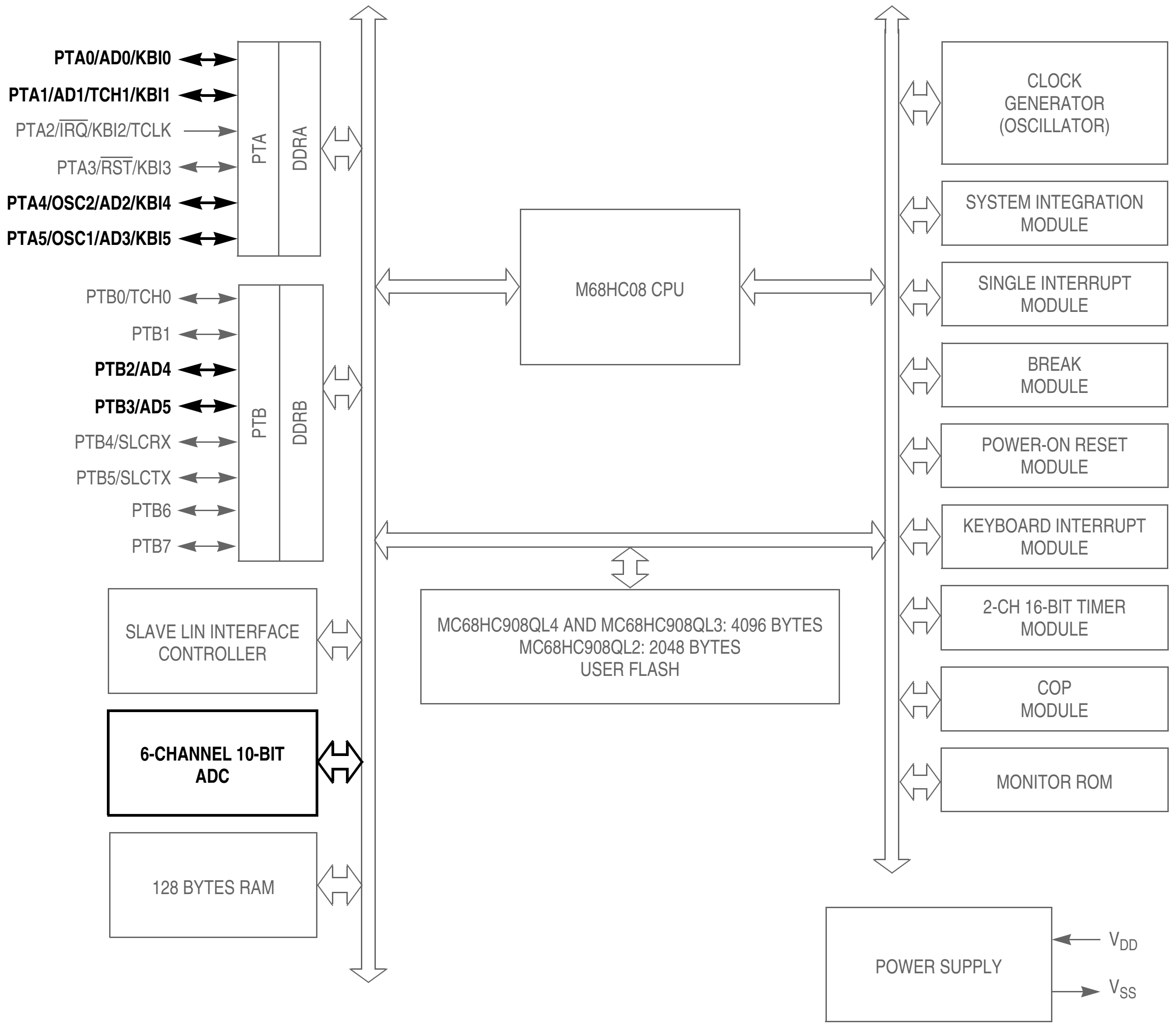
- Six channels with multiplexed input
- Linear successive approximation with monotonicity
- 10-bit resolution
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock
- Left or right justified result
- Left justified sign data mode

3.3 Functional Description

The ADC provides six pins for sampling external sources. An analog multiplexer allows the single ADC converter to select one of the ADC channels as ADC voltage in (V_{ADIN}). V_{ADIN} is converted by the successive approximation register-based analog-to-digital converter. When the conversion is completed, ADC places the result in the ADC data register and sets a flag or generates an interrupt. See **Figure 3-2**.

3.3.1 ADC Port I/O Pins

PTA0, PTA1, PTA4, PTA5, PTB2, and PTB3 are general-purpose I/O (input/output) pins that share with the ADC channels. The channel select bits define which ADC channel/port pin will be used as the input signal. The ADC overrides the port I/O logic by forcing that pin as input to the ADC. The remaining ADC channels/port pins are controlled by the port I/O logic and can be used as general-purpose I/O. Writes to the port register or data direction register (DDR) will not have any affect on the port pin that is selected by the ADC. Read of a port pin in use by the ADC will return a logic 0.



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30 kΩ) pull up
PTA0, PTA1, PTA3–PTA5: High current sink and source capability
PTA0–PTA5: Pins have programmable keyboard interrupt and pull up
ADC pins only available on MC68HC908QL4 and MC68HC908QL2

Figure 3-1. Block Diagram Highlighting ADC Block and Pins

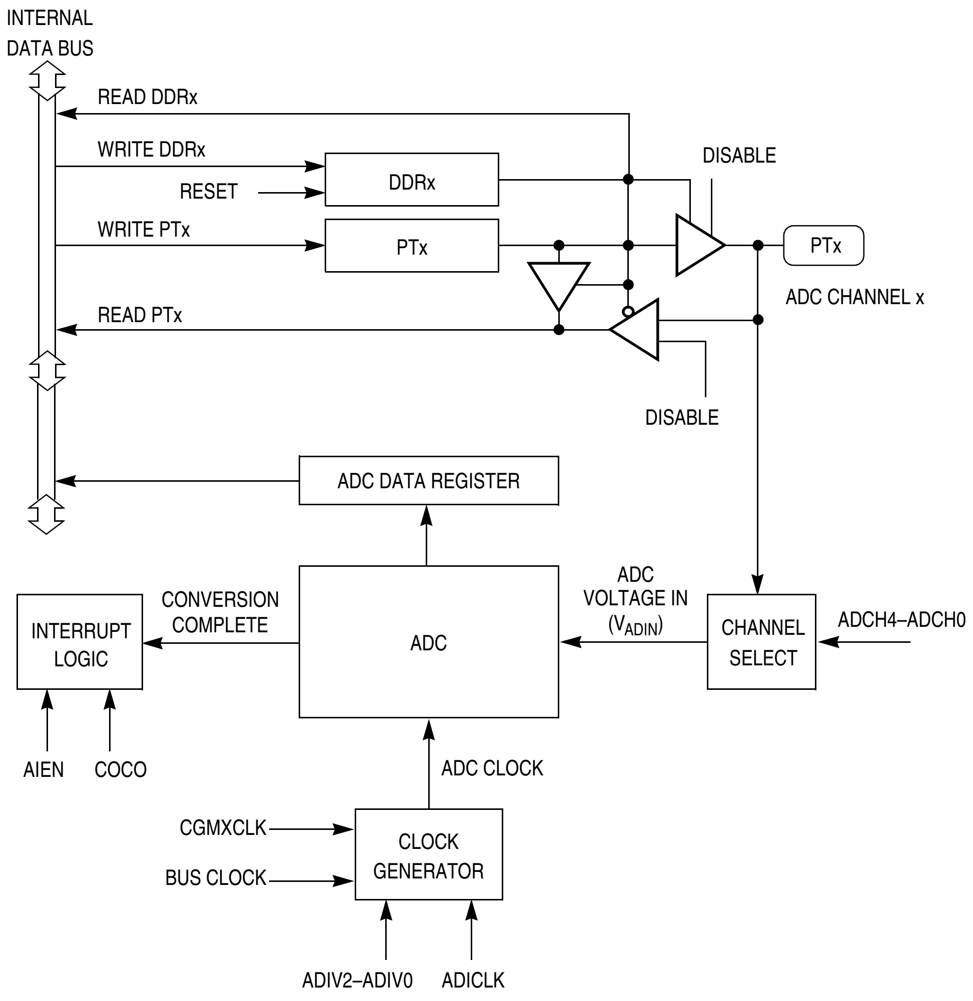


Figure 3-2. ADC Block Diagram

3.3.2 Voltage Conversion

When the input voltage to the ADC equals V_{REFH}, the ADC converts the signal to \$3FF (full scale). If the input voltage equals V_{REFL}, the ADC converts it to \$000. Input voltages between V_{REFH} and V_{REFL} are a straight-line linear conversion.

NOTE: *The ADC input voltage must always be greater than V_{SSA} and less than V_{DDA}. V_{REFH} must always be greater than or equal to V_{REFL}.*

Connect the V_{DDA} pin to the same voltage potential as the V_{DD} pin, and connect the V_{SSA} pin to the same voltage potential as the V_{SS} pin.

The V_{DDA} pin should be routed carefully for maximum noise immunity.

3.3.3 Conversion Time

Conversion starts after a write to the ADC status and control register (ADSCR). One conversion will take between 16 and 17 ADC clock cycles. The ADIVx and ADICLK bits should be set to provide a 1-MHz ADC clock frequency.

$$\text{Conversion time} = \frac{\text{16 to 17 ADC cycles}}{\text{ADC frequency}}$$

$$\text{Number of bus cycles} = \text{conversion time} \times \text{bus frequency}$$

3.3.4 Conversion

In continuous conversion mode, the ADC data register will be filled with new data after each conversion. Data from the previous conversion will be overwritten whether that data has been read or not. Conversions will continue until the ADCO bit is cleared. The COCO bit is set after each conversion and will stay set until the next write of the ADC status and control register or the next read of the ADC data register.

In single conversion mode, conversion begins with a write to the ADSCR. Only one conversion occurs between writes to the ADSCR.

3.3.5 Accuracy and Precision

The conversion process is monotonic and has no missing codes.

3.3.6 Result Justification

The conversion result may be formatted in four different ways:

1. Left justified
2. Right justified
3. Left Justified sign data mode
4. 8-bit truncation mode

All four of these modes are controlled using MODE0 and MODE1 bits located in the ADC clock register (ADCLK).

Left justification will place the eight most significant bits (MSB) in the corresponding ADC data register high, ADRH. This may be useful if the result is to be treated as an 8-bit result where the two least significant bits (LSB), located in the ADC data register low, ADRL, can be ignored. However, ADRL must be read after ADRH or else the interlocking will prevent all new conversions from being stored.

Right justification will place only the two MSBs in the corresponding ADC data register high, ADRH, and the eight LSBs in ADC data register low, ADRL. This mode of operation typically is used when a 10-bit unsigned result is desired.

Left justified sign data mode is similar to left justified mode with one exception. The MSB of the 10-bit result, AD9 located in ADRH, is complemented. This mode of operation is useful when a result, represented as a signed magnitude from mid-scale, is needed. Finally, 8-bit truncation mode will place the eight MSBs in the ADC data register low, ADRL. The two LSBs are dropped. This mode of operation is used when compatibility with 8-bit ADC designs are required. No interlocking between ADRH and ADRL is present.

NOTE: *Quantization error is affected when only the most significant eight bits are used as a result. See **Figure 3-3**.*

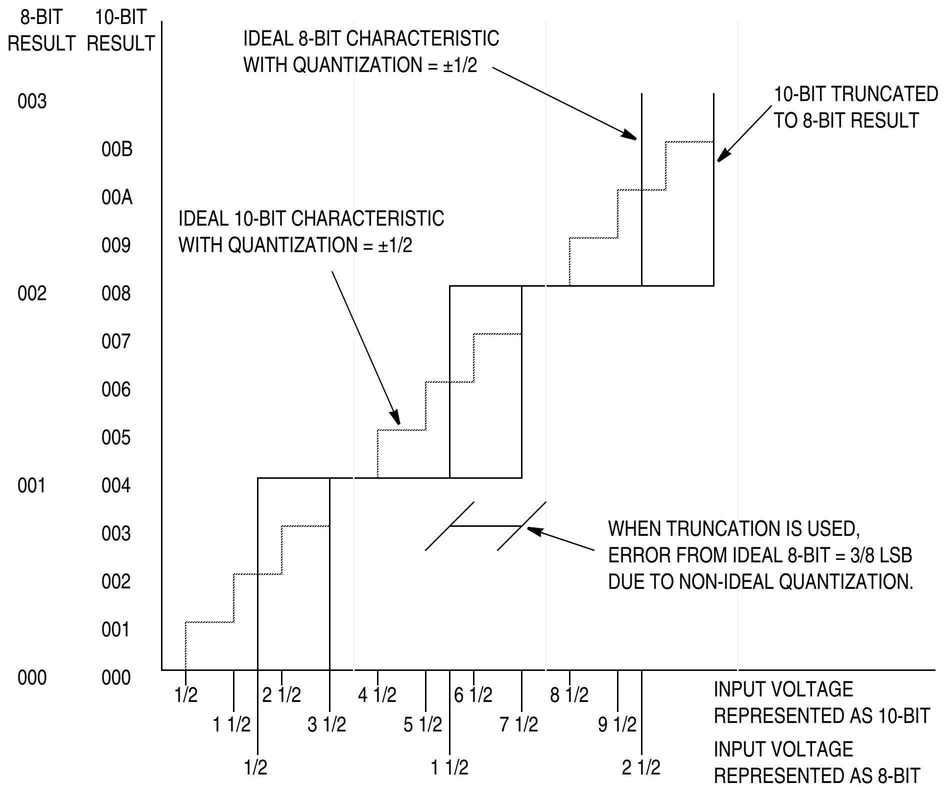

8-BIT RESULT
10-BIT RESULT
003
00B
00A
009
002 008
007
006
005
001 004
003
002
001
000 000
IDEAL 8-BIT CHARACTERISTIC WITH QUANTIZATION = ±1/2
10-BIT TRUNCATED TO 8-BIT RESULT
IDEAL 10-BIT CHARACTERISTIC WITH QUANTIZATION = ±1/2
WHEN TRUNCATION IS USED, ERROR FROM IDEAL 8-BIT = 3/8 LSB DUE TO NON-IDEAL QUANTIZATION.
1/2
1 1/2
2 1/2
3 1/2
4 1/2
5 1/2
6 1/2
7 1/2
8 1/2
9 1/2
INPUT VOLTAGE REPRESENTED AS 10-BIT
1/2
1 1/2
2 1/2
INPUT VOLTAGE REPRESENTED AS 8-BIT

Figure 3-3. Bit Truncation Mode Error

3.4 Monotonicity

The conversion process is monotonic and has no missing codes.

3.5 Interrupts

When the AIEN bit is set, the ADC module is capable of generating CPU interrupts after each ADC conversion. A CPU interrupt is generated if the COCO bit is at 0. The COCO bit is not used as a conversion complete flag when interrupts are enabled.

3.6 Low-Power Modes

The WAIT and STOP instruction can put the MCU in low power-consumption standby modes.

3.6.1 Wait Mode

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting ADCH4–ADCH0 bits in the ADC status and control register before executing the WAIT instruction.

3.6.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode after an external interrupt. Allow one conversion cycle to stabilize the analog circuitry.

3.7 I/O Signals

The ADC module has six pins shared with I/O pins on port A and port B.

3.7.1 ADC Analog Power Pin (V_{DDAD})

The ADC analog portion uses V_{DDAD} as its power pin and is internally connected to the V_{DD} pad. External filtering may be necessary to ensure clean V_{DD} for good results.

NOTE: *For maximum noise immunity, route V_{DD} carefully and place bypass capacitors as close as possible to the package.*

V_{DD} and V_{DDA} use the same pad on the MC68HC908QL4.

3.7.2 ADC Analog Ground Pin (V_{SSAD})

The ADC analog portion uses V_{SSAD} as its ground pin and is internally connected to the V_{SSAD} pad.

NOTE: *Route V_{SS} cleanly to avoid any offset errors.*

V_{DD} and V_{DDA} use the same pad on the MC68HC908QL4.

3.7.3 ADC Voltage Reference High Pin (V_{REFH})

The ADC analog portion uses V_{REFH} as its upper voltage reference pin. By default, connect the V_{REFH} pin to the same voltage potential as V_{DD}. External filtering is often necessary to ensure a clean V_{REFH} for good results. Any noise present on this pin will be reflected and possibly magnified in A/D conversion values.

NOTE: *For maximum noise immunity, route V_{REFH} carefully and place bypass capacitors as close as possible to the package. Routing V_{REFH} close and parallel to V_{REFL} may improve common mode noise rejection.*

V_{DD} and V_{REFH} are connected on the MC68HC908QL4.

3.7.4 ADC Voltage Reference Low Pin (V_{REFL})

The ADC analog portion uses V_{REFL} as its lower voltage reference pin. By default, connect the V_{REFL} pin to the same voltage potential as V_{SS}. External filtering is often necessary to ensure a clean V_{REFL} for good results. Any noise present on this pin will be reflected and possibly magnified in A/D conversion values.

NOTE: *For maximum noise immunity, route V_{REFL} carefully and, if not connected to V_{SS}, place bypass capacitors as close as possible to the package. Routing V_{REFH} close and parallel to V_{REFL} may improve common mode noise rejection.*

V_{SS} and V_{REFL} are connected on the MC68HC908QL4.

3.7.5 ADC Voltage In (V_{ADIN})

V_{ADIN} is the input voltage signal from one of the ADC channels to the ADC module.

3.8 I/O Registers

These I/O registers control and monitor ADC operation:

- ADC status and control register (ADSCR)
- ADC data register (ADRH and ADRL)
- ADC clock register (ADCLK)

3.8.1 ADC Status and Control Register

Function of the ADC status and control register (ADSCR) is described here.

Address: $003C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Reset:	0	0	0	1	1	1	1	1

Figure 3-4. ADC Status and Control Register (ADSCR)

COCO — Conversions Complete Bit

When the AIEN bit is 0, the COCO is a read-only bit which is set each time a conversion is completed except in the continuous conversion mode where it is set after the first conversion. This bit is cleared whenever the ADSCR is written or whenever the ADR is read.

If the AIEN bit is 1, the COCO becomes a read/write bit, which should be cleared to 0 for CPU to service the ADC interrupt request. Reset clears this bit.

1 = Conversion completed (AIEN = 0)
0 = Conversion not completed (AIEN = 0)/CPU interrupt (AIEN = 1)

AIEN — ADC Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of an ADC conversion. The interrupt signal is cleared when the data register is read or the status/control register is written. Reset clears the AIEN bit.

1 = ADC interrupt enabled
0 = ADC interrupt disabled

ADCO — ADC Continuous Conversion Bit

When set, the ADC will convert samples continuously and update the ADR register at the end of each conversion. Only one conversion is completed between writes to the ADSCR when this bit is cleared. Reset clears the ADCO bit.

1 = Continuous ADC conversion
0 = One ADC conversion

ADCH4–ADCH0 — ADC Channel Select Bits

ADCH4–ADCH0 form a 5-bit field which is used to select one of 16 ADC channels. Only eight channels, AD7–AD0, are available on this MCU. The channels are detailed in **Table 3-1**. Care should be taken when using a port pin as both an analog and digital input simultaneously to prevent switching noise from corrupting the analog signal.

The ADC subsystem is turned off when the channel select bits are all set to 1. This feature allows for reduced power consumption for the MCU when the ADC is not being used.

NOTE: *Recovery from the disabled state requires one conversion cycle to stabilize.*

The voltage levels supplied from internal reference nodes, as specified in **Table 3-1**, are used to verify the operation of the ADC converter both in production test and for user applications.

Table 3-1. Mux Channel Select[1]

ADCH4	ADCH3	ADCH2	ADCH1	ADCH0	Input Select
0	0	0	0	0	PTA0/AD0/KBI0
0	0	0	0	1	PTA1/AD1/KBI1
0	0	0	1	0	PTA4/OSC2/AD2/KBI2
0	0	0	1	1	PTA5/OSC1/AD3/KBI5
0	0	1	0	0	PTB2/AD4
0	0	1	0	1	PTB3/AD5
0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 0	0 ↓ 0	Unused
1	1	1	0	1	V_{DDA}
1	1	1	1	0	V_{SSA}
1	1	1	1	1	ADC power off

1. If any unused channels are selected, the resulting ADC conversion will be unknown or reserved.

3.8.2 ADC Data Register High and Data Register Low

3.8.2.1 Left Justified Mode

In left justified mode, the ADRH register holds the eight MSBs of the 10-bit result. The only difference from left justified mode is that the AD9 is complemented. The ADRL register holds the two LSBs of the 10-bit result. All other bits read as 0. ADRH and ADRL are updated each time an ADC single channel conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. All subsequent results will be lost until the ADRH and ADRL reads are completed.

Address:	$003D							ADRH
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							
Address:	$003E							ADRL
Read:	AD1	AD0	0	0	0	0	0	0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							

▨ = Unimplemented

Figure 3-5. ADC Data Register High (ADRH) and Low (ADRL)

3.8.2.2 Right Justified Mode

In right justified mode, the ADRH register holds the two MSBs of the 10-bit result. All other bits read as 0. The ADRL register holds the eight LSBs of the 10-bit result. ADRH and ADRL are updated each time an ADC single channel conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. All subsequent results will be lost until the ADRH and ADRL reads are completed.

Address:	$003D							ADRH
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	AD9	AD8
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							
Address:	$003E							ADRL
Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							

▨ = Unimplemented

Figure 3-6. ADC Data Register High (ADRH) and Low (ADRL)

3.8.2.3 Left Justified Signed Data Mode

In left justified signed data mode, the ADRH register holds the eight MSBs of the 10-bit result. The only difference from left justified mode is that the AD9 is complemented. The ADRL register holds the two LSBs of the 10-bit result. All other bits read as 0. ADRH and ADRL are updated each time an ADC single channel conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. All subsequent results will be lost until the ADRH and ADRL reads are completed.

Address:	$003D							ADRH
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	$\overline{\text{AD9}}$	AD8	AD7	AD6	AD5	AD4	AD3	AD2
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							
Address:	$003E							ADRL
Read:	AD1	AD0	0	0	0	0	0	0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							

▨ = Unimplemented

Figure 3-7. ADC Data Register High (ADRH) and Low (ADRL)

3.8.2.4 Eight Bit Truncation Mode

In 8-bit truncation mode, the ADRL register holds the eight MSBs of the 10-bit result. The ADRH register is unused and reads as 0. The ADRL register is updated each time an ADC single channel conversion completes. In 8-bit mode, the ADRL register contains no interlocking with ADRH.

Address:	$003D							ADRH
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							
Address:	$003E							ADRL
Read:	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	Unaffected by reset							

▨ = Unimplemented

Figure 3-8. ADC Data Register High (ADRH) and Low (ADRL)

3.8.3 ADC Clock Register

The ADC clock register (ADCLK) selects the clock frequency for the ADC.

Address:	$003F							
	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ADIV2	ADIV1	ADIV0	ADICLK	MODE1	MODE0	R	0
Write:								▨
Reset:	0	0	0	0	0	1	0	0

▨ = Unimplemented R = Reserved

Figure 3-9. ADC Clock Register (ADCLK)

ADIV2–ADIV0 — ADC Clock Prescaler Bits

ADIV2–ADIV0 form a 3-bit field which selects the divide ratio used by the ADC to generate the internal ADC clock. **Table 3-2** shows the available clock configurations. The ADC clock should be set to approximately 1 MHz.

Table 3-2. ADC Clock Divide Ratio

ADIV2	ADIV1	ADIV0	ADC Clock Rate
0	0	0	ADC input clock ÷ 1
0	0	1	ADC input clock ÷ 2
0	1	0	ADC input clock ÷ 4
0	1	1	ADC input clock ÷ 8
1	X(1)	X(1)	ADC input clock ÷ 16

1. X = Don’t care

ADICLK — ADC Input Clock Select Bit

ADICLK selects either the bus clock or the oscillator output clock (CGMXCLK) as the input clock source to generate the internal ADC clock. Reset selects CGMXCLK as the ADC clock source.

1 = Internal bus clock
0 = Oscillator output clock (CGMXCLK)

The ADC requires a clock rate of approximately 1 MHz for correct operation. If the selected clock source is not fast enough, the ADC will generate incorrect conversions. See **17.14 Analog-to-Digital Converter Characteristics**.

$$f_{ADIC} = \frac{f_{CGMXCLK} \text{ or bus frequency}}{\text{ADIV[2:0]}} \cong 1\text{ MHz}$$

MODE1 and MODE0 — Modes of Result Justification Bits

MODE1 and MODE0 select among four modes of operation. The manner in which the ADC conversion results will be placed in the ADC data registers is controlled by these modes of operation. Reset returns right-justified mode.

00 = 8-bit truncation mode
01 = Right justified mode
10 = Left justified mode
11 = Left justified signed data mode

Section 4. Auto Wakeup Module (AWU)

4.1 Introduction

This section describes the auto wakeup module (AWU). The AWU generates a periodic interrupt during stop mode to wake the part up without requiring an external signal. **Figure 4-2** is a block diagram of the AWU.

4.2 Features

Features of the auto wakeup module include:

- One internal interrupt with separate interrupt enable bit, sharing the same keyboard interrupt vector and keyboard interrupt mask bit.
- Exit from low-power stop mode without external signals.
- Selectable timeout periods of 16 milliseconds or 512 milliseconds.
- Dedicated low power internal oscillator separate from the main system clock sources.

Figure 4-1 provides a summary of the input/output (I/O) registers used in conjuction with the AWU.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 60.	Read:	0	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:	▨	▨				▨		
		Reset:	Unaffected by reset							
$001A	Keyboard Status and Control Register (KBSCR) See page 60.	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:	▨	▨	▨	▨	▨	ACKK		
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (KBIER) See page 61.	Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:	▨							
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 4-1. AWU Register Summary

4.3 Functional Description

The function of the auto wakeup logic is to generate periodic wakeup requests to bring the microcontroller unit (MCU) out of stop mode. The wakeup requests are treated as regular keyboard interrupt requests, with the difference that instead of a pin, the interrupt signal is generated by an internal logic.

Writing the AWUIE bit in the keyboard interrupt enable register enables or disables the auto wakeup interrupt input (see **Figure 4-2**). A logic 1 applied to the AWUIREQ input with auto wakeup interrupt request enabled, latches an auto wakeup interrupt request.

Auto wakeup latch, AWUL, can be read directly from the bit 6 position of port A data register (PTA). This is a read-only bit which is occupying an empty bit position on PTA. No PTA associated registers, such as PTA6 data direction or PTA6 pullup exist for this bit.

Entering stop mode will enable the auto wakeup generation logic. An internal RC oscillator (exclusive for the auto wakeup feature) drives the wakeup request generator. Once the overflow count is reached in the generator counter, a wakeup request, AWUIREQ, is latched and sent to the KBI logic. See **Figure 4-1**.

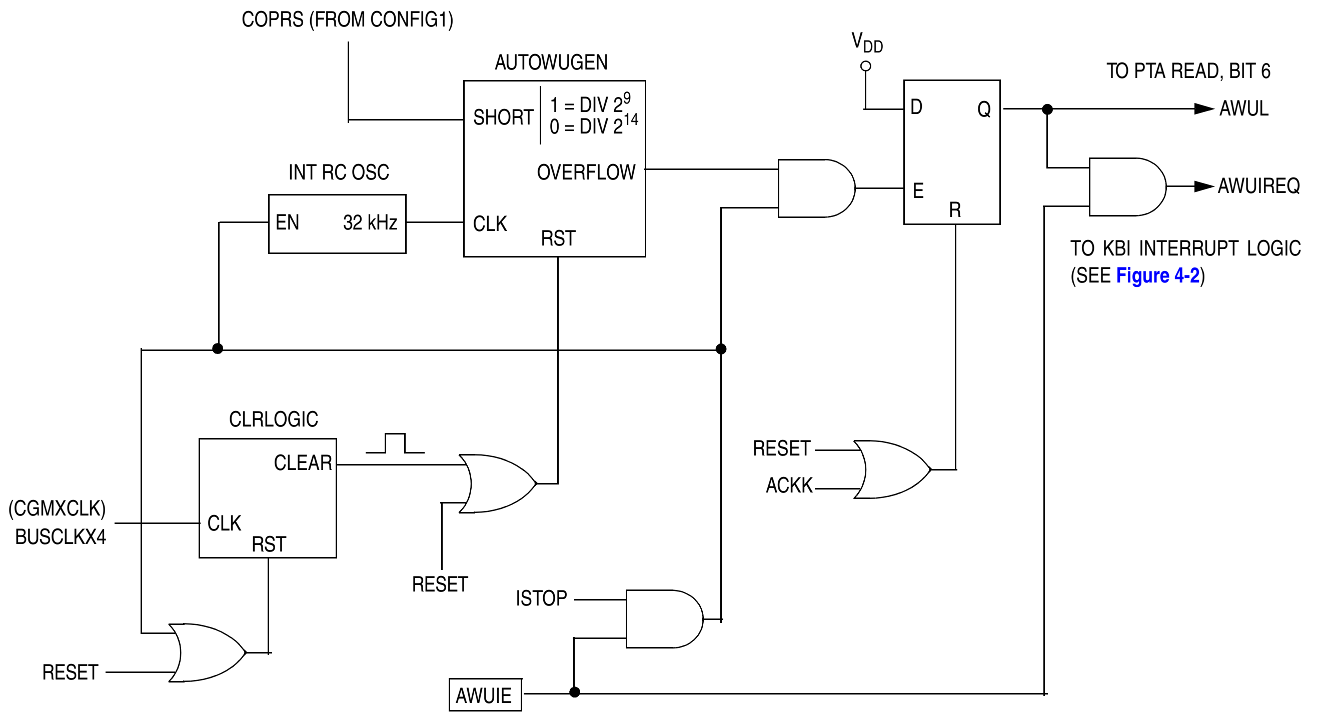


Figure 4-2. Auto Wakeup Interrupt Request Generation Logic

Entering stop mode will enable the auto wakeup generation logic. An internal RC oscillator (exclusive for the auto wakeup feature) drives the wakeup request generator. Once the overflow count is reached in the generator counter, a wakeup request, AWUIREQ, is latched and sent to the KBI logic. See **Figure 4-1**.

Wakeup interrupt requests will only be serviced if the associated interrupt enable bit, AWUIE, in KBIER is set. The AWU shares the keyboard interrupt vector.

The overflow count can be selected from two options defined by the COPRS bit in CONFIG1. This bit was “borrowed” from the computer operating properly (COP) using the fact that the COP feature is idle (no MCU clock available) in stop mode. The typical values of the periodic wakeup request are (at room temperature):

- COPRS = 0: 650 ms @ 5 V, 950 ms @ 3 V
- COPRS = 1: 16 ms @ 5 V, 23 ms @ 3 V

The auto wakeup RC oscillator is highly dependent on operating voltage and temperature. This feature is not recommended for use as a time-keeping function.

The wakeup request is latched to allow the interrupt source identification. The latched value, AWUL, can be read directly from the bit 6 position of PTA data register. This is a read-only bit which is occupying an empty bit position on PTA. No PTA associated registers, such as PTA6 data, PTA6 direction, and PTA6 pullup exist for this bit. The latch can be cleared by writing to the ACKK bit in the KBSCR register. Reset also clears the latch. AWUIE bit in KBI interrupt enable register (see **Figure 4-2**) has no effect on AWUL reading.

The AWU oscillator and counters are inactive in normal operating mode and become active only upon entering stop mode.

4.4 Wait Mode

The AWU module remains inactive in wait mode.

4.5 Stop Mode

When the AWU module is enabled (AWUIE = 1 in the keyboard interrupt enable register) it is activated automatically upon entering stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode. The AWU counters start from ‘0’ each time stop mode is entered.

4.6 Input/Output Registers

The AWU shares registers with the keyboard interrupt (KBI) module and the port A I/O module. The following I/O registers control and monitor operation of the AWU:

- Port A data register (PTA)
- Keyboard interrupt status and control register (KBSCR)
- Keyboard interrupt enable register (KBIER)

4.6.1 Port A I/O Register

The port A data register (PTA) contains a data latch for the state of the AWU interrupt request, in addition to the data latches for port A.

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
Write:	▨	▨				▨		
Reset:	0	0	Unaffected by reset					

▨ = Unimplemented

Figure 4-3. Port A Data Register (PTA)

AWUL — Auto Wakeup Latch

This is a read-only bit which has the value of the auto wakeup interrupt request latch. The wakeup request signal is generated internally. There is no PTA6 port or any of the associated bits such as PTA6 data direction or pullup bits.

1 = Auto wakeup interrupt request is pending
0 = Auto wakeup interrupt request is not pending

NOTE: *PTA5–PTA0 bits are not used in conjuction with the auto wakeup feature. To see a description of these bits, see* **12.2.1 Port A Data Register**.

4.6.2 Keyboard Status and Control Register

The keyboard status and control register (KBSCR):

- Flags keyboard/auto wakeup interrupt requests
- Acknowledges keyboard/auto wakeup interrupt requests
- Masks keyboard/auto wakeup interrupt requests

Address: $001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:	▨	▨	▨	▨	▨	ACKK		
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 4-4. Keyboard Status and Control Register (KBSCR)

Bits 7–4 — Not used

These read-only bits always read as 0s.

KEYF — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending on port A or auto wakeup. Reset clears the KEYF bit.

1 = Keyboard/auto wakeup interrupt pending
0 = No keyboard/auto wakeup interrupt pending

ACKK — Keyboard Acknowledge Bit

Writing a 1 to this write-only bit clears the keyboard/auto wakeup interrupt request on port A and auto wakeup logic. ACKK always reads as 0. Reset clears ACKK.

IMASKK— Keyboard Interrupt Mask Bit

Writing a 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests on port A or auto wakeup. Reset clears the IMASKK bit.

1 = Keyboard/auto wakeup interrupt requests masked
0 = Keyboard/auto wakeup interrupt requests not masked

NOTE: *MODEK is not used in conjuction with the auto wakeup feature. To see a description of this bit, see* ***9.7.1 Keyboard Status and Control Register****.*

4.6.3 Keyboard Interrupt Enable Register

The keyboard interrupt enable register (KBIER) enables or disables the auto wakeup to operate as a keyboard/auto wakeup interrupt input.

Address: $001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Write:	▨							
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 4-5. Keyboard Interrupt Enable Register (KBIER)

AWUIE — Auto Wakeup Interrupt Enable Bit

This read/write bit enables the auto wakeup interrupt input to latch interrupt requests. Reset clears AWUIE.

1 = Auto wakeup enabled as interrupt input
0 = Auto wakeup not enabled as interrupt input

NOTE: *KBIE5–KBIE0 bits are not used in conjuction with the auto wakeup feature. To see a description of these bits, see* ***9.7.2 Keyboard Interrupt Enable Register****.*

Section 5. Configuration Register (CONFIG)

5.1 Introduction

This section describes the configuration registers (CONFIG1 and CONFIG2). The configuration registers enable or disable the following options:

- Stop mode recovery time (32 × BUSCLKX4 cycles or 4096 × BUSCLKX4 cycles)
- STOP instruction
- Computer operating properly module (COP)
- COP reset period (COPRS): $(2^{13}-2^{4}) \times$ BUSCLKX4 or $(2^{18}-2^{4}) \times$ BUSCLKX4
- Low-voltage inhibit (LVI) enable and trip voltage selection
- OSC option selection
- $\overline{\text{IRQ}}$ pin
- $\overline{\text{RST}}$ pin
- Auto wakeup timeout period

5.2 Functional Description

The configuration registers are used in the initialization of various options. The configuration registers can be written once after each reset. Most of the configuration register bits are cleared during reset. Since the various options affect the operation of the microcontroller unit (MCU) it is recommended that this register be written immediately after reset. The configuration register is located at $001E and $001F, and may be read at anytime.

NOTE: *The CONFIG registers are one-time writable by the user after each reset. Upon a reset, the CONFIG registers default to predetermined settings as shown in* ***Figure 5-1*** *and* ***Figure 5-2****.*

Address: $001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	R	R	R	OSCOPT1	OSCOPT0	IRQPUD	IRQEN	RSTEN
Reset:	0	0	0	0	0	0	0	U
POR:	0	0	0	0	0	0	0	0

R = Reserved   U = Unaffected

Figure 5-1 Configuration Register 2 (CONFIG2)

OSCOPT1 and OSCOPT0 — Selection Bits for Oscillator Option
(0, 0) Internal oscillator
(0, 1) External oscillator
(1, 0) External RC oscillator
(1, 1) External XTAL oscillator

IRQPUD — $\overline{\text{IRQ}}$ Pin Pullup Control Bit
1 = Internal pullup is disconnected
0 = Internal pullup is connected between $\overline{\text{IRQ}}$ pin and V_{DD}

IRQEN — $\overline{\text{IRQ}}$ Pin Function Selection Bit
1 = Interrupt request function active in pin
0 = Interrupt request function inactive in pin

RSTEN — $\overline{\text{RST}}$ Pin Function Selection
1 = Reset function active in pin
0 = Reset function inactive in pin

NOTE: *The RSTEN bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.*

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVI5OR3	SSREC	STOP	COPD
Reset:	0	0	0	0	U	0	0	0
POR:	0	0	0	0	0	0	0	0

U = Unaffected

Figure 5-2 Configuration Register 1 (CONFIG1)

COPRS (Out of STOP Mode) — COP Reset Period Selection Bit
1 = COP reset short cycle = $(2^{13} - 2^4) \times$ BUSCLKX4
0 = COP reset long cycle = $(2^{18} - 2^4) \times$ BUSCLKX4

COPRS (In STOP Mode) — Auto Wakeup Period Selection Bit
1 = Auto wakeup short cycle = $(2^9) \times$ INTRCOSC
0 = Auto wakeup long cycle = $(2^{14}) \times$ INTRCOSC

LVISTOP — LVI Enable in Stop Mode Bit

When the LVIPWRD bit is clear, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

1 = LVI enabled during stop mode
0 = LVI disabled during stop mode

LVIRSTD — LVI Reset Disable Bit

LVIRSTD disables the reset signal from the LVI module.

1 = LVI module resets disabled
0 = LVI module resets enabled

LVIPWRD — LVI Power Disable Bit

LVIPWRD disables the LVI module.

1 = LVI module power disabled
0 = LVI module power enabled

LVI5OR3 — LVI 5-V or 3.3-V Operating Mode Bit

LVI5OR3 selects the voltage operating mode of the LVI module. The voltage mode selected for the LVI should match the operating V_{DD} for the LVI's voltage trip points for each of the modes.

1 = LVI operates in 5-V mode
0 = LVI operates in 3.3-V mode

NOTE: *The LVI5OR3 bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.*

SSREC — Short Stop Recovery Bit

SSREC enables the CPU to exit stop mode with a delay of 32 BUSCLKX4 cycles instead of a 4096 BUSCLKX4 cycle delay.

1 = Stop mode recovery after 32 BUSCLKX4 cycles
0 = Stop mode recovery after 4096 BUSCLKX4 cycles

NOTE: *Exiting stop mode by an LVI reset will result in the long stop recovery.*

When using the LVI during normal operation but disabling during stop mode, the LVI will have an enable time of t_{EN}. The system stabilization time for power-on reset and long stop recovery (both 4096 BUSCLKX4 cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32 BUSCLKX4 delay must be greater than the LVI's turn on time to avoid a period in startup where the LVI is not protecting the MCU.

STOP — STOP Instruction Enable Bit

STOP enables the STOP instruction.

1 = STOP instruction enabled
0 = STOP instruction treated as illegal opcode

COPD — COP Disable Bit

COPD disables the COP module.

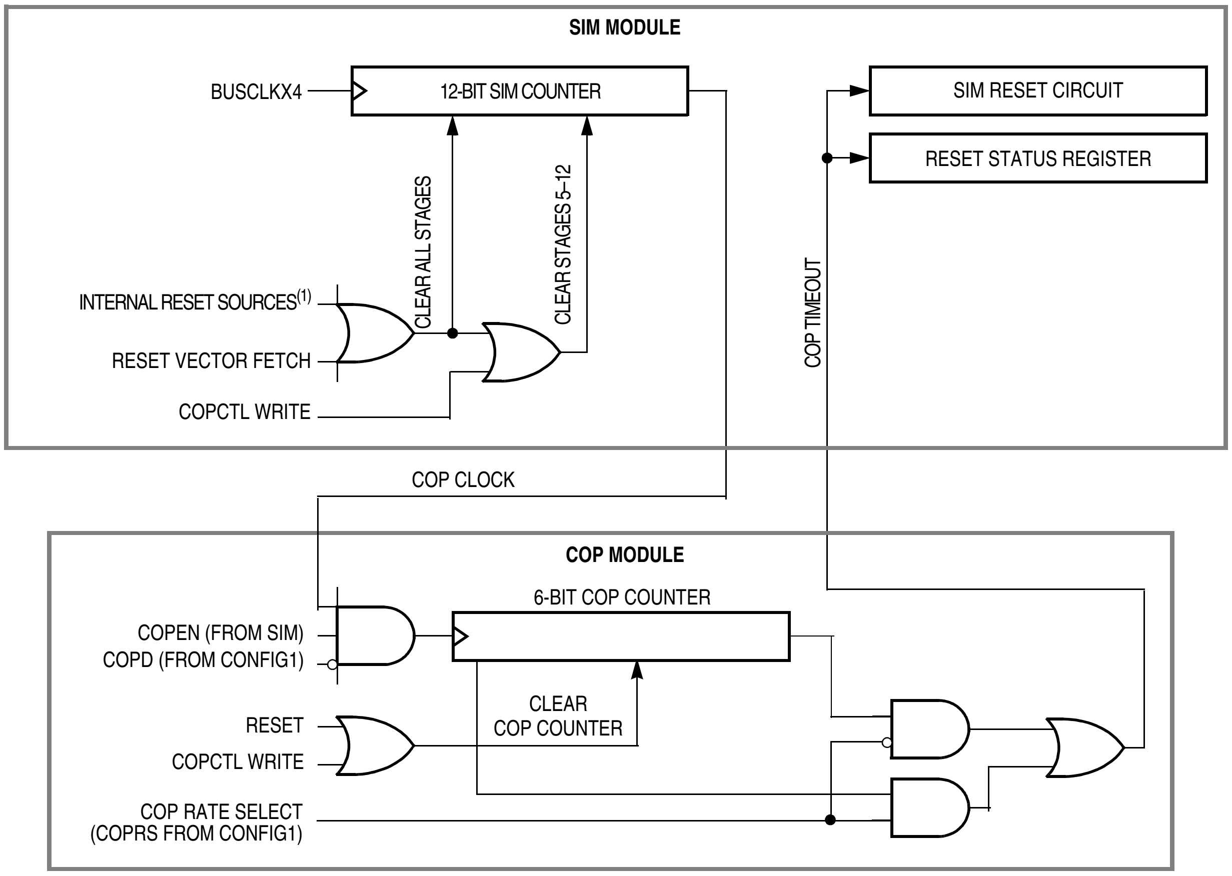
1 = COP module disabled
0 = COP module enabled

Section 6. Computer Operating Properly (COP)

6.1 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the configuration 1 (CONFIG1) register.

6.2 Functional Description



1. See **Section 13. System Integration Module (SIM)** for more details.

Figure 6-1. COP Block Diagram

The COP counter is a free-running 6-bit counter preceded by the 12-bit system integration module (SIM) counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after $2^{18} – 2^4$ or $2^{13} – 2^4$ BUSCLKX4 cycles; depending on the state of the COP rate select bit, COPRS, in configuration register 1. With a $2^{18} – 2^4$ BUSCLKX4 cycle overflow option, a 8-MHz crystal gives a COP timeout period of 32.766 ms. Writing any value to location $FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12–5 of the SIM counter.

NOTE: *Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.*

A COP reset pulls the $\overline{\text{RST}}$ pin low (if the RSTEN bit is set in the CONFIG1 register) for 32 × BUSCLKX4 cycles and sets the COP bit in the reset status register (RSR). See **13.8.1 SIM Reset Status Register**.

NOTE: *Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.*

6.3 I/O Signals

The following paragraphs describe the signals shown in **Figure 6-1**.

6.3.1 BUSCLKX4

BUSCLKX4 is the oscillator output signal. BUSCLKX4 frequency is equal to the crystal frequency or the RC-oscillator frequency.

6.3.2 COPCTL Write

Writing any value to the COP control register (COPCTL) (see **6.4 COP Control Register**) clears the COP counter and clears bits 12–5 of the SIM counter. Reading the COP control register returns the low byte of the reset vector.

6.3.3 Power-On Reset

The power-on reset (POR) circuit in the SIM clears the SIM counter 4096 × BUSCLKX4 cycles after power up.

6.3.4 Internal Reset

An internal reset clears the SIM counter and the COP counter.

6.3.5 Reset Vector Fetch

A reset vector fetch occurs when the vector address appears on the data bus. A reset vector fetch clears the SIM counter.

6.3.6 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register (CONFIG). See **Section 5. Configuration Register (CONFIG)**.

6.3.7 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register 1 (CONFIG1). See **Section 5. Configuration Register (CONFIG)**.

6.4 COP Control Register

The COP control register (COPCTL) is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LOW BYTE OF RESET VECTOR							
Write:	CLEAR COP COUNTER							
Reset:	Unaffected by reset							

Figure 6-2. COP Control Register (COPCTL)

6.5 Interrupts

The COP does not generate CPU interrupt requests.

6.6 Monitor Mode

The COP is disabled in monitor mode when V_{TST} is present on the $\overline{IRQ}$ pin.

6.7 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

6.7.1 Wait Mode

The COP remains active during wait mode. If COP is enabled, a reset will occur at COP timeout.

6.7.2 Stop Mode

Stop mode turns off the BUSCLKX4 input to the COP and clears the SIM counter. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

6.8 COP Module During Break Mode

The COP is disabled during a break interrupt with monitor mode when BDCOP bit is set in break auxiliary register (BRKAR).

Section 7. Central Processor Unit (CPU)

7.1 Introduction

The M68HC08 CPU (central processor unit) is an enhanced and fully object-code-compatible version of the M68HC05 CPU. The *CPU08 Reference Manual* (Motorola document order number CPU08RM/AD) contains a description of the CPU instruction set, addressing modes, and architecture.

7.2 Features

Features of the CPU include:

- Object code fully upward-compatible with M68HC05 Family
- 16-bit stack pointer with stack manipulation instructions
- 16-bit index register with x-register manipulation instructions
- 8-MHz CPU internal bus frequency
- 64-Kbyte program/data memory space
- 16 addressing modes
- Memory-to-memory data moves without using accumulator
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- Enhanced binary-coded decimal (BCD) data handling
- Modular architecture with expandable internal bus definition for extension of addressing range beyond 64 Kbytes
- Low-power stop and wait modes

7.3 CPU Registers

Figure 7-1 shows the five CPU registers. CPU registers are not part of the memory map.

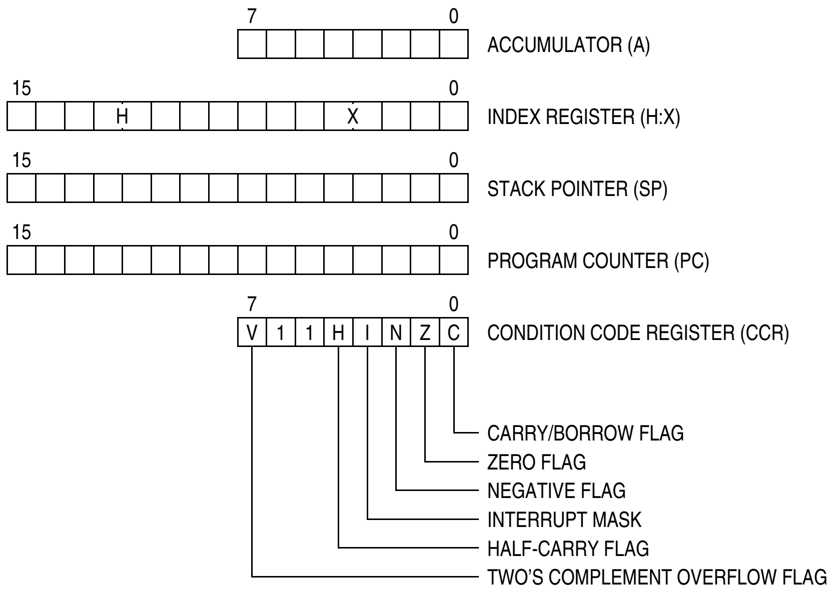


Figure 7-1. CPU Registers

7.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:								
Reset:	Unaffected by reset							

Figure 7-2. Accumulator (A)

7.3.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Read:																
Write:																
Reset:	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

X = Indeterminate

Figure 7-3. Index Register (H:X)

7.3.3 Stack Pointer

The stack pointer is a 16-bit register that contains the address of the next location on the stack. During a reset, the stack pointer is preset to $00FF. The reset stack pointer (RSP) instruction sets the least significant byte to $FF and does not affect the most significant byte. The stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

In the stack pointer 8-bit offset and 16-bit offset addressing modes, the stack pointer can function as an index register to access data on the stack. The CPU uses the contents of the stack pointer to determine the conditional address of the operand.

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Read:																
Write:																
Reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Figure 7-4. Stack Pointer (SP)

NOTE: *The location of the stack is arbitrary and may be relocated anywhere in random-access memory (RAM). Moving the SP out of page 0 ($0000 to $00FF) frees direct address (page 0) space. For correct operation, the stack pointer must point only to RAM locations.*

7.3.4 Program Counter

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

During reset, the program counter is loaded with the reset vector address located at $FFFE and $FFFF. The vector address is the address of the first instruction to be executed after exiting the reset state.

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Read: / Write:																
Reset:	Loaded with vector from $FFFE and $FFFF															

Figure 7-5. Program Counter (PC)

7.3.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	V	1	1	H	I	N	Z	C
Reset:	X	1	1	X	1	X	X	X

X = Indeterminate

Figure 7-6. Condition Code Register (CCR)

V — Overflow Flag

The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag.

1 = Overflow
0 = No overflow

H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C flags to determine the appropriate correction factor.

1 = Carry between bits 3 and 4
0 = No carry between bits 3 and 4

I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set
automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

1 = Interrupts disabled
0 = Interrupts enabled

NOTE: *To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.*

After the I bit is cleared, the highest-priority interrupt request is serviced first. A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).

N — Negative flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

1 = Negative result
0 = Non-negative result

Z — Zero flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of $00.

1 = Zero result
0 = Non-zero result

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

1 = Carry out of bit 7
0 = No carry out of bit 7

7.4 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (Motorola document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

7.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

7.5.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

7.5.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

7.6 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC:$FFFD or with $FEFC:$FEFD in monitor mode

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

7.7 Instruction Set Summary

Table 7-1 provides a summary of the M68HC08 instruction set.

Table 7-1. Instruction Set Summary (Sheet 1 of 7)

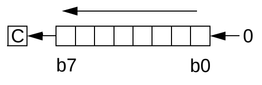
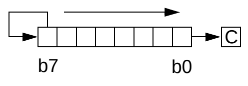
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X ADC *opr*,SP ADC *opr*,SP	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X ADD *opr*,SP ADD *opr*,SP	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #*opr*	Add Immediate Value (Signed) to SP	SP ← (SP) + (16 « M)	–	–	–	–	–	–	IMM	A7	ii	2
AIX #*opr*	Add Immediate Value (Signed) to H:X	H:X ← (H:X) + (16 « M)	–	–	–	–	–	–	IMM	AF	ii	2
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X AND *opr*,SP AND *opr*,SP	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X ASL *opr*,SP	Arithmetic Shift Left (Same as LSL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR *opr*,X ASR *opr*,SP	Arithmetic Shift Right		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + rel ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BCLR *n*, *opr*	Clear Bit n in M	Mn ← 0	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? (Z) = 1	–	–	–	–	–	–	REL	27	rr	3

Table 7-1. Instruction Set Summary (Sheet 2 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BGE *opr*	Branch if Greater Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? $(N \oplus V) = 0$	–	–	–	–	–	–	REL	90	rr	3
BGT *opr*	Branch if Greater Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) | $(N \oplus V) = 0$	–	–	–	–	–	–	REL	92	rr	3
BHCC *rel*	Branch if Half Carry Bit Clear	PC ← (PC) + 2 + *rel* ? (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS *rel*	Branch if Half Carry Bit Set	PC ← (PC) + 2 + *rel* ? (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? (C) | (Z) = 0	–	–	–	–	–	–	REL	22	rr	3
BHS *rel*	Branch if Higher or Same (Same as BCC)	PC ← (PC) + 2 + *rel* ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH *rel*	Branch if $\overline{IRQ}$ Pin High	PC ← (PC) + 2 + *rel* ? $\overline{IRQ}$ = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL *rel*	Branch if $\overline{IRQ}$ Pin Low	PC ← (PC) + 2 + *rel* ? $\overline{IRQ}$ = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X BIT *opr*,SP BIT *opr*,SP	Bit Test	(A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A5 B5 C5 D5 E5 F5 9EE5 9ED5	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
BLE *opr*	Branch if Less Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) | $(N \oplus V) = 1$	–	–	–	–	–	–	REL	93	rr	3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? (C) | (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT *opr*	Branch if Less Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? $(N \oplus V) = 1$	–	–	–	–	–	–	REL	91	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel*	–	–	–	–	–	–	REL	20	rr	3
BRCLR *n*,*opr*,*rel*	Branch if Bit *n* in M Clear	PC ← (PC) + 3 + *rel* ? (Mn) = 0	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2	–	–	–	–	–	–	REL	21	rr	3

Table 7-1. Instruction Set Summary (Sheet 3 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BRSET *n*,*opr*,*rel*	Branch if Bit *n* in M Set	PC ← (PC) + 3 + *rel* ? (Mn) = 1	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n*,*opr*	Set Bit *n* in M	Mn ← 1	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	–	–	–	–	–	–	REL	AD	rr	4
CBEQ *opr,rel* CBEQA #*opr,rel* CBEQX #*opr,rel* CBEQ *opr*,X+,*rel* CBEQ X+,*rel* CBEQ *opr*,SP,*rel*	Compare and Branch if Equal	PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (X) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 2 + rel ? (A) – (M) = $00 PC ← (PC) + 4 + rel ? (A) – (M) = $00	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask	I ← 0	–	–	0	–	–	–	INH	9A		2
CLR *opr* CLRA CLRX CLRH CLR *opr*,X CLR ,X CLR *opr*,SP	Clear	M ← $00 A ← $00 X ← $00 H ← $00 M ← $00 M ← $00 M ← $00	0	–	–	0	1	–	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff	3 1 1 1 3 2 4
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X CMP *opr*,SP CMP *opr*,SP	Compare A with M	(A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A1 B1 C1 D1 E1 F1 9EE1 9ED1	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
COM *opr* COMA COMX COM *opr*,X COM ,X COM *opr*,SP	Complement (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (M) X ← ($\overline{X}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	0	–	–	↕	↕	1	DIR INH INH IX1 IX SP1	33 43 53 63 73 9E63	dd ff ff	4 1 1 4 3 5
CPHX #*opr* CPHX *opr*	Compare H:X with M	(H:X) – (M:M + 1)	↕	–	–	↕	↕	↕	IMM DIR	65 75	ii ii+1 dd	3 4

Table 7-1. Instruction Set Summary (Sheet 4 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
CPX #*opr* CPX *opr* CPX *opr* CPX ,X CPX *opr*,X CPX *opr*,X CPX *opr*,SP CPX *opr*,SP	Compare X with M	(X) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A3 B3 C3 D3 E3 F3 9EE3 9ED3	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
DAA	Decimal Adjust A	$(A)_{10}$	U	–	–	↕	↕	↕	INH	72		2
DBNZ *opr,rel* DBNZA *rel* DBNZX *rel* DBNZ *opr*,X,*rel* DBNZ X,*rel* DBNZ *opr*,SP,*rel*	Decrement and Branch if Not Zero	A ← (A) – 1 or M ← (M) – 1 or X ← (X) – 1 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 4 + *rel* ? (result) ≠ 0	–	–	–	–	–	–	DIR INH INH IX1 IX SP1	3B 4B 5B 6B 7B 9E6B	dd rr rr rr ff rr rr ff rr	5 3 3 5 4 6
DEC *opr* DECA DECX DEC *opr*,X DEC ,X DEC *opr*,SP	Decrement	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1 M ← (M) – 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3A 4A 5A 6A 7A 9E6A	dd ff ff	4 1 1 4 3 5
DIV	Divide	A ← (H:A)/(X) H ← Remainder	–	–	–	–	↕	↕	INH	52		7
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X EOR *opr*,SP EOR *opr*,SP	Exclusive OR M with A	A ← (A ⊕ M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
INC *opr* INCA INCX INC *opr*,X INC ,X INC *opr*,SP	Increment	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 1 4 3 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Jump	PC ← Jump Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + *n* (*n* = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Unconditional Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	4 5 6 5 4
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X LDA *opr*,SP LDA *opr*,SP	Load A from M	A ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

Table 7-1. Instruction Set Summary (Sheet 5 of 7)

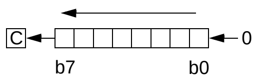
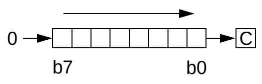
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
LDHX #*opr* LDHX *opr*	Load H:X from M	H:X ← (M:M + 1)	0	–	–	↕	↕	–	IMM DIR	45 55	ii jj dd	3 4
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X LDX *opr*,SP LDX *opr*,SP	Load X from M	X ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X LSL *opr*,SP	Logical Shift Left (Same as ASL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
LSR *opr* LSRA LSR*X* LSR *opr*,X LSR ,X LSR *opr*,SP	Logical Shift Right		↕	–	–	0	↕	↕	DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff	4 1 1 4 3 5
MOV *opr,opr* MOV *opr*,X+ MOV #*opr,opr* MOV X+,*opr*	Move	$(M)_{Destination} \leftarrow (M)_{Source}$ H:X ← (H:X) + 1 (IX+D, DIX+)	0	–	–	↕	↕	–	DD DIX+ IMD IX+D	4E 5E 6E 7E	dd dd dd ii dd dd	5 4 4 4
MUL	Unsigned multiply	X:A ← (X) × (A)	–	0	–	–	–	0	INH	42		5
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X NEG *opr*,SP	Negate (Two's Complement)	M ← –(M) = \$00 – (M) A ← –(A) = \$00 – (A) X ← –(X) = \$00 – (X) M ← –(M) = \$00 – (M) M ← –(M) = \$00 – (M)	↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	30 40 50 60 70 9E60	dd ff ff	4 1 1 4 3 5
NOP	No Operation	None	–	–	–	–	–	–	INH	9D		1
NSA	Nibble Swap A	A ← (A[3:0]:A[7:4])	–	–	–	–	–	–	INH	62		3
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X ORA *opr*,SP ORA *opr*,SP	Inclusive OR A and M	A ← (A) | (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	AA BA CA DA EA FA 9EEA 9EDA	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
PSHA	Push A onto Stack	Push (A); SP ← (SP) – 1	–	–	–	–	–	–	INH	87		2
PSHH	Push H onto Stack	Push (H); SP ← (SP) – 1	–	–	–	–	–	–	INH	8B		2
PSHX	Push X onto Stack	Push (X); SP ← (SP) – 1	–	–	–	–	–	–	INH	89		2
PULA	Pull A from Stack	SP ← (SP + 1); Pull (A)	–	–	–	–	–	–	INH	86		2
PULH	Pull H from Stack	SP ← (SP + 1); Pull (H)	–	–	–	–	–	–	INH	8A		2
PULX	Pull X from Stack	SP ← (SP + 1); Pull (X)	–	–	–	–	–	–	INH	88		2

Table 7-1. Instruction Set Summary (Sheet 6 of 7)

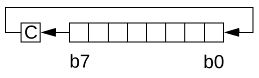
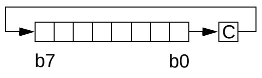
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X ROL *opr*,SP	Rotate Left through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X ROR *opr*,SP	Rotate Right through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	SP ← $FF	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		7
RTS	Return from Subroutine	SP ← SP + 1; Pull (PCH) SP ← SP + 1; Pull (PCL)	–	–	–	–	–	–	INH	81		4
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X SBC *opr*,SP SBC *opr*,SP	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask	I ← 1	–	–	1	–	–	–	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X STA *opr*,SP STA *opr*,SP	Store A in M	M ← (A)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
STHX *opr*	Store H:X in M	(M:M + 1) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STOP	Enable $\overline{\text{IRQ}}$ Pin; Stop Oscillator	I ← 0; Stop Oscillator	–	–	0	–	–	–	INH	8E		1
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X STX *opr*,SP STX *opr*,SP	Store X in M	M ← (X)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X SUB *opr*,SP SUB *opr*,SP	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

Table 7-1. Instruction Set Summary (Sheet 7 of 7)

Source Form	Operation	Description	Effect on CCR V	H	I	N	Z	C	Address Mode	Opcode	Operand	Cycles
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	–	–	1	–	–	–	INH	83		9
TAP	Transfer A to CCR	CCR ← (A)	↕	↕	↕	↕	↕	↕	INH	84		2
TAX	Transfer A to X	X ← (A)	–	–	–	–	–	–	INH	97		1
TPA	Transfer CCR to A	A ← (CCR)	–	–	–	–	–	–	INH	85		1
TST *opr* TSTA TSTX TST *opr*,X TST ,X TST *opr*,SP	Test for Negative or Zero	(A) – $00 or (X) – $00 or (M) – $00	0	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4
TSX	Transfer SP to H:X	H:X ← (SP) + 1	–	–	–	–	–	–	INH	95		2
TXA	Transfer X to A	A ← (X)	–	–	–	–	–	–	INH	9F		1
TXS	Transfer H:X to SP	(SP) ← (H:X) – 1	–	–	–	–	–	–	INH	94		2

A	Accumulator
C	Carry/borrow bit
CCR	Condition code register
dd	Direct address of operand
dd rr	Direct address of operand and relative offset of branch instruction
DD	Direct to direct addressing mode
DIR	Direct addressing mode
DIX+	Direct to indexed with post increment addressing mode
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing
EXT	Extended addressing mode
ff	Offset byte in indexed, 8-bit offset addressing
H	Half-carry bit
H	Index register high byte
hh ll	High and low bytes of operand address in extended addressing
I	Interrupt mask
ii	Immediate operand byte
IMD	Immediate source to direct destination addressing mode
IMM	Immediate addressing mode
INH	Inherent addressing mode
IX	Indexed, no offset addressing mode
IX+	Indexed, no offset, post increment addressing mode
IX+D	Indexed with post increment to direct addressing mode
IX1	Indexed, 8-bit offset addressing mode
IX1+	Indexed, 8-bit offset, post increment addressing mode
IX2	Indexed, 16-bit offset addressing mode
M	Memory location
N	Negative bit
n	Any bit
opr	Operand (one or two bytes)
PC	Program counter
PCH	Program counter high byte
PCL	Program counter low byte
REL	Relative addressing mode
rel	Relative program counter offset byte
rr	Relative program counter offset byte
SP1	Stack pointer, 8-bit offset addressing mode
SP2	Stack pointer 16-bit offset addressing mode
SP	Stack pointer
U	Undefined
V	Overflow bit
X	Index register low byte
Z	Zero bit
&	Logical AND
|	Logical OR
⊕	Logical EXCLUSIVE OR
( )	Contents of
–( )	Negation (two's complement)
#	Immediate value
«	Sign extend
←	Loaded with
?	If
:	Concatenated with
↕	Set or cleared
—	Not affected

7.8 Opcode Map

See **Table 7-2**.

Table 7-2. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write						Control		Register/Memory							
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
MSB / LSB	0	1	2	3	4	5	6	9E6	7	8	9	A	B	C	D	9ED	E	9EE	F
0	5 BRSET0 3 DIR	4 BSET0 2 DIR	3 BRA 2 REL	4 NEG 2 DIR	1 NEGA 1 INH	1 NEGX 1 INH	4 NEG 2 IX1	5 NEG 3 SP1	3 NEG 1 IX	7 RTI 1 INH	3 BGE 2 REL	2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	4 SUB 3 IX2	5 SUB 4 SP2	3 SUB 2 IX1	4 SUB 3 SP1	2 SUB 1 IX
1	5 BRCLR0 3 DIR	4 BCLR0 2 DIR	3 BRN 2 REL	5 CBEQ 3 DIR	4 CBEQA 3 IMM	4 CBEQX 3 IMM	5 CBEQ 3 IX1+	6 CBEQ 4 SP1	4 CBEQ 2 IX+	4 RTS 1 INH	3 BLT 2 REL	2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	4 CMP 3 IX2	5 CMP 4 SP2	3 CMP 2 IX1	4 CMP 3 SP1	2 CMP 1 IX
2	5 BRSET1 3 DIR	4 BSET1 2 DIR	3 BHI 2 REL	▨	5 MUL 1 INH	7 DIV 1 INH	3 NSA 1 INH	▨	2 DAA 1 INH	▨	3 BGT 2 REL	2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	4 SBC 3 IX2	5 SBC 4 SP2	3 SBC 2 IX1	4 SBC 3 SP1	2 SBC 1 IX
3	5 BRCLR1 3 DIR	4 BCLR1 2 DIR	3 BLS 2 REL	4 COM 2 DIR	1 COMA 1 INH	1 COMX 1 INH	4 COM 2 IX1	5 COM 3 SP1	3 COM 1 IX	9 SWI 1 INH	3 BLE 2 REL	2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	4 CPX 3 IX2	5 CPX 4 SP2	3 CPX 2 IX1	4 CPX 3 SP1	2 CPX 1 IX
4	5 BRSET2 3 DIR	4 BSET2 2 DIR	3 BCC 2 REL	4 LSR 2 DIR	1 LSRA 1 INH	1 LSRX 1 INH	4 LSR 2 IX1	5 LSR 3 SP1	3 LSR 1 IX	2 TAP 1 INH	2 TXS 1 INH	2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	4 AND 3 IX2	5 AND 4 SP2	3 AND 2 IX1	4 AND 3 SP1	2 AND 1 IX
5	5 BRCLR2 3 DIR	4 BCLR2 2 DIR	3 BCS 2 REL	4 STHX 2 DIR	3 LDHX 3 IMM	4 LDHX 2 DIR	3 CPHX 3 IMM	▨	4 CPHX 2 DIR	1 TPA 1 INH	2 TSX 1 INH	2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	4 BIT 3 IX2	5 BIT 4 SP2	3 BIT 2 IX1	4 BIT 3 SP1	2 BIT 1 IX
6	5 BRSET3 3 DIR	4 BSET3 2 DIR	3 BNE 2 REL	4 ROR 2 DIR	1 RORA 1 INH	1 RORX 1 INH	4 ROR 2 IX1	5 ROR 3 SP1	3 ROR 1 IX	2 PULA 1 INH	▨	2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	4 LDA 3 IX2	5 LDA 4 SP2	3 LDA 2 IX1	4 LDA 3 SP1	2 LDA 1 IX
7	5 BRCLR3 3 DIR	4 BCLR3 2 DIR	3 BEQ 2 REL	4 ASR 2 DIR	1 ASRA 1 INH	1 ASRX 1 INH	4 ASR 2 IX1	5 ASR 3 SP1	3 ASR 1 IX	2 PSHA 1 INH	1 TAX 1 INH	2 AIS 2 IMM	3 STA 2 DIR	4 STA 3 EXT	4 STA 3 IX2	5 STA 4 SP2	3 STA 2 IX1	4 STA 3 SP1	2 STA 1 IX
8	5 BRSET4 3 DIR	4 BSET4 2 DIR	3 BHCC 2 REL	4 LSL 2 DIR	1 LSLA 1 INH	1 LSLX 1 INH	4 LSL 2 IX1	5 LSL 3 SP1	3 LSL 1 IX	2 PULX 1 INH	1 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	4 EOR 3 IX2	5 EOR 4 SP2	3 EOR 2 IX1	4 EOR 3 SP1	2 EOR 1 IX
9	5 BRCLR4 3 DIR	4 BCLR4 2 DIR	3 BHCS 2 REL	4 ROL 2 DIR	1 ROLA 1 INH	1 ROLX 1 INH	4 ROL 2 IX1	5 ROL 3 SP1	3 ROL 1 IX	2 PSHX 1 INH	1 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	4 ADC 3 IX2	5 ADC 4 SP2	3 ADC 2 IX1	4 ADC 3 SP1	2 ADC 1 IX
A	5 BRSET5 3 DIR	4 BSET5 2 DIR	3 BPL 2 REL	4 DEC 2 DIR	1 DECA 1 INH	1 DECX 1 INH	4 DEC 2 IX1	5 DEC 3 SP1	3 DEC 1 IX	2 PULH 1 INH	2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	4 ORA 3 IX2	5 ORA 4 SP2	3 ORA 2 IX1	4 ORA 3 SP1	2 ORA 1 IX
B	5 BRCLR5 3 DIR	4 BCLR5 2 DIR	3 BMI 2 REL	5 DBNZ 3 DIR	3 DBNZA 2 INH	3 DBNZX 2 INH	5 DBNZ 3 IX1	6 DBNZ 4 SP1	4 DBNZ 2 IX	2 PSHH 1 INH	2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	4 ADD 3 IX2	5 ADD 4 SP2	3 ADD 2 IX1	4 ADD 3 SP1	2 ADD 1 IX
C	5 BRSET6 3 DIR	4 BSET6 2 DIR	3 BMC 2 REL	4 INC 2 DIR	1 INCA 1 INH	1 INCX 1 INH	4 INC 2 IX1	5 INC 3 SP1	3 INC 1 IX	1 CLRH 1 INH	1 RSP 1 INH	▨	2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	▨	3 JMP 2 IX1	▨	2 JMP 1 IX
D	5 BRCLR6 3 DIR	4 BCLR6 2 DIR	3 BMS 2 REL	3 TST 2 DIR	1 TSTA 1 INH	1 TSTX 1 INH	3 TST 2 IX1	4 TST 3 SP1	2 TST 1 IX	▨	1 NOP 1 INH	4 BSR 2 REL	4 JSR 2 DIR	5 JSR 3 EXT	6 JSR 3 IX2	▨	5 JSR 2 IX1	▨	4 JSR 1 IX
E	5 BRSET7 3 DIR	4 BSET7 2 DIR	3 BIL 2 REL	▨	5 MOV 3 DD	4 MOV 2 DIX+	4 MOV 3 IMD	▨	4 MOV 2 IX+D	1 STOP 1 INH	*	2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	4 LDX 3 IX2	5 LDX 4 SP2	3 LDX 2 IX1	4 LDX 3 SP1	2 LDX 1 IX
F	5 BRCLR7 3 DIR	4 BCLR7 2 DIR	3 BIH 2 REL	3 CLR 2 DIR	1 CLRA 1 INH	1 CLRX 1 INH	3 CLR 2 IX1	4 CLR 3 SP1	2 CLR 1 IX	1 WAIT 1 INH	1 TXA 1 INH	2 AIX 2 IMM	3 STX 2 DIR	4 STX 3 EXT	4 STX 3 IX2	5 STX 4 SP2	3 STX 2 IX1	4 STX 3 SP1	2 STX 1 IX

INH	Inherent	REL	Relative	SP1	Stack Pointer, 8-Bit Offset
IMM	Immediate	IX	Indexed, No Offset	SP2	Stack Pointer, 16-Bit Offset
DIR	Direct	IX1	Indexed, 8-Bit Offset	IX+	Indexed, No Offset with Post Increment
EXT	Extended	IX2	Indexed, 16-Bit Offset		
DD	Direct-Direct	IMD	Immediate-Direct	IX1+	Indexed, 1-Byte Offset with Post Increment
IX+D	Indexed-Direct	DIX+	Direct-Indexed		

*Pre-byte for stack pointer indexed instructions

	MSB / LSB	0	High Byte of Opcode in Hexadecimal
Low Byte of Opcode in Hexadecimal	0	5 BRSET0 3 DIR	Cycles; Opcode Mnemonic; Number of Bytes / Addressing Mode

Section 8. External Interrupt (IRQ)

8.1 Introduction

The $\overline{\text{IRQ}}$ pin (external interrupt), shared with PTA2 (general purpose input) and keyboard interrupt (KBI), provides a maskable interrupt input.

8.2 Features

Features of the IRQ module include the following:

- External interrupt pin, $\overline{\text{IRQ}}$
- $\overline{\text{IRQ}}$ interrupt control bits
- Hysteresis buffer
- Programmable edge-only or edge and level interrupt sensitivity
- Automatic interrupt acknowledge
- Selectable internal pullup resistor

8.3 Functional Description

$\overline{\text{IRQ}}$ pin functionality is enabled by setting configuration register 2 (CONFIG2) IRQEN bit accordingly. A zero disables the IRQ function and $\overline{\text{IRQ}}$ will assume the other shared functionalities. A one enables the IRQ function.

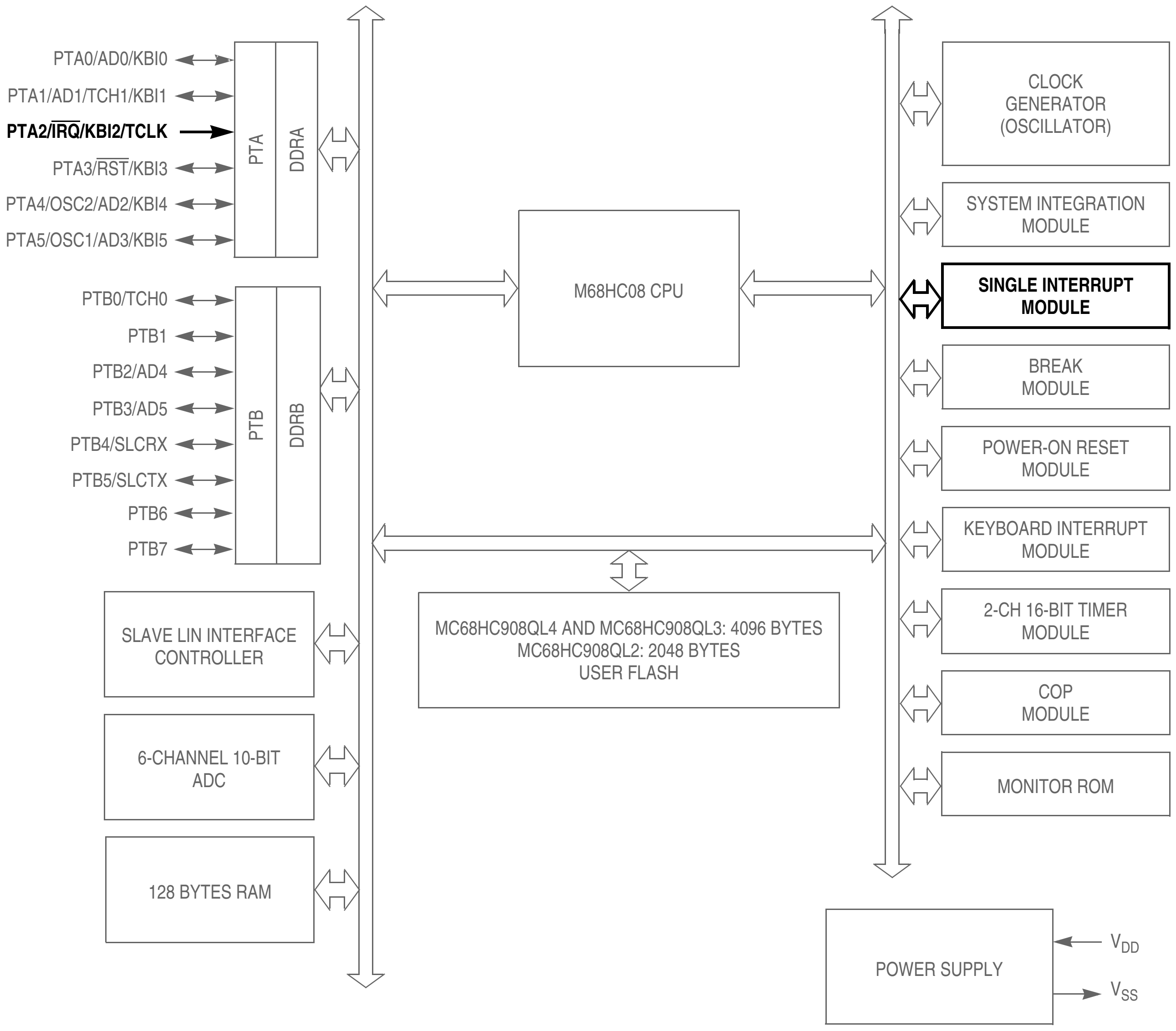
A logic 0 applied to the external interrupt pin can latch a central processor unit (CPU) interrupt request. **Figure 8-2** shows the structure of the IRQ module.

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ latch. An interrupt latch remains set until one of the following actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears the IRQ latch.
- Software clear — Software can clear the interrupt latch by writing to the acknowledge bit in the interrupt status and control register (ISCR). Writing a 1 to the ACK bit clears the IRQ latch.
- Reset — A reset automatically clears the interrupt latch.

The external interrupt pin is falling-edge-triggered and is software- configurable to be either falling-edge or falling-edge and low-level triggered. The MODE bit in the ISCR controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin.

When the interrupt pin is edge-triggered only, the CPU interrupt request remains set until a vector fetch, software clear, or reset occurs.



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30 kΩ) pull up
PTA0, PTA1, PTA3–PTA5: High current sink and source capability
PTA0–PTA5: Pins have programmable keyboard interrupt and pull up
ADC pins only available on MC68HC908QL4 and MC68HC908QL2

Figure 8-1. Block Diagram Highlighting IRQ Block and Pins

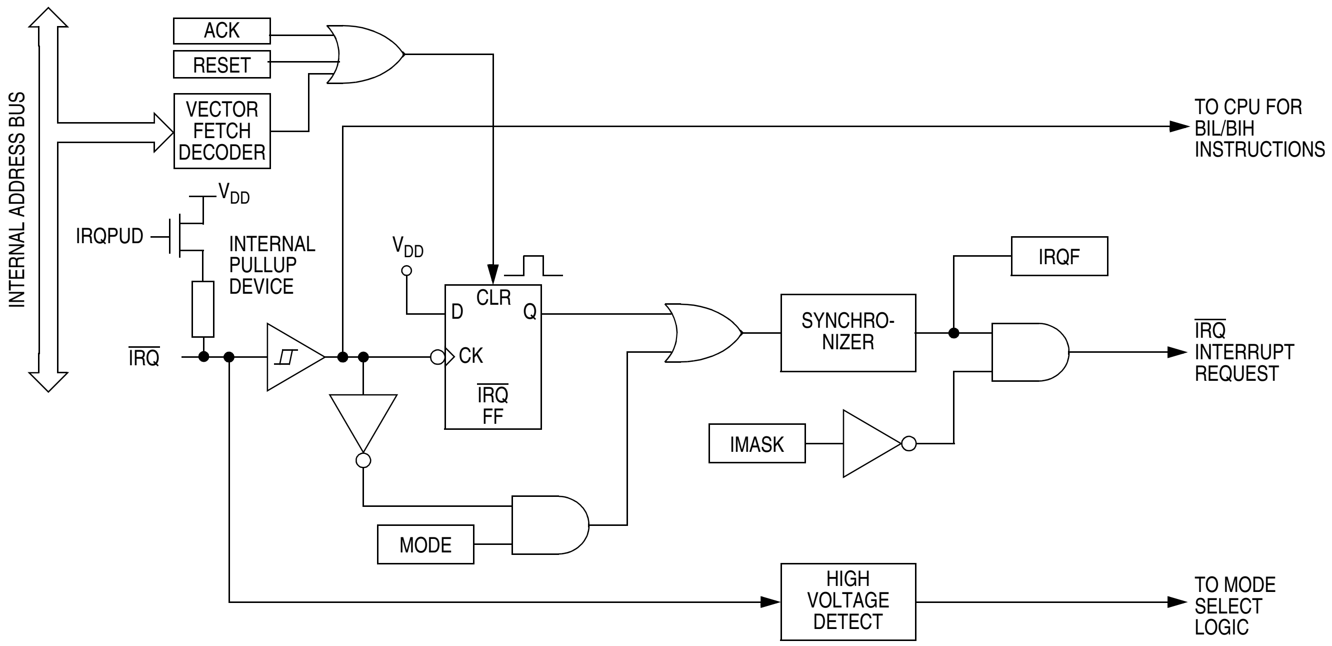


Figure 8-2. IRQ Module Block Diagram

When the interrupt pin is both falling-edge and low-level triggered, the CPU interrupt request remains set until both of the following occur:

- Vector fetch or software clear
- Return of the interrupt pin to logic 1

The vector fetch or software clear may occur before or after the interrupt pin returns to logic 1. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

When set, the IMASK bit in the ISCR mask all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the IMASK bit is clear.

NOTE: *The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests. See **13.6 Exception Control**.*

Figure 8-3 provides a summary of the IRQ I/O register.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001D	IRQ Status and Control Register (INTSCR) See page 89.	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:	▨	▨	▨	▨	▨	ACK	IMASK	MODE
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 8-3. IRQ I/O Register Summary

8.4 $\overline{\text{IRQ}}$ Pin

A logic 0 on the $\overline{\text{IRQ}}$ pin can latch an interrupt request into the IRQ latch. A vector fetch, software clear, or reset clears the IRQ latch.

If the MODE bit is set, the $\overline{\text{IRQ}}$ pin is both falling-edge sensitive and low-level sensitive. With MODE set, both of the following actions must occur to clear IRQ:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the latch. Software may generate the interrupt acknowledge signal by writing a 1 to the ACK bit in the interrupt status and control register (ISCR). The ACK bit is useful in applications that poll the $\overline{\text{IRQ}}$ pin and require software to clear the IRQ latch. Writing to the ACK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACK does not affect subsequent transitions on the $\overline{\text{IRQ}}$ pin. A falling edge that occurs after writing to the ACK bit latches another interrupt request. If the IRQ mask bit, IMASK, is clear, the CPU loads the program counter with the vector address at locations \$FFFA and \$FFFB.
- Return of the $\overline{\text{IRQ}}$ pin to logic 1 — As long as the $\overline{\text{IRQ}}$ pin is at logic 0, IRQ remains active.

The vector fetch or software clear and the return of the $\overline{\text{IRQ}}$ pin to logic 1 may occur in any order. The interrupt request remains pending as long as the $\overline{\text{IRQ}}$ pin is at logic 0. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

If the MODE bit is clear, the $\overline{\text{IRQ}}$ pin is falling-edge sensitive only. With MODE clear, a vector fetch or software clear immediately clears the IRQ latch.

The IRQF bit in the ISCR register can be used to check for pending interrupts. The IRQF bit is not affected by the IMASK bit, which makes it useful in applications where polling is preferred.

NOTE: *When the $\overline{\text{IRQ}}$ function is enabled in the CONFIG2 register, the BIH and BIL instructions can be used to read the logic level on the $\overline{\text{IRQ}}$ pin. If the $\overline{\text{IRQ}}$ function is disabled, these instructions will behave as if the $\overline{\text{IRQ}}$ pin is a logic 1, regardless of the actual level on the pin. Conversely, when the $\overline{\text{IRQ}}$ function is enabled, bit 2 of the port A data register will always read a 0.*

NOTE: *When using the level-sensitive interrupt trigger, avoid false interrupts by masking interrupt requests in the interrupt routine. An internal pullup resistor to V_{DD} is connected to the $\overline{\text{IRQ}}$ pin; this can be disabled by setting the IRQPUD bit in the CONFIG2 register (\$001E).*

8.5 IRQ Module During Break Interrupts

The system integration module (SIM) controls whether the IRQ latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear the latches during the break state. See **Section 13. System Integration Module (SIM)**.

To allow software to clear the IRQ latch during a break interrupt, write a 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latches during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), writing to the ACK bit in the IRQ status and control register during the break state has no effect on the IRQ latch.

8.6 IRQ Status and Control Register

The IRQ status and control register (ISCR) controls and monitors operation of the IRQ module, see **Section 5. Configuration Register (CONFIG)**.

The ISCR has the following functions:

- Shows the state of the IRQ flag
- Clears the IRQ latch
- Masks IRQ and interrupt request
- Controls triggering sensitivity of the $\overline{\text{IRQ}}$ interrupt pin

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	IRQF		IMASK	MODE
Write:	▨	▨	▨	▨	▨	ACK		
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 8-4. IRQ Status and Control Register (INTSCR)

IRQF — IRQ Flag
This read-only status bit is high when the IRQ interrupt is pending.
1 = $\overline{\text{IRQ}}$ interrupt pending
0 = $\overline{\text{IRQ}}$ interrupt not pending

ACK — IRQ Interrupt Request Acknowledge Bit
Writing a 1 to this write-only bit clears the IRQ latch. ACK always reads as 0. Reset clears ACK.

IMASK — IRQ Interrupt Mask Bit
Writing a 1 to this read/write bit disables IRQ interrupt requests. Reset clears IMASK.
1 = IRQ interrupt requests disabled
0 = IRQ interrupt requests enabled

MODE — IRQ Edge/Level Select Bit
This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin. Reset clears MODE.
1 = $\overline{\text{IRQ}}$ interrupt requests on falling edges and low levels
0 = $\overline{\text{IRQ}}$ interrupt requests on falling edges only

Section 9. Keyboard Interrupt Module (KBI)

9.1 Introduction

The keyboard interrupt module (KBI) provides six independently maskable external interrupts, which are accessible via the PTA0–PTA5 pins.

9.2 Features

Features of the keyboard interrupt module include:

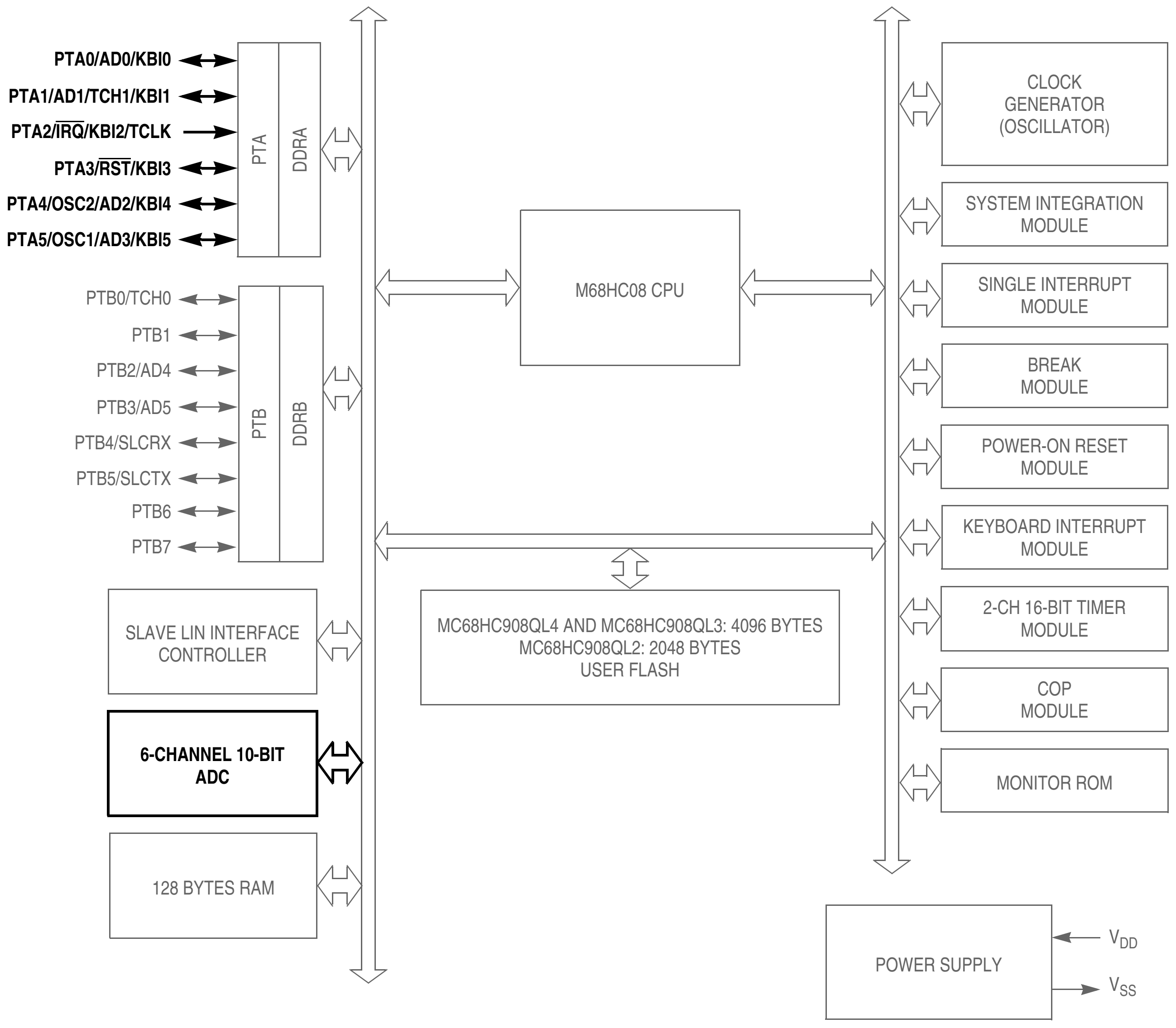
- Six keyboard interrupt pins with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Software configurable pullup device if input pin is configured as input port bit
- Programmable edge-only or edge and level interrupt sensitivity
- Exit from low-power modes

Figure 9-1 provides a summary of the input/output (I/O) registers

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001A	Keyboard Status and Control Register (KBSCR)	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:	▨	▨	▨	▨	▨	ACKK		
	See page 96.	Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (KBIER)	Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:	▨							
	See page 97.	Reset:	0	0	0	0	0	0	0	0

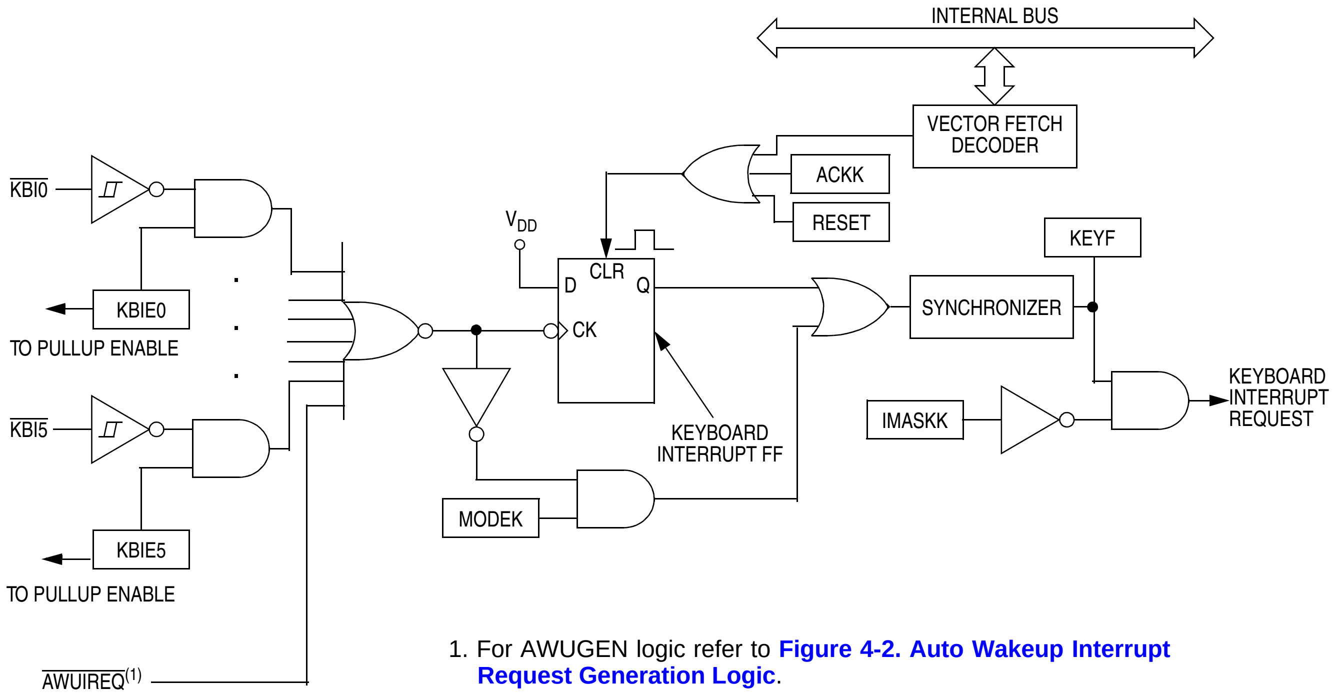
▨ = Unimplemented

Figure 9-1. KBI I/O Register Summary



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30 kΩ) pull up
PTA0, PTA1, PTA3–PTA5: High current sink and source capability
PTA0–PTA5: Pins have programmable keyboard interrupt and pull up
ADC pins only available on MC68HC908QL4 and MC68HC908QL2

Figure 9-2. Block Diagram Highlighting KBI Block and Pins



1. For AWUGEN logic refer to **Figure 4-2. Auto Wakeup Interrupt Request Generation Logic**.

Figure 9-3. Keyboard Interrupt Block Diagram

9.3 Functional Description

The keyboard interrupt module controls the enabling/disabling of interrupt functions on the six port A pins. These six pins can be enabled/disabled independently of each other.

9.3.1 Keyboard Operation

Writing to the KBIE0–KBIE5 bits in the keyboard interrupt enable register (KBIER) independently enables or disables each port A pin as a keyboard interrupt pin. Enabling a keyboard interrupt pin in port A also enables its internal pullup device irrespective of PTAPUEx bits in the port A input pullup enable register (see **12.2.3 Port A Input Pullup Enable Register**). A logic 0 applied to an enabled keyboard interrupt pin latches a keyboard interrupt request.

A keyboard interrupt is latched when one or more keyboard interrupt inputs goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering mode of the keyboard interrupt.

- If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard interrupt input does not latch an interrupt request if another keyboard pin is already low. To prevent losing an interrupt request on one input because another input is still low, software can disable the latter input while it is low.
- If the keyboard interrupt is falling edge and low-level sensitive, an interrupt request is present as long as any keyboard interrupt input is low.

If the MODEK bit is set, the keyboard interrupt inputs are both falling edge and low-level sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKK bit in the keyboard status and control register (KBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt inputs and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt inputs. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the central processor unit (CPU) loads the program counter with the vector address at locations $FFE0 and $FFE1.
- Return of all enabled keyboard interrupt inputs to logic 1 — As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set. The auto wakeup interrupt input, AWUIREQ, will be cleared only by writing to ACKK bit in KBSCR or reset.

The vector fetch or software clear and the return of all enabled keyboard interrupt pins to logic 1 may occur in any order.

If the MODEK bit is clear, the keyboard interrupt pin is falling-edge sensitive only. With MODEK clear, a vector fetch or software clear immediately clears the keyboard interrupt request.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt input stays at logic 0.

The keyboard flag bit (KEYF) in the keyboard status and control register can be used to see if a pending interrupt exists. The KEYF bit is not affected by the keyboard interrupt mask bit (IMASKK) which makes it useful in applications where polling is preferred.

To determine the logic level on a keyboard interrupt pin, use the data direction register to configure the pin as an input and then read the data register.

NOTE: *Setting a keyboard interrupt enable bit (KBIEx) forces the corresponding keyboard interrupt pin to be an input, overriding the data direction register. However, the data direction register bit must be a 0 for software to read the pin.*

9.3.2 Keyboard Initialization

When a keyboard interrupt pin is enabled, it takes time for the internal pullup to reach a logic 1. Therefore a false interrupt can occur as soon as the pin is enabled.

To prevent a false interrupt on keyboard initialization:

1. Mask keyboard interrupts by setting the IMASKK bit in the keyboard status and control register.
2. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.
3. Write to the ACKK bit in the keyboard status and control register to clear any false interrupts.
4. Clear the IMASKK bit.

An interrupt signal on an edge-triggered pin can be acknowledged immediately after enabling the pin. An interrupt signal on an edge- and level-triggered interrupt pin must be acknowledged after a delay that depends on the external load.

Another way to avoid a false interrupt:

1. Configure the keyboard pins as outputs by setting the appropriate DDRA bits in the data direction register A.
2. Write 1s to the appropriate port A data register bits.
3. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.

9.4 Wait Mode

The keyboard module remains active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

9.5 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

9.6 Keyboard Module During Break Interrupts

The system integration module (SIM) controls whether the keyboard interrupt latch can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state.

To allow software to clear the keyboard interrupt latch during a break interrupt, write a 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latch during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect.

9.7 Input/Output Registers

The following I/O registers control and monitor operation of the keyboard interrupt module:

- Keyboard interrupt status and control register (KBSCR)
- Keyboard interrupt enable register (KBIER)

9.7.1 Keyboard Status and Control Register

The keyboard status and control register (KBSCR):

- Flags keyboard interrupt requests
- Acknowledges keyboard interrupt requests
- Masks keyboard interrupt requests
- Controls keyboard interrupt triggering sensitivity

Address: $001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
Write:	▨	▨	▨	▨	▨	ACKK		
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 9-4. Keyboard Status and Control Register (KBSCR)

Bits 7–4 — Not used
These read-only bits always read as 0s.

KEYF — Keyboard Flag Bit
This read-only bit is set when a keyboard interrupt is pending on port A or auto wakeup. Reset clears the KEYF bit.
1 = Keyboard interrupt pending
0 = No keyboard interrupt pending

ACKK — Keyboard Acknowledge Bit
Writing a 1 to this write-only bit clears the keyboard interrupt request on port A and auto wakeup logic. ACKK always reads as 0. Reset clears ACKK.

IMASKK— Keyboard Interrupt Mask Bit
Writing a 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests on port A or auto wakeup. Reset clears the IMASKK bit.
1 = Keyboard interrupt requests masked
0 = Keyboard interrupt requests not masked

MODEK — Keyboard Triggering Sensitivity Bit

This read/write bit controls the triggering sensitivity of the keyboard interrupt pins on port A and auto wakeup. Reset clears MODEK.

1 = Keyboard interrupt requests on falling edges and low levels
0 = Keyboard interrupt requests on falling edges only

9.7.2 Keyboard Interrupt Enable Register

The port A keyboard interrupt enable register (KBIER) enables or disables each port A pin or auto wakeup to operate as a keyboard interrupt input.

Address: $001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	AWUIE	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
Write:	▨							
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 9-5. Keyboard Interrupt Enable Register (KBIER)

KBIE5–KBIE0 — Port A Keyboard Interrupt Enable Bits

Each of these read/write bits enables the corresponding keyboard interrupt pin on port A to latch interrupt requests. Reset clears the keyboard interrupt enable register.

1 = KBIx pin enabled as keyboard interrupt pin
0 = KBIx pin not enabled as keyboard interrupt pin

NOTE: *AWUIE bit is not used in conjunction with the keyboard interrupt feature. To see a description of this bit, see* **Section 4. Auto Wakeup Module (AWU)**.

Section 10. Low-Voltage Inhibit (LVI)

10.1 Introduction

This section describes the low-voltage inhibit (LVI) module, which monitors the voltage on the V_{DD} pin and can force a reset when the V_{DD} voltage falls below the LVI trip falling voltage, V_{TRIPF}.

10.2 Features

Features of the LVI module include:

- Programmable LVI reset
- Programmable power consumption
- Selectable LVI trip voltage
- Programmable stop mode operation

10.3 Functional Description

Figure 10-1 shows the structure of the LVI module. LVISTOP, LVIPWRD, LVI5OR3, and LVIRSTD are user selectable options found in the configuration register (CONFIG1). See **Section 5. Configuration Register (CONFIG)**.

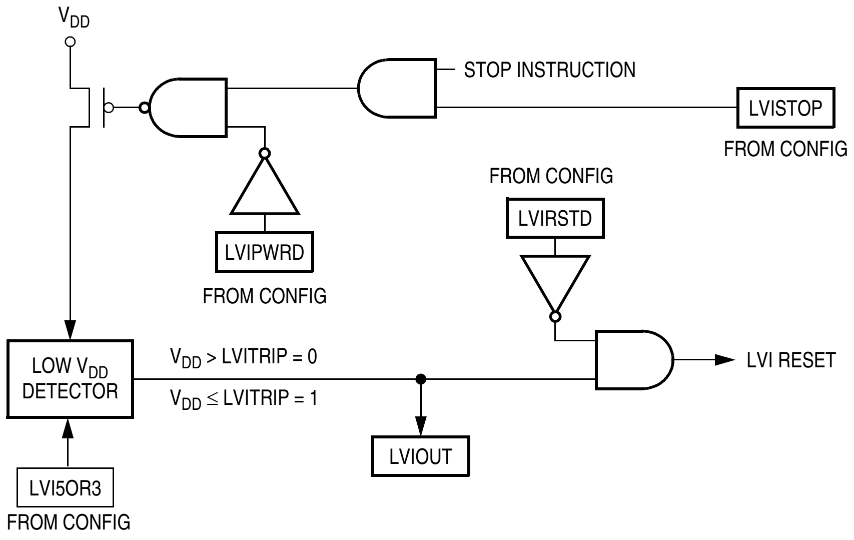


Figure 10-1. LVI Module Block Diagram

The LVI is enabled out of reset. The LVI module contains a bandgap reference circuit and comparator. Clearing the LVI power disable bit, LVIPWRD, enables the LVI to monitor V_{DD} voltage. Clearing the LVI reset disable bit, LVIRSTD, enables the LVI module to generate a reset when V_{DD} falls below a voltage, V_{TRIPF}. Setting the LVI enable in stop mode bit, LVISTOP, enables the LVI to operate in stop mode. Setting the LVI 5-V or 3-V trip point bit, LVI5OR3, enables the trip point voltage, V_{TRIPF}, to be configured for 5-V operation. Clearing the LVI5OR3 bit enables the trip point voltage, V_{TRIPF}, to be configured for 3-V operation. The actual trip thresholds are specified in **17.5 5-V DC Electrical Characteristics** and **17.9 3.3-V DC Electrical Characteristics**.

NOTE: *After a power-on reset, the LVI's default mode of operation is 3 volts. If a 5-V system is used, the user must set the LVI5OR3 bit to raise the trip point to 5-V operation.*

If the user requires 5-V mode and sets the LVI5OR3 bit after power-on reset while the V_{DD} supply is not above the V_{TRIPR} for 5-V mode, the microcontroller unit (MCU) will immediately go into reset. The next time the LVI releases the reset, the supply will be above the V_{TRIPR} for 5-V mode.

Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR}, which causes the MCU to exit reset. See **Section 13. System Integration Module (SIM)** for the reset recovery sequence.

The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR) and can be used for polling LVI operation when the LVI reset is disabled.

10.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be at 0 to enable the LVI module, and the LVIRSTD bit must be at 1 to disable LVI resets.

10.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, the LVIPWRD and LVIRSTD bits must be at 0 to enable the LVI module and to enable LVI resets.

10.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the LVI will maintain a reset condition until V_{DD} rises above the rising trip point voltage, V_{TRIPR}. This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF}. V_{TRIPR} is greater than V_{TRIPF} by the hysteresis voltage, V_{HYS}.

10.3.4 LVI Trip Selection

The LVI5OR3 bit in the configuration register selects whether the LVI is configured for 5-V or 3-V protection.

NOTE: *The microcontroller is guaranteed to operate at a minimum supply voltage. The trip point (V_{TRIPF} [5 V] or V_{TRIPF} [3 V]) may be lower than this. See* ***17.5 5-V DC Electrical Characteristics*** *and* ***17.9 3.3-V DC Electrical Characteristics*** *for the actual trip point voltages.*

10.4 LVI Status Register

The LVI status register (LVISR) indicates if the V_{DD} voltage was detected below the V_{TRIPF} level while LVI resets have been disabled.

Address: $FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	R
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented   R = Reserved

Figure 10-2. LVI Status Register (LVISR)

LVIOUT — LVI Output Bit

This read-only flag becomes set when the V_{DD} voltage falls below the V_{TRIPF} trip voltage and is cleared when V_{DD} voltage rises above V_{TRIPR}. The difference in these threshold levels results in a hysteresis that prevents oscillation into and out of reset (see **Table 10-1**). Reset clears the LVIOUT bit.

Table 10-1. LVIOUT Bit Indication

V_{DD}	LVIOUT
$V_{DD} > V_{TRIPR}$	0
$V_{DD} < V_{TRIPF}$	1
$V_{TRIPF} < V_{DD} < V_{TRIPR}$	Previous value

10.5 LVI Interrupts

The LVI module does not generate interrupt requests.

10.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby modes.

10.6.1 Wait Mode

If enabled, the LVI module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

10.6.2 Stop Mode

When the LVIPWRD bit in the configuration register is cleared and the LVISTOP bit in the configuration register is set, the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

Section 11. Oscillator Module (OSC)

11.1 Introduction

The oscillator module is used to provide a stable clock source for the microcontroller system and bus. The oscillator module generates two output clocks, BUSCLKX2 and BUSCLKX4. The BUSCLKX4 clock is used by the system integration module (SIM) and the computer operating properly module (COP). The BUSCLKX2 clock is divided by two in the SIM to be used as the bus clock for the microcontroller. Therefore the bus frequency will be one forth of the BUSCLKX4 frequency.

11.2 Features

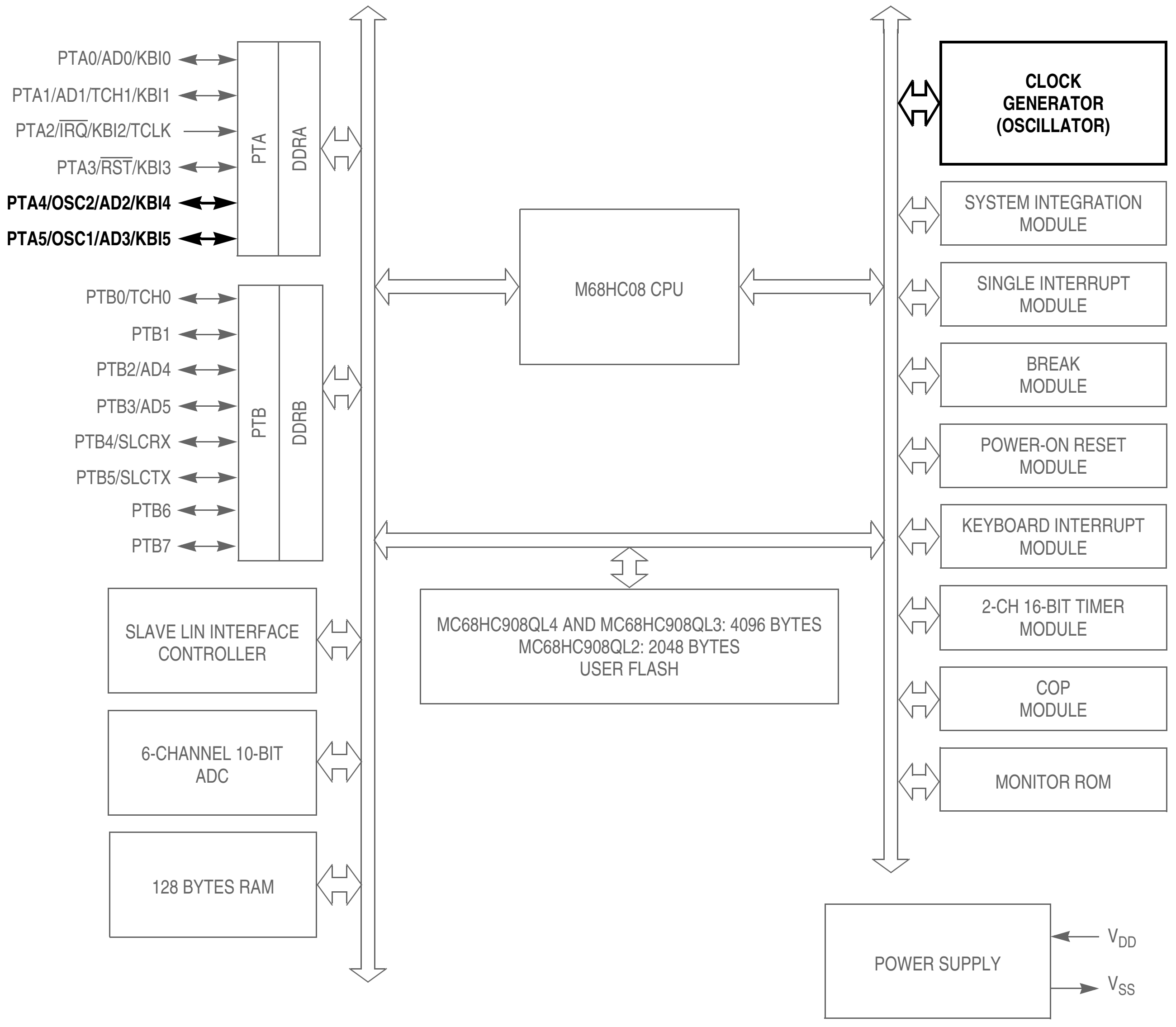
The oscillator has these four clock source options available:

1. Internal oscillator: An internally generated, fixed frequency clock, trimmable to ± 5%. This is the default option out of reset.
2. External oscillator: An external clock that can be driven directly into OSC1.
3. External RC: A built-in oscillator module (RC oscillator) that requires an external R connection only. The capacitor is internal to the chip.
4. External crystal: A built-in oscillator module (XTAL oscillator) that requires an external crystal or ceramic-resonator.

11.3 Functional Description

The oscillator contains these major subsystems:

- Internal oscillator circuit
- Internal or external clock switch control
- External clock circuit
- External crystal circuit
- External RC clock circuit



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30 kΩ) pull up
PTA0, PTA1, PTA3–PTA5: High current sink and source capability
PTA0–PTA5: Pins have programmable keyboard interrupt and pull up
ADC pins only available on MC68HC908QL4 and MC68HC908QL2

Figure 11-1. Block Diagram Highlighting OSC Block and Pins

11.3.1 Internal Oscillator

The internal oscillator circuit is designed for use with no external components to provide a clock source with tolerance less than ±25% untrimmed. An 8-bit trimming register allows the adjust to a tolerance of less than ±5%.

The internal oscillator will generate a clock of 25.6 MHz typical (INTCLK) resulting in a maximum bus speed (internal clock ÷ 4) of 6.4 MHz. The bus clock is software selectable to be 3.2 MHz, which is the default frequency after reset. The 3.2 MHz selection is required for applications running at 3.3 V. The maximum frequency at 5 V is 8 MHz, since the internal oscillator will have a ±25% tolerance (pre-trim), then the +25% case should not allow a frequency higher than 8 MHz:

6.4 MHz + 25% = 8 MHz for 5 V operation
3.2 MHz + 25% = 4 MHz for 3.3 V operation

Figure 11-3 shows how BUSCLKX4 is derived from INTCLK and, like the RC oscillator, OSC2 can output BUSCLKX4 by setting OSC2EN in PTAPUE register. See **Section 12. Input/Output Ports (PORTS)**.

11.3.1.1 Internal Oscillator Trimming

The 8-bit trimming register, OSCTRIM, allows a clock period adjust of +127 and –128 steps. Increasing OSCTRIM value increases the clock period. Trimming allows the internal clock frequency to be set to 25.6 MHz ± 5%.

There’s an option to order a trimmed version of MC68HC908QL4. The trimming value will be provided in a known FLASH location, $FFC0. So that the user would be able to copy this byte from the FLASH to the OSCTRIM register right at the beginning of assembly code.

Reset loads OSCTRIM with a default value of $80.

11.3.1.2 Internal to External Clock Switching

When external clock source (external OSC, RC, or XTAL) is desired, the user must perform the following steps:

1. For external crystal circuits only, OSCOPT[1:0] = 1:1: To help precharge an external crystal oscillator, set PTA4 (OSC2) as an output and drive high for several cycles. This may help the crystal circuit start more robustly.
2. Set CONFIG2 bits OSCOPT[1:0] according to **Table 11-2**. The oscillator module control logic will then set OSC1 as an external clock input and, if the external crystal option is selected, OSC2 will also be set as the clock output.
3. Create a software delay to wait the stabilization time needed for the selected clock source (crystal, resonator, RC) as recommended by the component manufacturer. A good rule of thumb for crystal oscillators is to wait 4096 cycles of the crystal frequency, i.e., for a 4-MHz crystal, wait approximately 1 ms.

4. After the manufacturer's recommended delay has elapsed, the ECGON bit in the OSC status register (OSCSTAT) needs to be set by the user software.
5. After ECGON set is detected, the OSC module checks for oscillator activity by waiting two external clock rising edges.
6. The OSC module then switches to the external clock. Logic provides a glitch free transition.
7. The OSC module first sets the ECGST bit in the OSCSTAT register and then stops the internal oscillator.

NOTE: *Once transition to the external clock is done, the internal oscillator will only be reactivated with reset. No post-switch clock monitor feature is implemented (clock does not switch back to internal if external clock dies).*

11.3.2 External Oscillator

The external clock option is designed for use when a clock signal is available in the application to provide a clock source to the microcontroller. The OSC1 pin is enabled as an input by the oscillator module. The clock signal is used directly to create BUSCLKX4 and also divided by two to create BUSCLKX2.

In this configuration, the OSC2 pin cannot output BUSCLKX4. So the OSC2EN bit in the port A pullup enable register will be clear to enable PTA4 I/O functions on the pin.

11.3.3 XTAL Oscillator

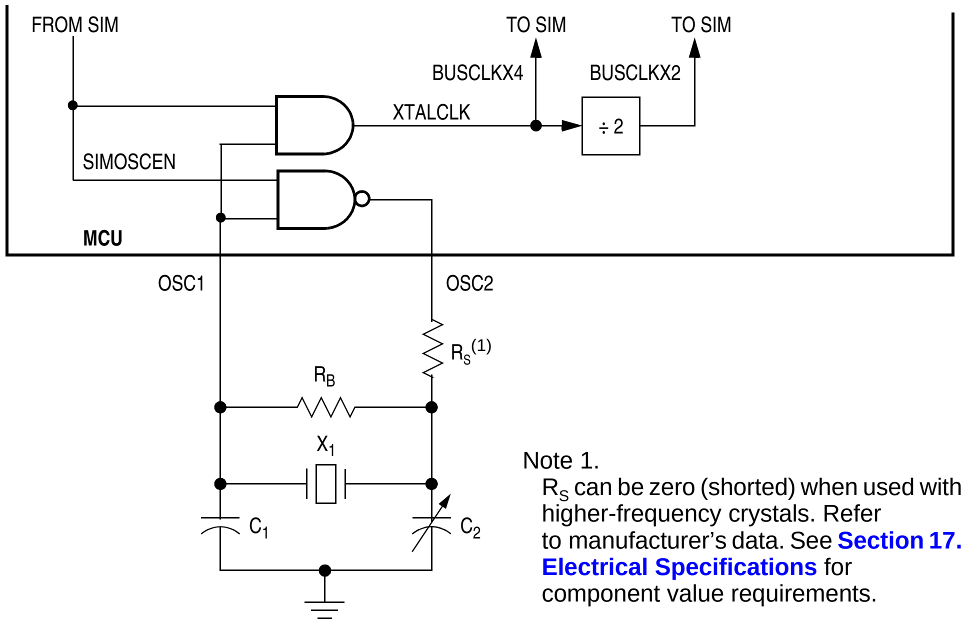
The XTAL oscillator circuit is designed for use with an external crystal or ceramic resonator to provide an accurate clock source. In this configuration, the OSC2 pin is dedicated to the external crystal circuit. The OSC2EN bit in the port A pullup enable register has no effect when this clock mode is selected.

In its typical configuration, the XTAL oscillator is connected in a Pierce oscillator configuration, as shown in **Figure 11-2**. This figure shows only the logical representation of the internal components and may not represent actual circuitry.

The oscillator configuration uses five components:

- Crystal, X_1
- Fixed capacitor, C_1
- Tuning capacitor, C_2 (can also be a fixed capacitor)
- Feedback resistor, R_B
- Series resistor, R_S (optional)

NOTE: *The series resistor (R_S) is included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals. Refer to the crystal manufacturer's data for more information.*



Note 1.
R_S can be zero (shorted) when used with higher-frequency crystals. Refer to manufacturer's data. See **Section 17. Electrical Specifications** for component value requirements.

Figure 11-2. XTAL Oscillator External Connections

11.3.4 RC Oscillator

The RC oscillator circuit is designed for use with external R to provide a clock source with tolerance less than 25%.

In its typical configuration, the RC oscillator requires two external components, one R and one C. In the MC68HC908QL4, the capacitor is internal to the chip. The R value should have a tolerance of 1% or less, to obtain a clock source with less than 25% tolerance. The oscillator configuration uses one component, R_{EXT}.

In this configuration, the OSC2 pin can be left in the reset state as PTA4. Or, the OSC2EN bit in the port A pullup enable register can be set to enable the OSC2 output function on the pin. Enabling the OSC2 output slightly increases the external RC oscillator frequency, f_{RCCLK}. See **Figure 11-3**.

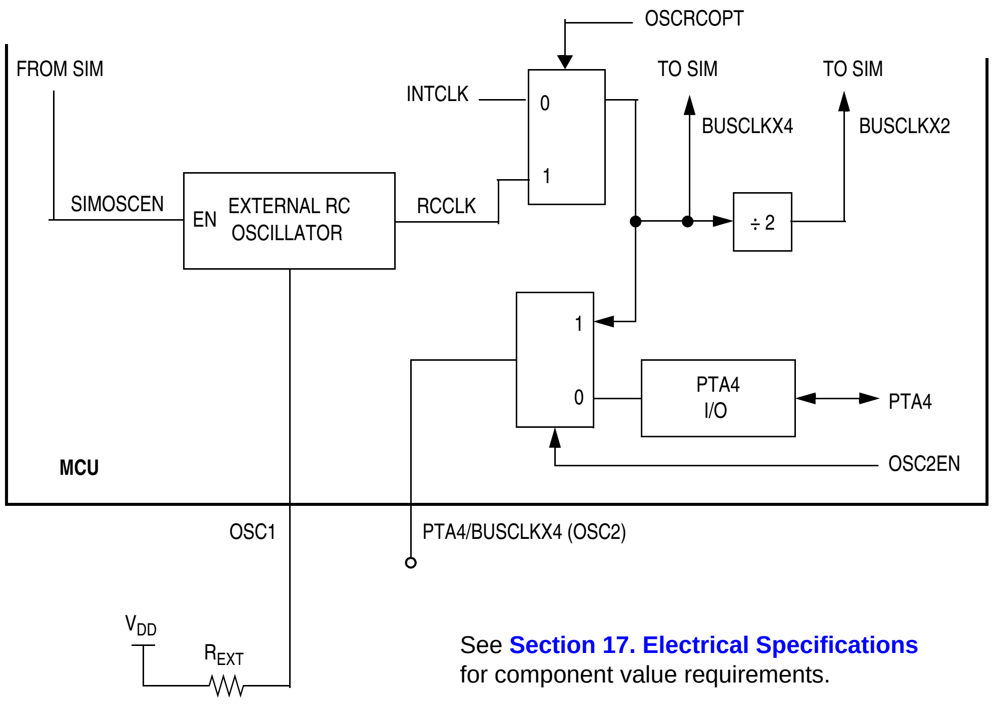
11.4 Oscillator Module Signals

The following paragraphs describe the signals that are inputs to and outputs from the oscillator module.

11.4.1 Crystal Amplifier Input Pin (OSC1)

The OSC1 pin is either an input to the crystal oscillator amplifier, an input to the RC oscillator circuit, or an external clock source.

For the internal oscillator configuration, the OSC1 pin can assume other functions according to **Table 1-3. Function Priority in Shared Pins**.



See **Section 17. Electrical Specifications** for component value requirements.

Figure 11-3. RC Oscillator External Connections

11.4.2 Crystal Amplifier Output Pin (OSC2/PTA4/BUSCLKX4)

For the XTAL oscillator device**,** the OSC2 pin is the crystal oscillator inverting amplifier output.

For the external clock option, the OSC2 pin is dedicated to the PTA4 I/O function. The OSC2EN bit has no effect.

For the internal oscillator or RC oscillator options, the OSC2 pin can assume other functions according to **Table 1-3. Function Priority in Shared Pins**, or the output of the oscillator clock (BUSCLKX4).

Table 11-1. OSC2 Pin Function

Option	OSC2 Pin Function
XTAL oscillator	Inverting OSC1
External clock	PTA4 I/O

Internal oscillator
or
RC oscillator
	Controlled by OSC2EN bit in PTAPUE register
	OSC2EN = 0: PTA4 I/O
	OSC2EN = 1: BUSCLKX4 output

11.4.3 Oscillator Enable Signal (SIMOSCEN)

The SIMOSCEN signal comes from the system integration module (SIM) and enables/disables either the XTAL oscillator circuit, the RC oscillator, or the internal oscillator.

11.4.4 XTAL Oscillator Clock (XTALCLK)

XTALCLK is the XTAL oscillator output signal. It runs at the full speed of the crystal (f_{XCLK}) and comes directly from the crystal oscillator circuit. **Figure 11-2** shows only the logical relation of XTALCLK to OSC1 and OSC2 and may not represent the actual circuitry. The duty cycle of XTALCLK is unknown and may depend on the crystal and other external factors. Also, the frequency and amplitude of XTALCLK can be unstable at start up.

11.4.5 RC Oscillator Clock (RCCLK)

RCCLK is the RC oscillator output signal. Its frequency is directly proportional to the time constant of external R and internal C. **Figure 11-3** shows only the logical relation of RCCLK to OSC1 and may not represent the actual circuitry.

11.4.6 Internal Oscillator Clock (INTCLK)

INTCLK is the internal oscillator output signal. INTCLK is software selectable to be 12.8 MHz or 25.6 MHz, but it can also trimmed using the oscillator trimming feature of the OSCTRIM register (see **11.3.1.1 Internal Oscillator Trimming**).

11.4.7 Oscillator Out 2 (BUSCLKX4)

BUSCLKX4 is the same as the input clock (XTALCLK, RCCLK, or INTCLK). This signal is driven to the SIM module and is used to determine the COP cycles.

11.4.8 Oscillator Out (BUSCLKX2)

The frequency of this signal is equal to half of the BUSCLKX4, this signal is driven to the SIM for generation of the bus clocks used by the CPU and other modules on the MCU. BUSCLKX2 will be divided again in the SIM and results in the internal bus frequency being one fourth of either the XTALCLK, RCCLK, or INTCLK frequency.

11.5 Low Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

11.5.1 Wait Mode

The WAIT instruction has no effect on the oscillator logic. BUSCLKX2 and BUSCLKX4 continue to drive to the SIM module.

11.5.2 Stop Mode

The STOP instruction disables either the XTALCLK, the RCCLK, or INTCLK output, hence BUSCLKX2 and BUSCLKX4.

11.6 Oscillator During Break Mode

The oscillator continues to drive BUSCLKX2 and BUSCLKX4 when the device enters the break state.

11.7 CONFIG2 Options

Two CONFIG2 register options affect the operation of the oscillator module: OSCOPT1 and OSCOPT0. All CONFIG2 register bits will have a default configuration. Refer to **Section 5. Configuration Register (CONFIG)** for more information on how the CONFIG2 register is used.

Table 11-2 shows how the OSCOPT bits are used to select the oscillator clock source.

Table 11-2. Oscillator Modes

OSCOPT1	OSCOPT0	Oscillator Modes
0	0	Internal oscillator
0	1	External oscillator
1	0	External RC
1	1	External crystal

11.8 Input/Output (I/O) Registers

The oscillator module contains these two registers:

1. Oscillator status register (OSCSTAT)
2. Oscillator trim register (OSCTRIM)

11.8.1 Oscillator Status Register

The oscillator status register (OSCSTAT) contains the bits for switching from internal to external clock sources.

Address: $0036

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	BFS	ECGON	ECGST
Write:	R	R	R	R	R	BFS	ECGON	▨
Reset:	0	0	0	0	0	0	0	0

R = Reserved   ▨ = Unimplemented

Figure 11-4. Oscillator Status Register (OSCSTAT)

BFS — Bus Frequency Select Bit
This read/write bit enables the bus frequency to be increased for 5-V applications from 3.2 MHz to 6.4 MHz when running off the internal oscillator.
1 = 6.4 MHz Bus Frequency
0 = 3.2 MHz Bus Frequency

ECGON — External Clock Generator On Bit
This read/write bit enables external clock generator, so that the switching process can be initiated. This bit is forced low during reset. This bit is ignored in monitor mode with the internal oscillator bypassed, PTM or CTM mode.
1 = External clock generator enabled
0 = External clock generator disabled

ECGST — External Clock Status Bit
This read-only bit indicates whether or not an external clock source is engaged to drive the system clock.
1 = An external clock source engaged
0 = An external clock source disengaged

11.8.2 Oscillator Trim Register (OSCTRIM)

Address: $0038

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
Reset:	1	0	0	0	0	0	0	0

Figure 11-5. Oscillator Trim Register (OSCTRIM)

TRIM7–TRIM0 — Internal Oscillator Trim Factor Bits

These read/write bits change the size of the internal capacitor used by the internal oscillator. By measuring the period of the internal clock and adjusting this factor accordingly, the frequency of the internal clock can be fine tuned. Increasing (decreasing) this factor by one increases (decreases) the period by approximately 0.2% of the untrimmed period (the period for TRIM = $80). The trimmed frequency is guaranteed not to vary by more than ±5% over the full specified range of temperature and voltage. The reset value is $80, which sets the frequency to 12.8 MHz (3.2 MHz bus speed, provided BFS = 0) ±25%.

Section 12. Input/Output Ports (PORTS)

12.1 Introduction

MC68HC908QL4, MC68HC908QL3, MC68HC908QL2, and MC68HC908QL4 have thirteen bidirectional pins and one input only pin. All input/output (I/O) pins are programmable as inputs or outputs.

NOTE: *Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

Figure 12-1 provides a summary of the I/O registers.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 114.	Read:	0	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:	▨	▨				▨		
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PTB) See page 117.	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
$0004	Data Direction Register A (DDRA) See page 115.	Read:	0	0	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
		Write:	▨	▨				▨		
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 117.	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000B	Port A Input Pullup Enable Register (PTAPUE) See page 116.	Read:	OSC2EN	▨	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:		▨						
		Reset:	0	0	0	0	0	0	0	0
$000C	Port B Input Pullup Enable Register (PTBPUE) See page 119.	Read:	PTBPUE7	PTBPUE6	PTBPUE5	PTBPUE4	PTBPUE3	PTBPUE2	PTBPUE1	PTBPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 12-1. I/O Port Register Summary

12.2 Port A

Port A is an 6-bit special function port that shares all six of its pins with the keyboard interrupt (KBI) module (see **Section 9. Keyboard Interrupt Module (KBI)**). Each port A pin also has a software configurable pullup device if the corresponding port pin is configured as an input port.

NOTE: *PTA2 is input only. PTA0, PTA1, PTA4, and PTA5 can also serve as ESCI pins*

When the $\overline{IRQ}$ function is enabled in the configuration register 2 (CONFIG2), bit 2 of the port A data register (PTA) will always read a 0. In this case, the BIH and BIL instructions can be used to read the logic level on the PTA2 pin. When the $\overline{IRQ}$ function is disabled, these instructions will behave as if the PTA2 pin is a logic 1. However, reading bit 2 of PTA will read the actual logic level on the pin.

12.2.1 Port A Data Register

The port A data register (PTA) contains a data latch for each of the six port A pins.

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
Write:	▨	▨				▨		
Reset:	Unaffected by reset							
Additional Functions:	▨	▨	KBI5	KBI4	KBI3	KBI2	KBI1	KBI0

▨ = Unimplemented

Figure 12-2. Port A Data Register (PTA)

PTA[5:0] — Port A Data Bits
These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

AWUL — Auto Wakeup Latch Data Bit
This is a read-only bit which has the value of the auto wakeup interrupt request latch. The wakeup request signal is generated internally. There is no PTA6 port nor any of the associated bits such as PTA6 data register, pullup enable or direction. See **Section 4. Auto Wakeup Module (AWU)**

KBI[5:0] — Port A Keyboard Interrupts
The keyboard interrupt enable bits, KBIE5–KBIE0, in the keyboard interrupt control enable register (KBIER) enable the port A pins as external interrupt pins. See **Section 9. Keyboard Interrupt Module (KBI)**.

12.2.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output. Writing a 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a 0 disables the output buffer.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
Write:	▨	▨				▨		
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 12-3. Data Direction Register A (DDRA)

DDRA[5:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[5:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE: *Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.*

Figure 12-4 shows the port A I/O logic.

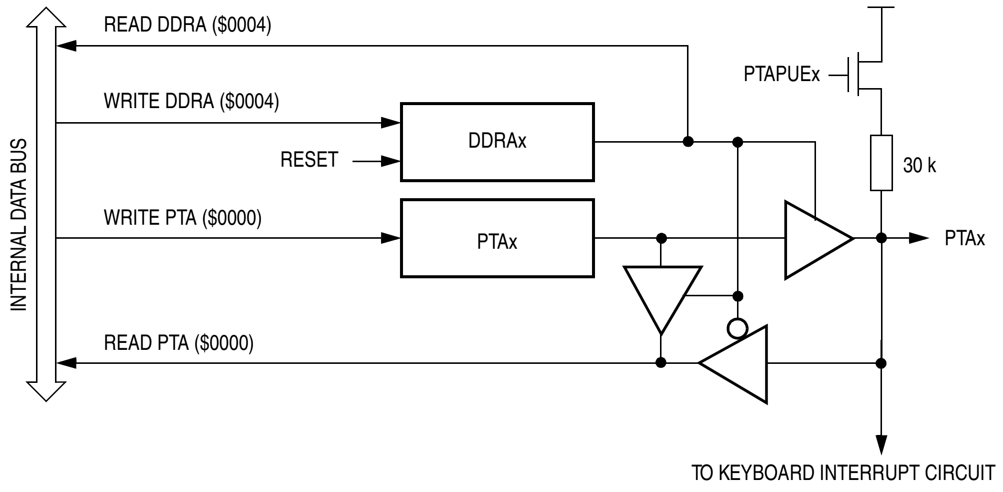


Figure 12-4. Port A I/O Circuit

NOTE: *Figure 12-4 does not apply to PTA2*

When DDRAx is a 1, reading address $0000 reads the PTAx data latch. When DDRAx is a 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

12.2.3 Port A Input Pullup Enable Register

The port A input pullup enable register (PTAPUE) contains a software configurable pullup device for each if the six port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx, to be configured as input. Each pullup device is automatically and dynamically disabled when its corresponding DDRAx bit is configured as output.

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OSC2EN	▨	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE2	PTAPUE0
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 12-5. Port A Input Pullup Enable Register (PTAPUE)

OSC2EN — Enable PTA4 on OSC2 Pin

This read/write bit configures the OSC2 pin function when internal oscillator or RC oscillator option is selected. This bit has no effect for the XTAL or external oscillator options.

1 = OSC2 pin outputs the internal or RC oscillator clock (BUSCLKX4)

0 = OSC2 pin configured for PTA4 I/O, having all the interrupt and pullup functions

PTAPUE[5:0] — Port A Input Pullup Enable Bits

These read/write bits are software programmable to enable pullup devices on port A pins.

1 = Corresponding port A pin configured to have internal pull if its DDRA bit is set to 0

0 = Pullup device is disconnected on the corresponding port A pin regardless of the state of its DDRA bit

Table 12-1 summarizes the operation of the port A pins.

Table 12-1. Port A Pin Functions

PTAPUE Bit	DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
				Read/Write	Read	Write
1	0	X(1)	Input, V_{DD}(2)	DDRA5–DDRA0	Pin	PTA5–PTA0(3)
0	0	X	Input, Hi-Z(4)	DDRA5–DDRA0	Pin	PTA5–PTA0(3)
X	1	X	Output	DDRA5–DDRA0	PTA5–PTA0	PTA5–PTA0(5)

1. X = don't care
2. I/O pin pulled to V_{DD} by internal pullup.
3. Writing affects data register, but does not affect input.
4. Hi-Z = high impedance
5. Output does not apply to PTA2

12.3 Port B

Port B is an 8-bit general purpose I/O port. Port B is only available on the MC68HC908QL4, MC68HC908QL3, and MC68HC908QL2.

12.3.1 Port B Data Register

The port B data register (PTB) contains a data latch for each of the eight port B pins.

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
Reset:	Unaffected by reset							

Figure 12-6. Port B Data Register (PTB)

PTB[7:0] — Port B Data Bits

These read/write bits are software programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

12.3.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output. Writing a 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a 0 disables the output buffer.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Reset:	0	0	0	0	0	0	0	0

Figure 12-7. Data Direction Register B (DDRB)

DDRB[7:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[7:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE: *Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.* ***Figure 12-8*** *shows the port B I/O logic.*

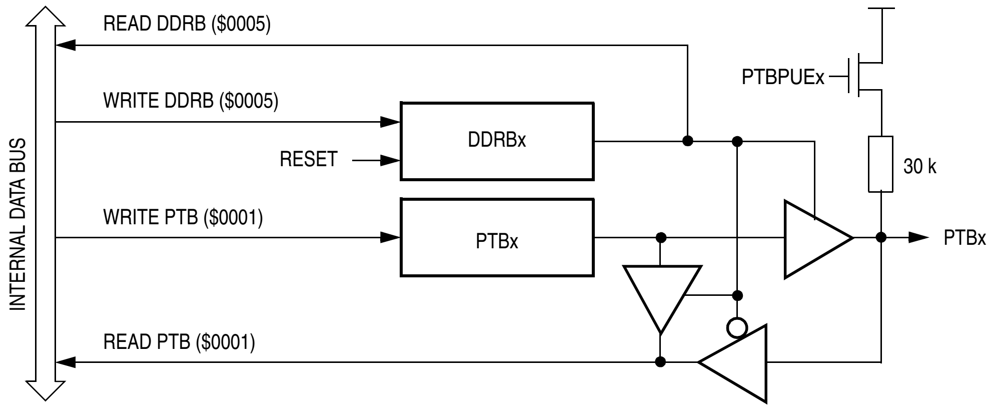


Figure 12-8. Port B I/O Circuit

When DDRBx is a 1, reading address $0001 reads the PTBx data latch. When DDRBx is a 0, reading address $0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 12-2** summarizes the operation of the port B pins.

Table 12-2. Port B Pin Functions

DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
			Read/Write	Read	Write
0	X[(1)]	Input, Hi-Z[(2)]	DDRB7–DDRB0	Pin	PTB7–PTB0[(3)]
1	X	Output	DDRB7–DDRB0	Pin	PTB7–PTB0

1. X = don't care
2. Hi-Z = high impedance
3. Writing affects data register, but does not affect the input.

12.3.3 Port B Input Pullup Enable Register

The port B input pullup enable register (PTBPUE) contains a software configurable pullup device for each of the eight port B pins. Each bit is individually configurable and requires the corresponding data direction register, DDRBx, be configured as input. Each pullup device is automatically and dynamically disabled when its corresponding DDRBx bit is configured as output.

Address: $000C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTBPUE7	PTBPUE6	PTBPUE5	PTBPUE4	PTBPUE3	PTBPUE2	PTBPUE2	PTBPUE0
Reset:	0	0	0	0	0	0	0	0

Figure 12-9. Port B Input Pullup Enable Register (PTBPUE)

PTBPUE[7:0] — Port B Input Pullup Enable Bits

These read/write bits are software programmable to enable pullup devices on port B pins

1 = Corresponding port B pin configured to have internal pull if its DDRB bit is set to 0

0 = Pullup device is disconnected on the corresponding port B pin regardless of the state of its DDRB bit.

Table 12-3 summarizes the operation of the port B pins.

Table 12-3. Port B Pin Functions

PTBPUE Bit	DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
				Read/Write	Read	Write
1	0	X[(1)]	Input, V_{DD}[(2)]	DDRB7–DDRB0	Pin	PTB7–PTB0[(3)]
0	0	X	Input, Hi-Z[(4)]	DDRB7–DDRB0	Pin	PTB7–PTB0[(3)]
X	1	X	Output	DDRB7–DDRB0	PTB7–PTB0	PTB7–PTB0

1. X = don't care
2. I/O pin pulled to V_{DD} by internal pullup.
3. Writing affects data register, but does not affect input.
4. Hi-Z = high impedance

Section 13. System Integration Module (SIM)

13.1 Introduction

This section describes the system integration module (SIM), which supports up to 24 external and/or internal interrupts. Together with the central processor unit (CPU), the SIM controls all microcontroller unit (MCU) activities. A block diagram of the SIM is shown in **Figure 13-1**. **Figure 13-2** is a summary of the SIM I/O registers. The SIM is a system state controller that coordinates CPU and exception timing.

The SIM is responsible for:

- Bus clock generation and control for CPU and peripherals
  - Stop/wait/reset/break entry and recovery
  - Internal clock control
- Master reset control, including power-on reset (POR) and computer operating properly (COP) timeout
- Interrupt control:
  - Acknowledge timing
  - Arbitration control timing
  - Vector address generation
- CPU enable/disable timing

13.2 $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ Pins Initialization

$\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ pins come out of reset as PTA3 and PTA2 respectively. $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ functions can be activated by programing CONFIG2 accordingly. Refer to **Section 5. Configuration Register (CONFIG)**.

13.3 SIM Bus Clock Control and Generation

The bus clock generator provides system clock signals for the CPU and peripherals on the MCU. The system clocks are generated from an incoming clock, BUSCLKX2, as shown in **Figure 13-3**.

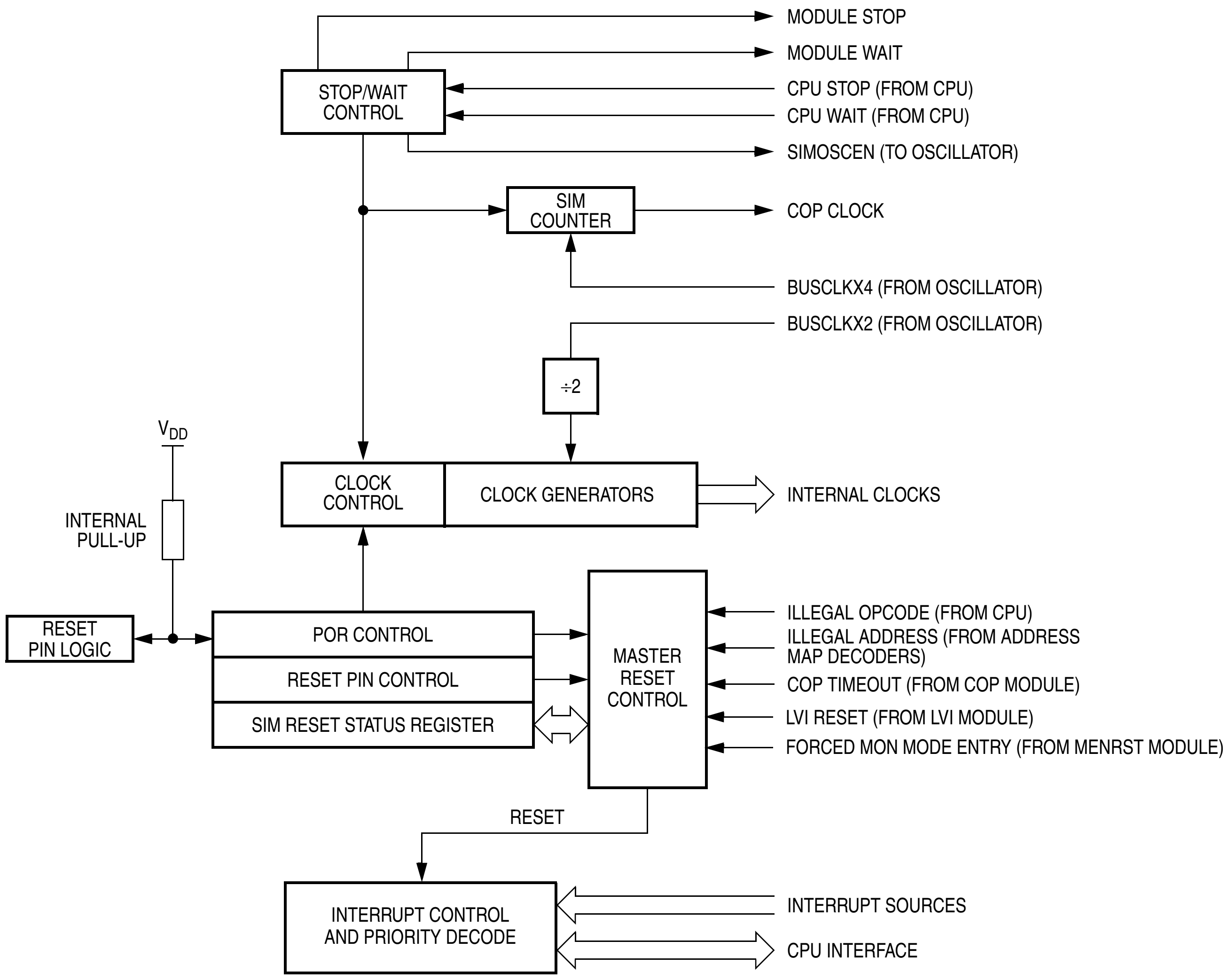


Figure 13-1. SIM Block Diagram

Table 13-1. Signal Name Conventions

Signal Name	Description
BUSCLKX4	Buffered clock from the internal, RC or XTAL oscillator circuit.
BUSCLKX2	The BUSCLKX4 frequency divided by two. This signal is again divided by two in the SIM to generate the internal bus clocks (bus clock = BUSCLKX4 ÷ 4).
Address bus	Internal address bus
Data bus	Internal data bus
PORRST	Signal from the power-on reset module to the SIM
IRST	Internal reset signal
R/$\overline{\text{W}}$	Read/write signal

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE00	Break Status Register (BSR) See page 138.	Read:	R	R	R	R	R	R	SBSW	R
		Write:							Note 1	
		Reset:	0	0	0	0	0	0	0	0
			1. Writing a 0 clears SBSW.							
$FE01	SIM Reset Status Register (SRSR) See page 137.	Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		POR:	1	0	0	0	0	0	0	0
$FE02	Reserved		R	R	R	R	R	R	R	R
$FE03	Break Flag Control Register (BFCR) See page 138.	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							
$FE04	Interrupt Status Register 1 (INT1) See page 132.	Read:	0	IF5	IF4	IF3	0	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE05	Interrupt Status Register 2 (INT2) See page 133.	Read:	IF14	0	0	0	0	0	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
$FE06	Interrupt Status Register 3 (INT3) See page 133.	Read:	0	0	0	0	0	0	0	IF15
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented R = Reserved

Figure 13-2. SIM I/O Register Summary

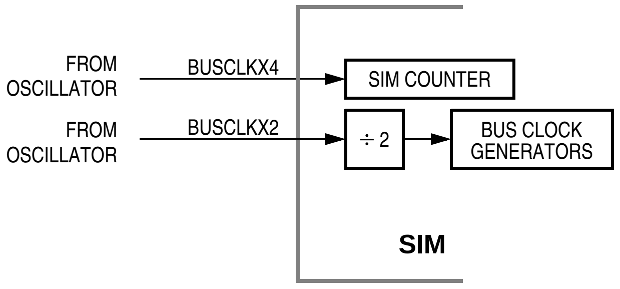


Figure 13-3. SIM Clock Signals

13.3.1 Bus Timing

In user mode, the internal bus frequency is the oscillator frequency (BUSCLKX4) divided by four.

13.3.2 Clock Start-Up from POR

When the power-on reset module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 BUSCLKX4 cycle POR time out has completed. The IBUS clocks start upon completion of the time out.

13.3.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt or reset, the SIM allows BUSCLKX4 to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay time out. This time out is selectable as 4096 or 32 BUSCLKX4 cycles. See **13.7.2 Stop Mode**.

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

13.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector \$FFFE–FFFF (\$FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see **13.5 SIM Counter**), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See **13.8 SIM Registers**.

13.4.1 External Pin Reset

The $\overline{\text{RST}}$ pin circuits include an internal pullup device. Pulling the asynchronous $\overline{\text{RST}}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{\text{RST}}$ is held low for a minimum of 67 BUSCLKX4 cycles, assuming that the POR was not the source of the reset. See **Table 13-2** for details. **Figure 13-4** shows the relative timing. The $\overline{\text{RST}}$ pin function is only available if the RSTEN bit is set in the CONFIG1 register.

Table 13-2. PIN Bit Set Timing

Reset Type	Number of Cycles Required to Set PIN
POR	4163 (4096 + 64 + 3)
All others	67 (64 + 3)

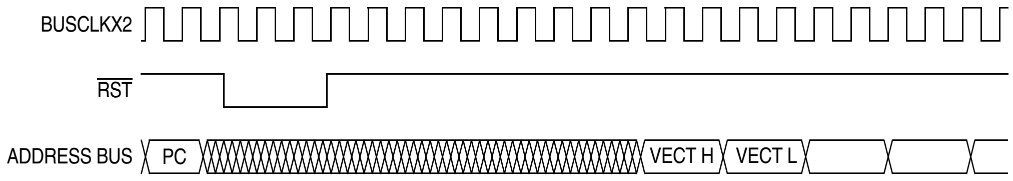


Figure 13-4. External Reset Timing

13.4.2 Active Resets from Internal Sources

The $\overline{\text{RST}}$ pin is initially setup as a general-purpose input after a POR. Setting the RSTEN bit in the CONFIG1 register enables the pin for the reset function. This section assumes the RSTEN bit is set when describing activity on the $\overline{\text{RST}}$ pin.

All internal reset sources actively pull the $\overline{\text{RST}}$ pin low for 32 BUSCLKX4 cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles (see **Figure 13-5**). An internal reset can be caused by an illegal address, illegal opcode, COP time out, LVI, or POR (see **Figure 13-6**).

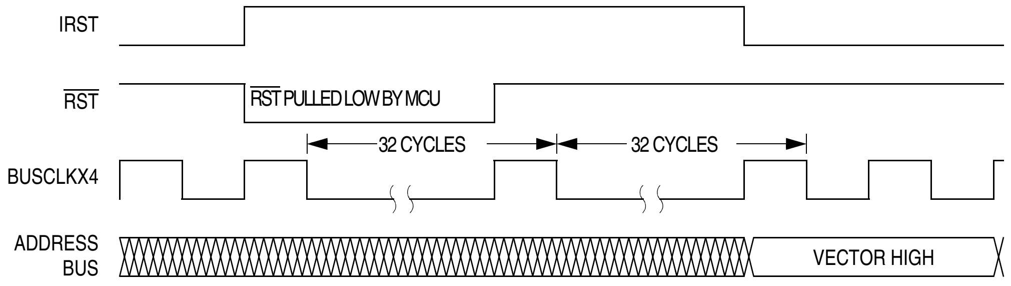


Figure 13-5. Internal Reset Timing

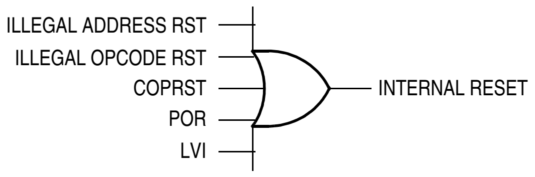


Figure 13-6. Sources of Internal Reset

NOTE: *For POR resets, the SIM cycles through 4096 BUSCLKX4 cycles. The internal reset signal then follows the sequence from the falling edge of $\overline{\text{RST}}$ shown in **Figure 13-5**.*

The COP reset is asynchronous to the bus clock.

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

13.4.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power on has occurred. SIM counter counts out 4096 BUSCLKX4 cycles. Sixty-four BUSCLKX4 cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power on, the following events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables the oscillator to drive BUSCLKX4.
- Internal clocks to the CPU and modules are held inactive for 4096 BUSCLKX4 cycles to allow stabilization of the oscillator.
- The POR bit of the SIM reset status register (SRSR) is set and all other bits in the register are cleared.

See **Figure 13-7**.

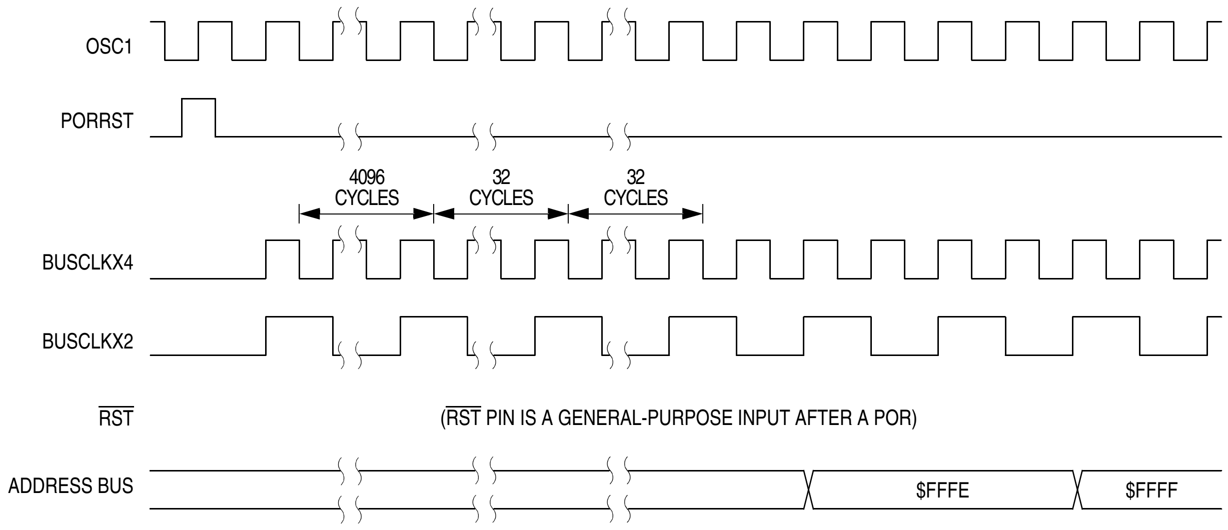


Figure 13-7. POR Recovery

13.4.2.2 Computer Operating Properly (COP) Reset

An input to the SIM is reserved for the COP reset signal. The overflow of the COP counter causes an internal reset and sets the COP bit in the SIM reset status register (SRSR). The SIM actively pulls down the $\overline{\text{RST}}$ pin for all internal reset sources.

To prevent a COP module time out, write any value to location $FFFF. Writing to location $FFFF clears the COP counter and stages 12–5 of the SIM counter. The SIM counter output, which occurs at least every (2^{12} – 2^4) BUSCLKX4 cycles, drives the COP counter. The COP should be serviced as soon as possible out of reset to guarantee the maximum amount of time before the first time out.

The COP module is disabled during a break interrupt with monitor mode when BDCOP bit is set in break auxiliary register (BRKAR).

13.4.2.3 Illegal Opcode Reset

The SIM decodes signals from the CPU to detect illegal instructions. An illegal instruction sets the ILOP bit in the SIM reset status register (SRSR) and causes a reset.

If the stop enable bit, STOP, in the mask option register is 0, the SIM treats the STOP instruction as an illegal opcode and causes an illegal opcode reset. The SIM actively pulls down the $\overline{\text{RST}}$ pin for all internal reset sources.

13.4.2.4 Illegal Address Reset

An opcode fetch from an unmapped address generates an illegal address reset. The SIM verifies that the CPU is fetching an opcode prior to asserting the ILAD bit in the SIM reset status register (SRSR) and resetting the MCU. A data fetch from an unmapped address does not generate a reset. The SIM actively pulls down the $\overline{\text{RST}}$ pin for all internal reset sources.

13.4.2.5 Low-Voltage Inhibit (LVI) Reset

The LVI asserts its output to the SIM when the V_{DD} voltage falls to the LVI trip voltage V_{Trip}. The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin ($\overline{\text{RST}}$) is held low while the SIM counter counts out 4096 BUSCLKX4 cycles. Sixty-four BUSCLKX4 cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the ($\overline{\text{RST}}$) pin for all internal reset sources.

13.5 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter uses 12 stages for counting, followed by a 13th stage that triggers a reset of SIM counters and supplies the clock for the COP module. The SIM counter is clocked by the falling edge of BUSCLKX4.

13.5.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the oscillator to drive the bus clock state machine.

13.5.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the configuration register 1 (CONFIG1). If the SSREC bit is a 1, then the stop recovery is reduced from the normal delay of 4096 BUSCLKX4 cycles down to 32 BUSCLKX4 cycles. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared in the configuration register 1 (CONFIG1).

13.5.3 SIM Counter and Reset States

External reset has no effect on the SIM counter (see **13.7.2 Stop Mode** for details.) The SIM counter is free-running after all reset states. See **13.4.2 Active Resets from Internal Sources** for counter control and internal reset recovery sequences.

13.6 Exception Control

Normal sequential program execution can be changed in three different ways:

1. Interrupts
   a. Maskable hardware CPU interrupts
   b. Non-maskable software interrupt instruction (SWI)
2. Reset
3. Break interrupts

13.6.1 Interrupts

An interrupt temporarily changes the sequence of program execution to respond to a particular event. **Figure 13-8** flow charts the handling of system interrupts.

Interrupts are latched, and arbitration is performed in the SIM at the start of interrupt processing. The arbitration result is a constant that the CPU uses to determine which vector to fetch. Once an interrupt is latched by the SIM, no other interrupt can take precedence, regardless of priority, until the latched interrupt is serviced (or the I bit is cleared).

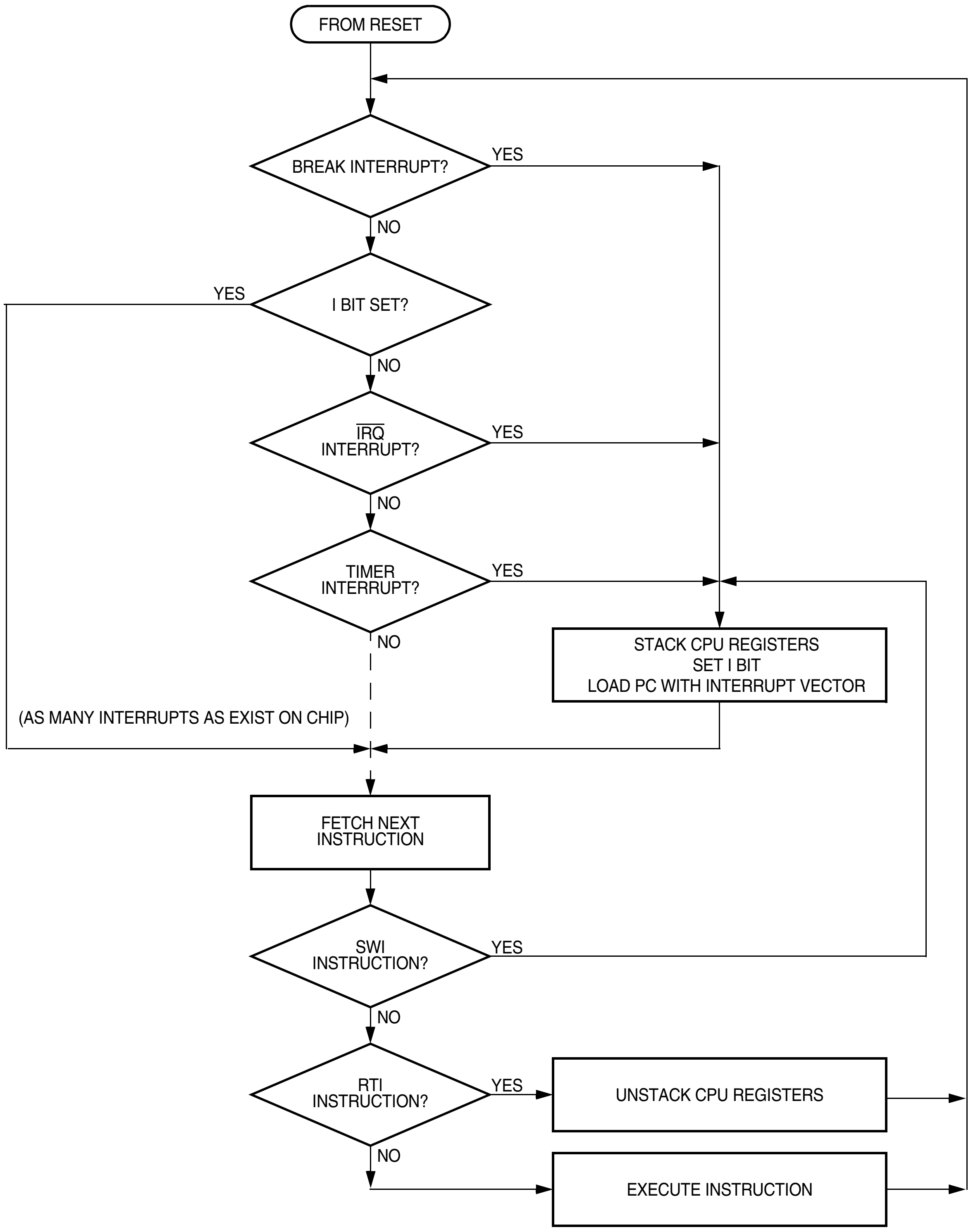


Figure 13-8. Interrupt Processing

At the beginning of an interrupt, the CPU saves the CPU register contents on the stack and sets the interrupt mask (I bit) to prevent additional interrupts. At the end of an interrupt, the RTI instruction recovers the CPU register contents from the stack so that normal processing can resume. **Figure 13-9** shows interrupt entry timing. **Figure 13-10** shows interrupt recovery timing.

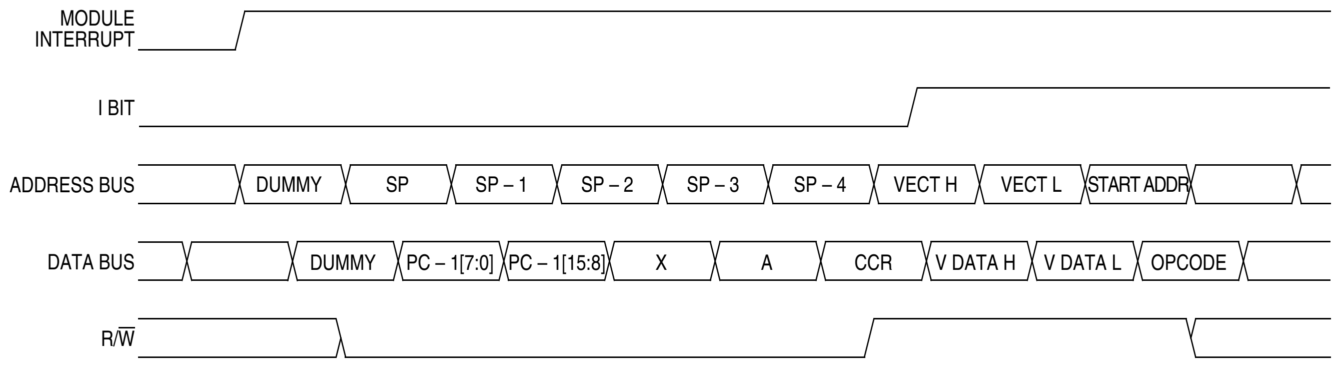


Figure 13-9. Interrupt Entry

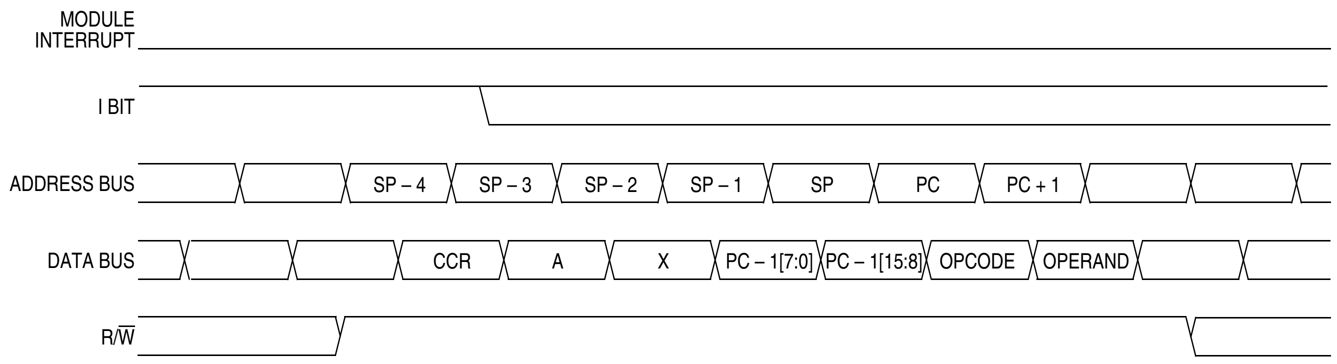


Figure 13-10. Interrupt Recovery

13.6.1.1 Hardware Interrupts

A hardware interrupt does not stop the current instruction. Processing of a hardware interrupt begins after completion of the current instruction. When the current instruction is complete, the SIM checks all pending hardware interrupts. If interrupts are not masked (I bit clear in the condition code register), and if the corresponding interrupt enable bit is set, the SIM proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If more than one interrupt is pending at the end of an instruction execution, the highest priority interrupt is serviced first. **Figure 13-11** demonstrates what happens when two interrupts are pending. If an interrupt is pending upon exit from the original interrupt service routine, the pending interrupt is serviced before the LDA instruction is executed.

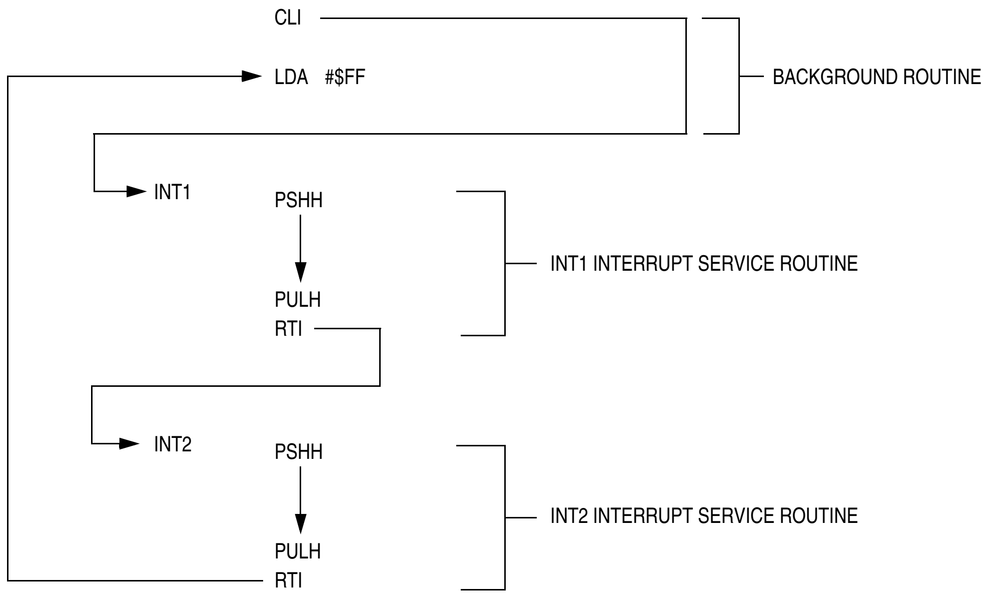

CLI
LDA #$FF
BACKGROUND ROUTINE
INT1
PSHH
PULH
RTI
INT1 INTERRUPT SERVICE ROUTINE
INT2
PSHH
PULH
RTI
INT2 INTERRUPT SERVICE ROUTINE

Figure 13-11. Interrupt Recognition Example

The LDA opcode is prefetched by both the INT1 and INT2 return-from-interrupt (RTI) instructions. However, in the case of the INT1 RTI prefetch, this is a redundant operation.

NOTE: *To maintain compatibility with the M6805 Family, the H register is not pushed on the stack during interrupt entry. If the interrupt service routine modifies the H register or uses the indexed addressing mode, software should save the H register and then restore it prior to exiting the routine.*

13.6.1.2 SWI Instruction

The SWI instruction is a non-maskable instruction that causes an interrupt regardless of the state of the interrupt mask (I bit) in the condition code register.

NOTE: *A software interrupt pushes PC onto the stack. A software interrupt does **not** push PC – 1, as a hardware interrupt does.*

13.6.2 Interrupt Status Registers

The flags in the interrupt status registers identify maskable interrupt sources. Table 13-3 summarizes the interrupt sources and the interrupt status register flags that they set. The interrupt status registers can be useful for debugging.

Table 13-3. Interrupt Sources

Priority	Source	Flag	Mask[1]	INT Register Flag	Vector Address
Highest	Reset	—	—	—	\$FFFE–\$FFFF
	SWI instruction	—	—	—	\$FFFC–\$FFFD
	$\overline{\text{IRQ}}$ pin	IRQF1	IMASK1	IF1	\$FFFA–\$FFFB
	Timer channel 0 interrupt	CH0F	CH0IE	IF3	\$FFF6–\$FFF7
	Timer channel 1 interrupt	CH1F	CH1IE	IF4	\$FFF4–\$FFF5
	Timer overflow interrupt	TOF	TOIE	IF5	\$FFF2–\$FFF3
	SLIC interrupt	SLCF	SLCIE	IF9	\$FFE6–\$FFE7
	Keyboard interrupt	KEYF	IMASKK	IF14	\$FFDE–\$FFDF
Lowest	ADC conversion complete interrupt	COCO	AIEN	IF15	\$FFE0–\$FFE1

1. The I bit in the condition code register is a global mask for all interrupt sources except the SWI instruction.

13.6.2.1 Interrupt Status Register 1

Address: \$FE04

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	IF5	IF4	IF3	0	IF1	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 13-12. Interrupt Status Register 1 (INT1)

IF1 and IF3–IF5 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in Table 13-3.

1 = Interrupt request present

0 = No interrupt request present

Bit 0, 1, 3, and 7 — Always read 0

13.6.2.2 Interrupt Status Register 2

Address: $FE05

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IF14	0	0	0	0	IF9	0	0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 13-13. Interrupt Status Register 2 (INT2)

IF14 and IF11–IF9 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in **Table 13-3**.

1 = Interrupt request present
0 = No interrupt request present

Bit 0, 1, 3–6 — Always read 0

13.6.2.3 Interrupt Status Register 3

Address: $FE06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	IF15
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 13-14. Interrupt Status Register 3 (INT3)

IF15 — Interrupt Flags

These flags indicate the presence of interrupt requests from the sources shown in **Table 13-3**.

1 = Interrupt request present
0 = No interrupt request present

Bit 1–7 — Always read 0

13.6.3 Reset

All reset sources always have equal and highest priority and cannot be arbitrated.

13.6.4 Break Interrupts

The break module can stop normal program flow at a software programmable break point by asserting its break interrupt output. (See **Section 16. Development Support**.) The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

13.6.5 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

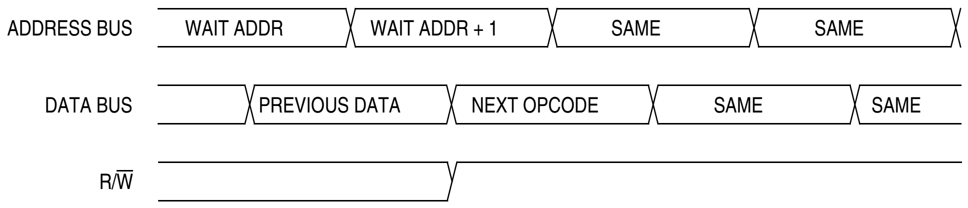
Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a two-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

13.7 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described below. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

13.7.1 Wait Mode

In wait mode, the CPU clocks are inactive while the peripheral clocks continue to run. **Figure 13-15** shows the timing for wait mode entry.



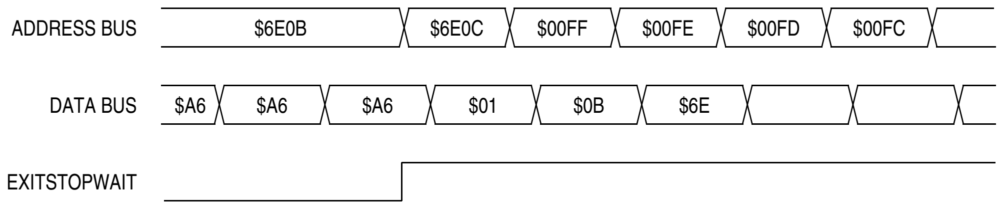
NOTE: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 13-15. Wait Mode Entry Timing

A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

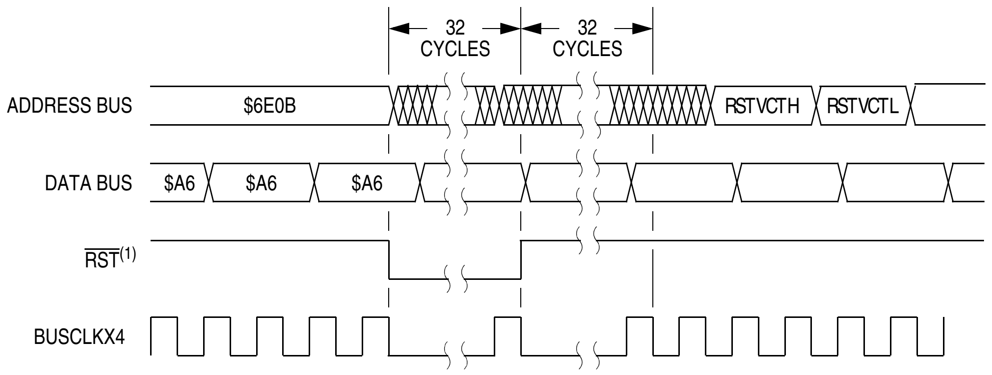
Wait mode can also be exited by a reset (or break in emulation mode). A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the break status register (BSR). If the COP disable bit, COPD, in the configuration register is 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.

Figure 13-16 and **Figure 13-17** show the timing for wait recovery.



NOTE: EXITSTOPWAIT = $\overline{\text{RST}}$ pin OR CPU interrupt

Figure 13-16. Wait Recovery from Interrupt



1. $\overline{\text{RST}}$ is only available if the RSTEN bit in the CONFIG1 register is set.

Figure 13-17. Wait Recovery from Internal Reset

13.7.2 Stop Mode

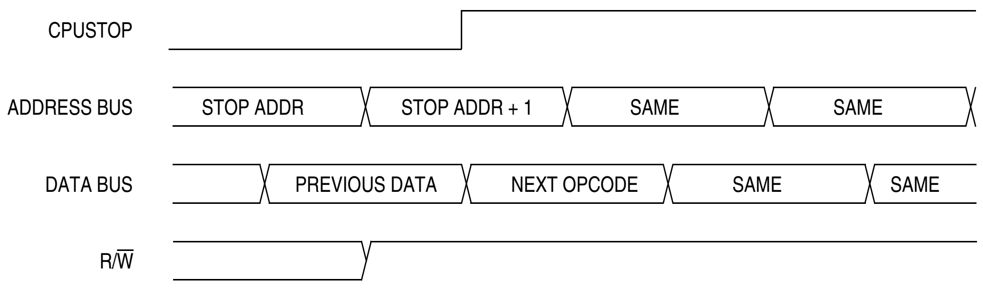
In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

The SIM disables the oscillator signals (BUSCLKX2 and BUSCLKX4) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the configuration register 1 (CONFIG1). If SSREC is set, stop recovery is reduced from the normal delay of 4096 BUSCLKX4 cycles down to 32. This is ideal for the internal oscillator, RC oscillator, and external oscillator options which do not require long start-up times from stop mode.

NOTE: *External crystal applications should use the full stop recovery time by clearing the SSREC bit.*

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. **Figure 13-18** shows stop mode entry timing and **Figure 13-19** shows the stop mode recovery time from interrupt or break

NOTE: *To minimize stop current, all pins configured as inputs should be driven to a logic 1 or logic 0.*



NOTE: Previous data can be operand data or the STOP opcode, depending on the last instruction.

Figure 13-18. Stop Mode Entry Timing

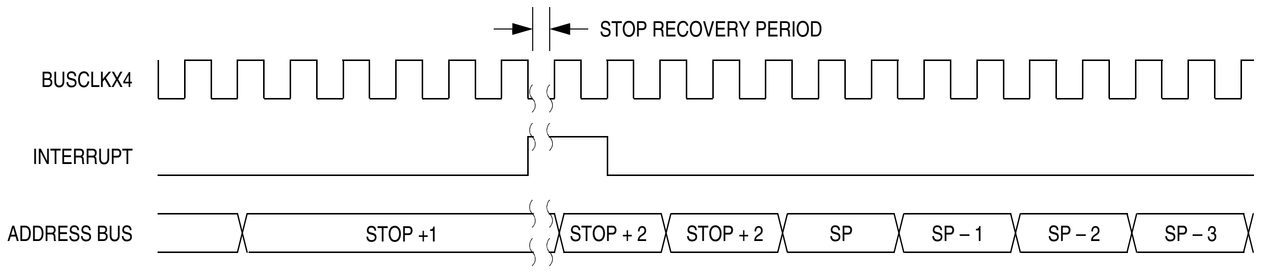


Figure 13-19. Stop Mode Recovery from Interrupt

13.8 SIM Registers

The SIM has three memory mapped registers. **Table 13-4** shows the mapping of these registers.

Table 13-4. SIM Registers

Address	Register	Access Mode
$FE00	BSR	User
$FE01	SRSR	User
$FE03	BFCR	User

13.8.1 SIM Reset Status Register

This register contains seven flags that show the source of the last reset. Clear the SIM reset status register by reading it. A power-on reset sets the POR bit and clears all other bits in the register.

Address: $FE01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
POR:	1	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 13-20. SIM Reset Status Register (SRSR)

POR — Power-On Reset Bit
- 1 = Last reset caused by POR circuit
- 0 = Read of SRSR

PIN — External Reset Bit
- 1 = Last reset caused by external reset pin ($\overline{\text{RST}}$)
- 0 = POR or read of SRSR

COP — Computer Operating Properly Reset Bit
- 1 = Last reset caused by COP counter
- 0 = POR or read of SRSR

ILOP — Illegal Opcode Reset Bit
- 1 = Last reset caused by an illegal opcode
- 0 = POR or read of SRSR

ILAD — Illegal Address Reset Bit (opcode fetches only)
- 1 = Last reset caused by an opcode fetch from an illegal address
- 0 = POR or read of SRSR

MODRST — Monitor Mode Entry Module Reset bit
- 1 = Last reset caused by monitor mode entry when vector locations $FFFE and $FFFF are $FF after POR while $\overline{\text{IRQ}}$ = V_{DD}
- 0 = POR or read of SRSR

LVI — Low Voltage Inhibit Reset bit
- 1 = Last reset caused by LVI circuit
- 0 = POR or read of SRSR

13.8.2 Break Flag Control Register

The break control register (BFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: $FE03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	BCFE	R	R	R	R	R	R	R
Reset:	0							

R = Reserved

Figure 13-21. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break
0 = Status bits not clearable during break

13.8.3 Break Status Register

The break status register (BSR) contains a flag to indicate that a break caused an exit from wait mode. This register is only used in emulation mode.

Address: $FE00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							Note [1]	
Reset:							0	

R = Reserved

1. Writing a 0 clears SBSW.

Figure 13-22. Break Status Register (BSR)

SBSW — SIM Break Stop/Wait

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it.

1 = Wait mode was exited by break interrupt
0 = Wait mode was not exited by break interrupt

Section 14. Slave LIN Interface Controller (SLIC)

14.1 Introduction

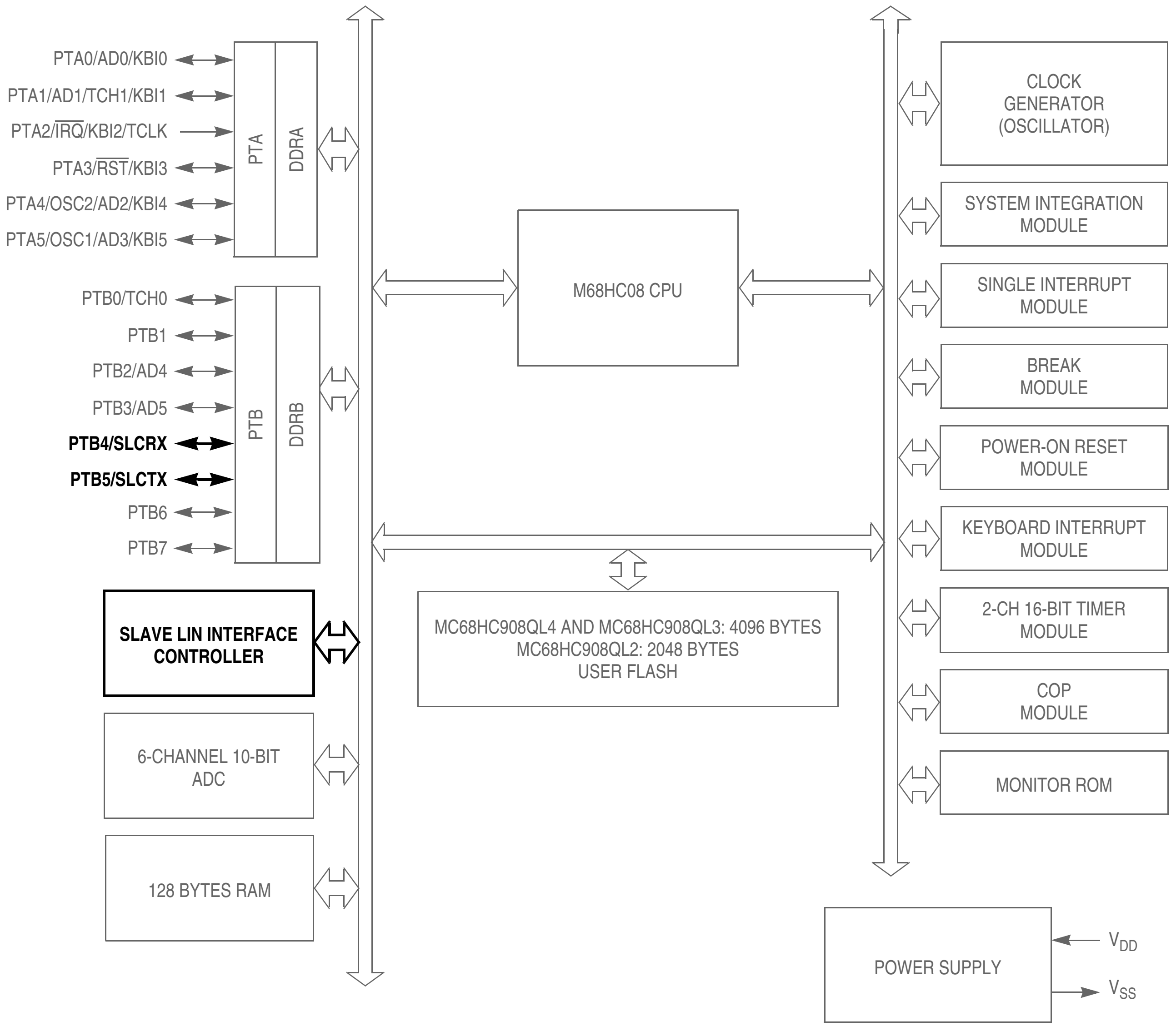
The slave LIN interface controller (SLIC) is designed to provide slave node connectivity on a local interconnect network (LIN) sub-bus. LIN is an open-standard serial protocol developed for the automotive industry to connect sensors, motors, and actuators.

The SLIC provides full standard LIN message buffering for a slave node, minimizing the need for CPU intervention. Routine protocol functions (such as synchronization to the communication channel, reception, and verification of header data) and generation of the checksum are handled automatically by the SLIC. This allows application software to be greatly simplified relative to standard UART implementations, as well as reducing the impact of interrupts needed in those applications to handle each byte of a message independently.

Additionally, the SLIC has the ability to automatically synchronize to any LIN message, regardless of the LIN bus bit rate (1–20 kbps), properly receiving that message without prior programming of the target LIN bit rate. Furthermore, this can even be accomplished using an untrimmed internal oscillator, provided it’s accuracy is at least ±50% of nominal.

The SLIC also has a simple UART-like byte transfer mode, which allows the user to send and receive single bytes of data in half-duplex 8-N-1 format (8-bit data, no parity, 1 stop bit) without the need for LIN message framing.

Figure 14-2 is a block diagram of the SLIC module, showing the basic functional blocks contained in the module.



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30 kΩ) pull up
PTA0, PTA1, PTA3–PTA5: High current sink and source capability
PTA0–PTA5: Pins have programmable keyboard interrupt and pull up
ADC pins only available on MC68HC908QL4 and MC68HC908QL2

Figure 14-1. Block Diagram Highlighting SLIC Block and Pins

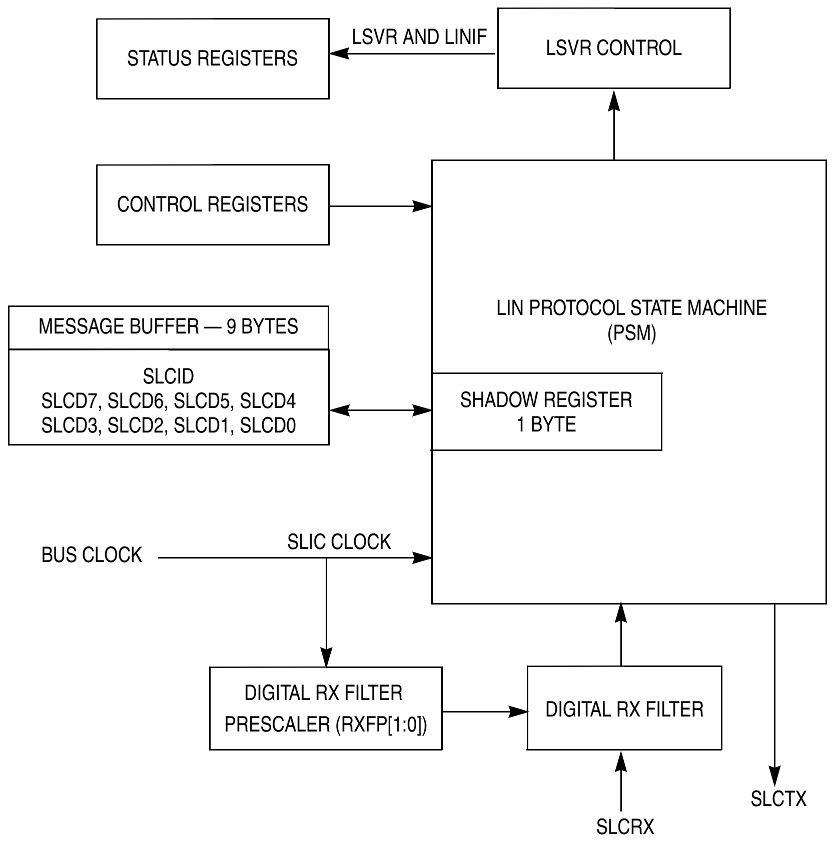


Figure 14-2. SLIC Module Block Diagram

14.2 Features

The SLIC includes these distinctive features:

- Full LIN message buffering of identifier and 8 data bytes
- Automatic bit rate and LIN message frame synchronization:
  - No prior programming of bit rate required, 1–20 kbps LIN bus speed operation
  - All LIN messages will be received (no message loss due to synchronization process)
  - Input clock tolerance as high as ±50%, allowing internal oscillator to remain untrimmed
  - Incoming break symbols always allowed to be 10 or more bit times without message loss
  - Supports automatic software trimming of internal oscillator using LIN synchronization data
- Automatic processing and verification of LIN SYNCH BREAK and SYNCH BYTE

- Automatic checksum calculation and verification with error reporting
- Maximum of two interrupts per standard LIN message frame with no errors
- Full LIN error checking and reporting
- High-speed LIN capability up to 83.33 kbps to 120.00 kbps[1]
- Configurable digital receive filter
- Streamlined interrupt servicing through use of a state vector register
- Switchable UART-like byte transfer mode for processing bytes one at a time without LIN message framing constraints
- Enhanced checksum (includes ID) generation and verification

14.3 Modes of Operation

Figure 14-3 shows the modes in which the SLIC will operate.

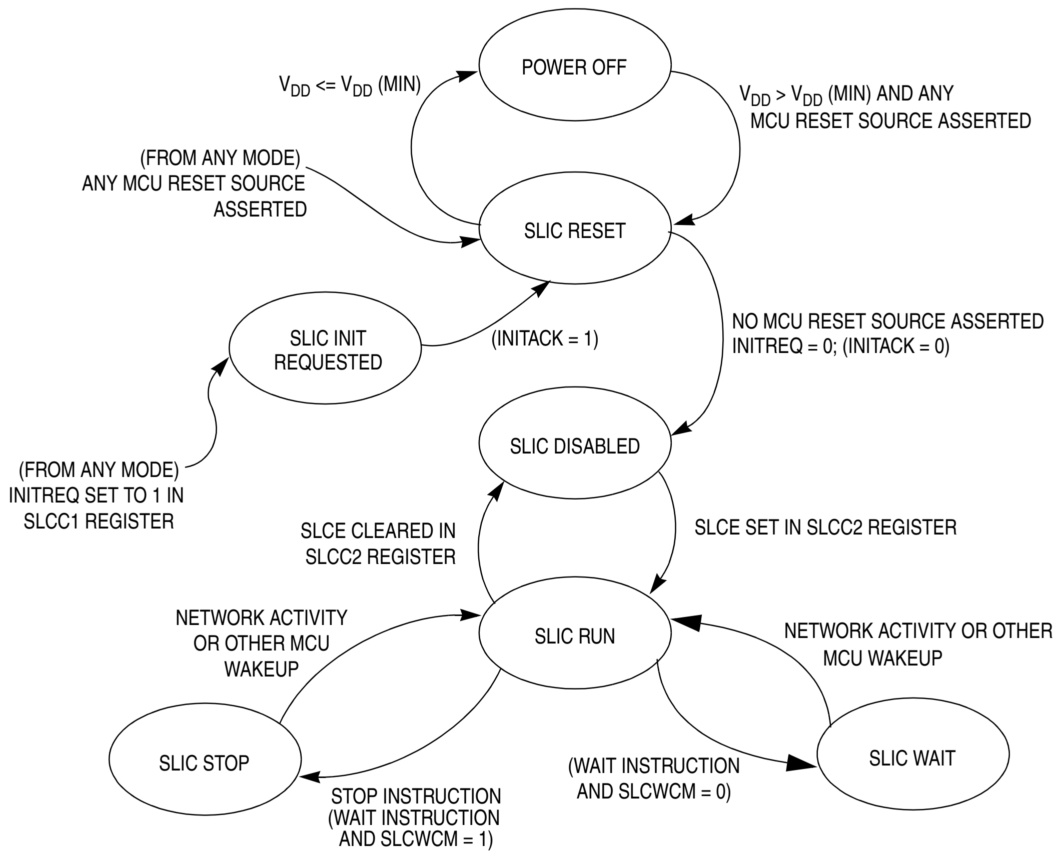

POWER OFF
V_{DD} <= V_{DD} (MIN)
V_{DD} > V_{DD} (MIN) AND ANY MCU RESET SOURCE ASSERTED
(FROM ANY MODE) ANY MCU RESET SOURCE ASSERTED
SLIC RESET
SLIC INIT REQUESTED
(INITACK = 1)
NO MCU RESET SOURCE ASSERTED INITREQ = 0; (INITACK = 0)
SLIC DISABLED
(FROM ANY MODE) INITREQ SET TO 1 IN SLCC1 REGISTER
SLCE CLEARED IN SLCC2 REGISTER
SLCE SET IN SLCC2 REGISTER
NETWORK ACTIVITY OR OTHER MCU WAKEUP
SLIC RUN
NETWORK ACTIVITY OR OTHER MCU WAKEUP
SLIC STOP
SLIC WAIT
STOP INSTRUCTION (WAIT INSTRUCTION AND SLCWCM = 1)
(WAIT INSTRUCTION AND SLCWCM = 0)

Figure 14-3. SLIC Operating Modes

1. Maximum bit rate of SLIC module dependent upon frequency of SLIC input clock.

14.3.1 Power Off

This mode is entered from the reset mode whenever the SLIC module supply voltage V_{DD} drops below its minimum specified value for the SLIC module to guarantee operation. The SLIC module will be placed in the reset mode by a system low-voltage reset (LVR) before being powered down. In this mode, the pin input and output specifications are not guaranteed.

14.3.2 Reset

This mode is entered from the power off mode whenever the SLIC module supply voltage V_{DD} rises above its minimum specified value ($V_{DD(MIN)}$) and some MCU reset source is asserted. To prevent the SLIC from entering an unknown state, the internal MCU reset is asserted while powering up the SLIC module. SLIC reset mode is also entered from any other mode as soon as one of the MCU's possible reset sources (e.g., LVR, POR, COP watchdog, $\overline{\text{RST}}$ pin, etc.) is asserted. SLIC reset mode may also be entered by the user software by asserting the INITREQ bit. INITACK indicates whether the SLIC module is in the reset mode as a result of writing INITREQ in SLCC1. While in the reset state the SLIC module clocks are stopped. Clearing the INITREQ allows the SLIC to proceed and enter SLIC run mode (if SLCE is set). The module will clear INITACK once the module has left reset mode and the SLIC will seek the next LIN header. It is the responsibility of the user to verify that this operation is compatible with the application before implementing this feature.

In this mode, the internal SLIC module voltage references are operative, V_{DD} is supplied to the internal circuits, which are held in their reset state and the internal SLIC module system clock is running. Registers will assume their reset condition. Outputs are held in their programmed reset state, inputs and network activity are ignored.

14.3.3 SLIC Disabled

This mode is entered from the reset mode after all MCU reset sources are no longer asserted or INITREQ bit is cleared by the user and the SLIC module clears the INITACK bit. It is entered from the run mode whenever the SLCE bit in the SLCC2 register is cleared. In this mode the SLIC clock is stopped to conserve power and allow the SLIC module to be configured for proper operation on the LIN bus. The IP bus interface clocks are left running in this mode to allow access to all SLIC module registers for initialization.

14.3.4 SLIC Run

This mode is entered from the SLIC disabled mode when the SLCE bit in the SLCC2 register is set. It is entered from the SLIC wait mode whenever activity is sensed on the LIN bus or some other MCU source wakes the CPU out of wait mode.

It is entered from the SLIC stop mode whenever network activity is sensed or some other MCU source wakes the CPU out of stop mode. Messages will not be received properly until the clocks have stabilized and the CPU is also in the run mode.

14.3.5 SLIC Wait (Core Specific)

This power conserving mode is automatically entered from the run mode whenever the CPU executes a WAIT instruction and the SLCWCM bit in the SLCC1 register is previously cleared. In this mode, the SLIC module internal clocks continue to run. Any activity on the LIN network will cause the SLIC module to exit SLIC wait mode and generate an unmaskable interrupt of the CPU. This wakeup interrupt state is reflected in the SLCSV, encoded as the highest priority interrupt. This interrupt can be cleared by the CPU with a read of the SLCSV.

14.3.6 Wakeup from SLIC Wait with CPU in WAIT

If the CPU executes the WAIT instruction and the SLIC module enters the wait mode (SLCWCM = 0), the clocks to the SLIC module as well as the clocks in the MCU continue to run. Therefore, the message which wakes up the SLIC module from WAIT and the CPU from wait mode will also be received correctly by the SLIC module. This is because all of the required clocks continue to run in the SLIC module in wait mode.

14.3.7 SLIC Stop (Core Specific)

This power conserving mode is automatically entered from the run mode whenever the CPU executes a STOP instruction, or if the CPU executes a WAIT instruction and the SLCWCM bit in the SLCC1 register is previously set. In this mode, the SLIC internal clocks are stopped. Any activity on the network will cause the SLIC module to exit SLIC stop mode and generate an unmaskable interrupt of the CPU. This wakeup interrupt state is reflected in the SLCSV, encoded as the highest priority interrupt. This interrupt can be cleared by the CPU with a read of the SLCSV. Depending upon which low-power mode instruction the CPU executes to cause the SLIC module to enter SLIC stop, the message which wakes up the SLIC module (and the CPU) may or may not be received.

There are two different possibilities:

1. Wakeup from SLIC Stop with CPU in STOP

   When the CPU executes the STOP instruction, all clocks in the MCU, including clocks to the SLIC module, are turned off. Therefore, the message which wakes up the SLIC module and the CPU from stop mode will not be received. This is due primarily to the amount of time required for the MCU's oscillator to stabilize before the clocks can be applied internally to the other MCU modules, including the SLIC module.

2. Wakeup from SLIC Stop with CPU in WAIT

   If the CPU executes the WAIT instruction and the SLIC module enters the stop mode (SLCWCM = 1), the clocks to the SLIC module are turned off, but the clocks in the MCU continue to run. Therefore, the message which wakes up the SLIC module from stop and the CPU from wait mode will be received correctly by the SLIC module. This is because very little time is required for the CPU to turn the clocks to the SLIC module back on once the wakeup interrupt occurs.

NOTE: *While the SLIC module will correctly receive a message which arrives when the SLIC module is in stop or wait mode and the MCU is in wait mode, if the user enters this mode while a message is being received, the data in the message will become corrupted. This is due to the steps required for the SLIC module to resume operation upon exiting stop or wait mode, and its subsequent resynchronization with the LIN bus.*

14.3.8 Normal and Emulation Mode Operation (Core Specific)

The SLIC module operates in the same manner in all normal and emulation modes. All SLIC module registers can be read and written except those that are reserved, unimplemented, or write once. The user must be careful not to unintentionally write a register when using 16-bit writes in order to avoid unexpected SLIC module behavior.

14.3.9 Special Mode Operation (Core Specific)

Some aspects of SLIC module operation can be modified in special test mode. This mode is reserved for internal use only.

14.3.10 Low-Power Options (Core Specific)

The SLIC module can save power in disabled, wait, and stop modes. A complete description of what the SLIC module does while in a low-power mode can be found in **14.3 Modes of Operation**.

14.4 External Signal Description

The SLIC module has only two external signals which may be brought out to MCU pins. These might share functionality with other modules or general-purpose input/output functions of the pins. When used in a LIN system, these pins will be connected to the TX and RX pins of the LIN physical layer.

14.4.1 SLCTX — SLIC Transmit Pin

The SLCTX pin serves as the serial output of the SLIC module.

14.4.2 SLCRX — SLIC Receive Pin

The SLCRX pin serves as the serial input of the SLIC module. This input feeds directly into the digital receive filter block which filters out noise glitches from the incoming data stream.

14.5 Memory Map/Register Definition

Table 14-1 shows the registers for the SLIC module.

Table 14-1. SLIC Module Memory Map

Address	Use	Access
$0040	SLIC control register 1 (SLCC1)	R/W
$0041	SLIC control register 2 (SLCC2)	R/W
$0042	SLIC status register (SLCS)	R/W
$0043	SLIC prescaler register (SLCP)	R/W
$0044	SLIC bit time register high (SLCBTH)	R/W
$0045	SLIC bit time register low (SLCBTL)	R/W
$0046	SLIC state vector register (SLCSV)	R
$0047	SLIC data length code register (SLCDLC)	R/W
$0048	SLIC identifier register (SLCID)	R/W
$0049	SLIC data register 7 (SLCD7)	R/W
$004A	SLIC data register 6 (SLCD6)	R/W
$004B	SLIC data register 5 (SLCD5)	R/W
$004C	SLIC data register 4 (SLCD4)	R/W
$004D	SLIC data register 3 (SLCD3)	R/W
$004E	SLIC data register 2 (SLCD2)	R/W
$004F	SLIC data register 1 (SLCD1)	R/W
$0050	SLIC data register 0 (SLCD0)	R/W

14.6 SLIC Registers and Control Bits

This subsection provides information about all registers and control bits associated with the SLIC module.

14.6.1 SLIC Control Register 1

SLIC control register 1 (SLCC1) contains bits used to control various basic features of the SLIC module, including features used for initialization and at runtime.

Address: $0040

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	INITREQ	0	WAKETX	TXABRT	IMSG	SLCIE
Write:	▨	▨		▨				
Reset:	0	0	1	0	0	0	0	0

▨ = Unimplemented

Figure 14-4. SLIC Control Register 1 (SLCC1)

INITREQ —Initialization Request

Requesting initialization mode by setting this bit will place the SLIC module into its initialized state immediately. If transmission or reception of data is in progress, the transaction will be terminated immediately upon entry into initialization mode (signified by INITACK being set to 1). To return to normal SLIC operation after the SLIC has been initialized (the INITACK is high), the INITREQ has to be cleared by software.

1 = Request for SLIC to be put into reset state immediately
0 = Normal operation

WAKETX — Transmit Wakeup Symbol

This bit allows the user to transmit a wakeup symbol on the LIN bus. When set, this sends a wakeup symbol, as defined in the LIN specification a single time, then resets to 0. This bit will read 1 while the wakeup symbol is being transmitted on the bus. This bit will be automatically cleared when the wakeup symbol is complete.

1 = Send wakeup symbol on LIN bus
0 = Normal operation

TXABRT — Transmit Abort Message

1 = Transmitter aborts current transmission at next byte boundary; TXABRT resets to 0 after the transmission is successfully aborted
0 = Normal operation

IMSG — SLIC Ignore Message Bit

The IMSG bit cannot be cleared by a write of 0, but is cleared automatically by the SLIC module after the next BREAK/SYNC symbol pair is validated.

1 = SLIC to ignore data field of message, SLIC interrupts are suppressed until the next message header arrives
0 = Normal operation

SLCIE — SLIC Interrupt Enable

1 = SLIC interrupt sources are enabled
0 = SLIC interrupt sources are disabled

14.6.2 SLIC Control Register 2

SLIC control register 2 (SLCC2) contains bits used to control various features of the SLIC module.

Address: $0041

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	SLCWCM	BTM	0	SLCE
Write:	▨	▨	▨	▨			▨	
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 14-5. SLIC Control Register 2 (SLCC2)

SLCWCM — SLIC Wait Clock Mode

This bit can only be written once out of reset state.

1 = SLIC clocks stop when the CPU is placed into wait mode
0 = SLIC clocks continue to run when the CPU is placed into wait mode so that the SLIC can receive messages and wakeup the CPU.

BTM — UART Byte Transfer Mode

Byte transmit mode bypasses the normal LIN message framing and checksum monitoring and allows the user to send and receive single bytes in a method similar to a half-duplex UART. When enabled, this mode reads the bit time register (SLCBT) value and assumes this is the value corresponding to the number of SLIC clock counts for one bit time to establish the desired UART bit rate. The user software must initialize this register prior to sending or receiving data, based on the input clock selection, prescaler stage choice, and desired bit rate.

BTM forces the data length in SLCDLC register to one byte (DLC = 0x00) and disables the checksum circuitry so that CHKMOD has no effect. Refer to **14.18 Byte Transfer Mode Operation** for more detailed information about how to use this mode.

BTM sets up the SLIC module to send and receive one byte at a time, with 8-bit data, no parity, and 1 STOP bit (8-N-1). This is the most commonly used setup for UART communications and should work for most applications. This is fixed in the SLIC and is not configurable.

1 = UART byte transfer mode enabled
0 = UART byte transfer mode disabled

SLCE — SLIC Module Enable

1 = SLIC module enabled
0 = SLIC module disabled

NOTE: *In order to guarantee timing, the user must ensure that clock source used allows the proper communications timing tolerances and therefore internal oscillator circuits might not be appropriate for use with BTM mode.*

14.6.3 SLIC Status Register

SLIC status register (SLCS) contains bits used to monitor the status of the SLIC module.

Address: $0042

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SLCACT	0	INITACK	0	0	0	0	SLCF
Write:	▨	▨	▨	▨	▨	▨	▨	
Reset:	0	0	1	0	0	0	0	0

▨ = Unimplemented

Figure 14-6. SLIC Status Register (SLCS)

SLCACT — SLIC Active (Oscillator Trim Blocking Semaphore)

SLCACT is used to indicate if it is safe to trim the oscillator based upon current SLIC activity. This bit indicates that the SLIC module might be currently receiving a message header, synchronization byte, ID byte, or sending or receiving data bytes. This bit is read-only.

1 = SLIC module activity (not safe to trim oscillator)
SLCACT is automatically set to 1 if a falling edge is seen on the SLCRX pin and has successfully been passed through the digital RX filter. This edge is the potential beginning of a LIN message frame.

0 = SLIC module not active (safe to trim oscillator)
The SLCACT bit is cleared by the SLIC module only upon assertion of the RX Message Buffer Full Checksum OK (SLCSV = $10) or the TX Message Buffer Empty Checksum Transmitted (SLCSV = $08) interrupt sources.

INITACK — Initialization Mode Acknowledge

INITACK indicates whether the SLIC module is in the reset mode as a result of writing INITREQ in SLCC1. While in the reset state the SLIC module clocks are stopped. Clearing the INITREQ allows the SLIC to proceed and enter SLIC run mode (if SLCE is set). The module will clear INITACK once the module has left reset mode and the SLIC will seek the next LIN header. This bit is read-only.

1 = SLIC module is in reset state
0 = Normal operation

SLCF — SLIC Interrupt Flag

The SLCF interrupt flag indicates if a SLIC module interrupt is pending. If set, the SLCSV is then used to determine what interrupt is pending. This flag is cleared by writing a 1 to the bit. If additional interrupt sources are pending, the bit will be automatically set to 1 again by the SLIC.

1 = SLIC interrupt pending
0 = No SLIC interrupt pending

14.6.4 SLIC Prescaler Register

SLIC prescaler register (SLCP) is used to divide the CPU bus clock for the digital receive filter circuit. The SLIC clock is divided through a prescaler (controlled by RXFP[1:0]) to drive the digital receive circuit. Variations on the input clock will propagate through these prescale stages, so if internal oscillators are used, worst case oscillator frequencies must be accounted for when determining prescaler settings to ensure that the frequency of the SLIC clock always remains between 2 MHz and 8 MHz.

Address: $0043

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RXFP1	RXFP0	0	0	0	0	0	0
Write:			▨	▨	▨	▨	▨	▨
Reset:	1	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 14-7. SLIC Prescale Register (SLCP)

Table 14-2. Digital Receive Filter Clock Prescaler

RXFP[1:0]	Digital RX Filter Clock Prescaler (Divide by)	Maximum Filter Delay (in µs)					
		SLIC Clock (in MHz)					
		2	**3.2**	**4**	**6**	**6.4**	**8**
$00	1	8	5	4	2.67	2.5	2
$01	2	16	10	8	5.33	5	4
$10	3 (default)	24	15	12	8	7.5	6
$11	4	32	20	16	10.67	10	8

RXFP[1:0] — Receive Filter Prescaler

These bits set the prescale value for the clock for the digital receive filter circuit. This is a further prescaling of the SLIC input clock, which must be kept between 2 MHz and 8 MHz for proper SLIC operation in LIN. The RXFP bits control the speed of the clock feeding the digital receive filter circuit, which determines the total maximum filter delay. Any pulse which is smaller than the maximum filter delay value will be rejected by the filter and ignored as noise. For this reason, the user must choose the prescaler value appropriately to ensure that all valid message traffic is able to pass the filter for the desired bit rate. For more details about setting up the digital receive filter, please refer to **14.20 Digital Receive Filter**.

The frequency of the SLIC clock must be between 2 MHz and 8 MHz, factoring in worst case possible numbers due to untrimmed process variations, as well as temperature and voltage variations in oscillator frequency. This will guarantee greater than 1.5% accuracy for all LIN messages from 1–20 kbps. The faster this input clock is, the greater the resulting accuracy and the higher the possible bit rates at which the SLIC can send and receive. In LIN systems, the bit rates will not exceed 20 kbps; however, the SLIC module is capable of much higher speeds without any configuration changes, for cases such as high-speed downloads for reprogramming of FLASH memory or diagnostics in a test environment where radiated emissions requirements are not as stringent. In these situations, the user may choose to run faster than the 20 kbps limit which is imposed by the LIN specification for EMC reasons. Details of how to calculate maximum bit rates and operate the SLIC above 20 kbps are detailed in **14.17 High-Speed LIN Operation**.

Refer to **14.9 SLIC Module Initialization Procedure** for more information on when to set up this register.

14.6.5 SLIC Bit Time Registers

NOTE: *In this subsection, the SLIC bit time registers are collectively referred to as SLCBT.*

In LIN operating mode (BTM = 0), the SLCBT is updated by the SLIC upon reception of a LIN break-synch combination and provides the number of SLIC clock counts that equal one LIN bit time to the user software. This value can be used by the software to calculate the clock drift in the oscillator as an offset to a known count value (based on nominal oscillator frequency and LIN bus speed). The user software can then trim the oscillator to compensate for clock drift. Refer to **14.19 Oscillator Trimming with SLIC** for more information on this procedure. The user cannot read the bit time value from SLCBTH and SLCBTL any time after the identifier byte is received until the beginning of the next LIN message frame on the bus. The beginning of this message frame activity will be indicated by the SLCACT bit.

When in byte transfer mode (BTM = 1), the SLCBT must be written by the user to set the length of one bit at the desired bit rate in SLIC clock counts. The user software must initialize this number prior to sending or receiving data, based on the input clock selection, prescaler stage choice, and desired bit rate. This setting is similar to choosing an input capture or output compare value for a timer. The closest even value should be chosen for this value, as BT0 will be forced to 0 by the SLIC module and any odd value will always be reduced to the next lowest even integer value. For example, a write of value 51 (0x33) will be forced to value of 50 and read back as 0x32. A write to both registers is required to update the bit time value.

NOTE: *The SLIC bit time will not be updated until a write of the SLCBTL has occurred.*

Address: $0044

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	BT12	BT11	BT10	BT9	BT8
Write:	▨	▨	▨					
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 14-8. SLIC Bit Time Register High (SLCBTH)

Address: $0045

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BT7	BT6	BT5	BT4	BT3	BT2	BT1	0
Write:								▨
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 14-9. SLIC Bit Time Register Low (SLCBTL)

BT — Bit Time Value

BT displays the number of SLIC clocks that equals one bit time in LIN mode (BTM = 0). For details of the use of the SLCBT registers in LIN mode for trimming of the internal oscillator, refer to **14.19 Oscillator Trimming with SLIC**.

BT sets the number of SLIC clocks that equals one bit time in byte transfer mode (BTM = 1). For details of the use of the SLCBT registers in BTM mode, refer to **14.18 Byte Transfer Mode Operation**.

14.6.6 SLIC State Vector Register

SLIC state vector register (SLCSV) is provided to substantially decrease the CPU overhead associated with servicing interrupts while under operation of a LIN protocol. It provides an index offset that is directly related to the LIN module’s current state, which can be used with a user supplied jump table to rapidly enter an interrupt service routine. This eliminates the need for the user to maintain a duplicate state machine in software.

Address: $0046

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	I3	I2	I1	I0	0	0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 14-10. SLIC State Vector Register (SLCSV)

READ: any time
WRITE: ignored

I[3:0] — Interrupt State Vector (Bits 5–2)

These bits indicate the source of the interrupt request that is currently pending.

14.6.6.1 LIN Mode Operation

Table 14-3 shows the possible values for the possible sources for a SLIC interrupt while in LIN mode operation (BTM = 0).

Table 14-3. Interrupt Sources Summary (BTM = 0)

SLCSV	I3	I2	I1	I0	Interrupt Source	Priority
$00	0	0	0	0	No Interrupts Pending	0 (Lowest)
$04	0	0	0	1	No-Bus-Activity	1
$08	0	0	1	0	TX Message Buffer Empty Checksum Transmitted	2
$0C	0	0	1	1	TX Message Buffer Empty	3
$10	0	1	0	0	RX Message Buffer Full Checksum OK	4
$14	0	1	0	1	RX Data Buffer Full No Errors	5
$18	0	1	1	0	Bit-Error	6
$1C	0	1	1	1	Receiver Buffer Overrun	7
$20	1	0	0	0	(RESERVED)	8
$24	1	0	0	1	Checksum Error	9
$28	1	0	1	0	Byte Framing Error	10
$2C	1	0	1	1	Identifier Received Successfully	11
$30	1	1	0	0	Identifier Parity Error	12
$34	1	1	0	1	Inconsistent-Synch-Field-Error	13
$38	1	1	1	0	Reserved	14
$3C	1	1	1	1	Wakeup	15 (Highest)

- No Interrupts Pending
  This value indicates that all pending interrupt sources have been serviced. In polling mode, the SLCSV is read and interrupts serviced until this value reads back 0. This source will not generate an interrupt of the CPU, regardless of state of the SLCIE bit.
- No Bus Activity (LIN specified error)
  The No-Bus-Activity condition occurs if no valid SYNCH BREAK FIELD or BYTE FIELD was received for more than $t_{TIMEOUT}$ (as defined in LIN Protocol Specification) since the reception of the last valid message.
- TX Message Buffer Empty — Checksum Transmitted
  When the entire LIN message frame has been transmitted successfully, complete with the appropriately selected checksum byte, this interrupt source is asserted. This source is used for all standard LIN message frames and the final set of bytes with extended LIN message frames.

- TX Message Buffer Empty
  This interrupt source indicates that all 8 bytes in the LIN message buffer have been transmitted with no checksum appended. This source is used for intermediate sets of 8 bytes in extended LIN message frames.
- RX Message Buffer Full — Checksum OK
  When the entire LIN message frame has been received successfully, complete with the appropriately selected checksum byte, and the checksum calculates correctly, this interrupt source is asserted. This source is used for all standard LIN message frames and the final set of bytes with extended LIN message frames. In order to clear this source, the SLCD0 register must be read.
- RX Data Buffer Full — No Errors
  This interrupt source indicates that 8 bytes have been received with no checksum byte and are waiting in the LIN message buffer. This source is used for intermediate sets of 8 bytes in extended LIN message frames. In order to clear this source, the SLCD0 register must be read.
- Bit Error
  A unit that is sending a bit on the bus also monitors the bus. A BIT_ERROR has to be detected at that bit time, when the bit value that is monitored is different from the bit value that is sent. The SLIC will terminate the data transmission at the next byte boundary, according to the LIN specification. Bit errors are not checked when the LIN bus is running at high speed due to the effects of physical layer round trip delay. Bit errors are fully checked at all LIN 2.0 compliant speeds of 20 kbps and below.
- Receiver Buffer Overrun Error
  This error is an indication that the receive buffer has not been emptied and additional bytes have been received, resulting in lost data.
- Reserved
  This source is reserved for future use.
- Checksum Error (LIN specified error)
  The checksum error occurs when the calculated checksum value does not match the expected value. If this error is encountered, it is important to verify that the correct checksum calculation method was employed for this message frame. Refer to the LIN specification for more details on the calculations.
- Byte Framing Error
  This error comes from the standard UART definition for byte encoding and occurs when the STOP bit is sampled and reads back as a 0. The STOP bit should always read as 1.
- Identifier Received Successfully
  This interrupt source indicates that a LIN identifier byte has been received with correct parity and is waiting in the LIN identifier buffer (SLCID). Upon

reading this interrupt source from the SLCSV register, the user can then decode the identifier in software to determine the nature of the LIN message frame. In order to clear this source, the SLCID register must be read.

- Identifier-Parity-Error
  A parity error in the identifier (i.e., corrupted identifier) will be flagged. Typical LIN slave applications do not distinguish between an unknown but valid identifier, and a corrupted identifier. However, it is mandatory for all slave nodes to evaluate in case of a known identifier all 8 bits of the ID-Field and distinguish between a known and a corrupted identifier. The received identifier value is reported in the SLCID register so that the user software can choose to acknowledge or ignore the parity error message.
- Inconsistent-Synch-Field-Error
  An Inconsistent-Synch-Field-Error has to be detected if a slave detects the edges of the SYNCH FIELD outside the given tolerance.
- Reserved
  This source is reserved for future use.
- Wakeup
  The wakeup interrupt source indicates that the SLIC module has entered SLIC run mode from SLIC wait or SLIC stop mode.

14.6.6.2 Byte Transfer Mode Operation

When byte transfer mode is enabled (BTM = 1), many of the interrupt sources for the SLCSV no longer apply, as they are specific to LIN operations. **Table 14-4** shows those interrupt sources which are applicable to BTM operations. The value of the SLCSV for each interrupt source remains the same, as well as the priority of the interrupt source.

Table 14-4. Interrupt Sources Summary (BTM = 1)

SLCSV	I3	I2	I1	I0	Interrupt Source	Priority
$00	0	0	0	0	No Interrupts Pending	0 (Lowest)
$0C	0	0	1	1	TX Message Buffer Empty	3
$14	0	1	0	1	RX Data Buffer Full No Errors	5
$18	0	1	1	0	Bit-Error	6
$1C	0	1	1	1	Receiver Buffer Overrun	7
$28	1	0	1	0	Byte Framing Error	10
$38	1	1	1	0	Reserved	14
$3C	1	1	1	1	Wakeup	15 (Highest)

- No Interrupts Pending
  This value indicates that all pending interrupt sources have been serviced. In polling mode, the SLCSV is read and interrupts serviced until this value reads back 0. This source will not generate an interrupt of the CPU, regardless of state of the SLCIE bit.
- TX Message Buffer Empty
  In byte transfer mode, this interrupt source indicates that the byte in the SLCID has been transmitted.
- RX Data Buffer Full — No Errors
  This interrupt source indicates that a byte has been received and is waiting in the SLCID register. In order to clear this source, the SLCID register must be read.
- Bit-Error
  A unit that is sending a bit on the bus also monitors the bus. A BIT_ERROR has to be detected at that bit time, when the bit value that is monitored is different from the bit value that is sent.
- Receiver Buffer Overrun Error
  The receiver buffer overrun error occurs when the number of bytes received by the SLIC module exceeds the value written to the SLCDLC. If this error is encountered, ensure that the correct data length value is associated with the proper identifier in software. This error can also be an indication that the receive buffer has not been emptied and additional byte(s) have been received, resulting in lost data.
- Byte Framing Error
  This error comes from the standard UART definition for byte encoding and occurs when the STOP bit is sampled and reads back as a 0. The STOP bit should always read as 1.
- Reserved
  This source is reserved for future use.
- Wakeup
  The wakeup interrupt source indicates that the SLIC module has entered SLIC run mode from SLIC wait or SLIC stop mode.

14.6.7 SLIC Data Length Code Register

The SLIC data length code register (SLCDLC) is the primary functional control register for the SLIC module during normal LIN operations. It contains the data length code of the message buffer, indicating how many bytes of data are to be sent or received, as well as the checksum mode control and transmit enabling bit.

Address: $0047

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TXGO	CHKMOD	DLC5	DLC4	DLC3	DLC2	DLC1	DLC0
Reset:	0	0	0	0	0	0	0	0

Figure 14-11. SLIC Data Length Code Register (SLCDLC)

TXGO — SLIC Transmit Go

This bit controls whether the SLIC module is sending or receiving data bytes. This bit is automatically reset to 0 once a transmit operation is complete or an error is encountered and transmission has been aborted.

1 = Initiate SLIC transmit

The SLIC assumes the user has loaded the proper data into the message buffer and will begin transmitting the number of bytes indicated in the SLCDLC bits. If the number of bytes is greater than 8, the first 8 bytes will be transmitted and an interrupt will be triggered (if unmasked) for the user to enter the next bytes of the message. If the number of bytes is 8 or fewer, the SLIC will transmit the appropriate number of bytes and automatically append the checksum to the transmission.

0 = SLIC receive data

CHKMOD — LIN Checksum Mode

CHKMOD is used to decide what checksum method to use for this message frame. Resets after error code or message frame complete.

1 = Checksum calculated without the identifier byte (LIN spec <= 1.3)
0 = Checksum calculated with the identifier byte included (SAE J2602/LIN 2.0)

DLC — Data Length Control Bits

The value of the bits indicate the number of data bytes in message. Values $00–$07 are for ’normal’ LIN messaging. Values $08–$3F are for "extended" LIN messaging.

Table 14-5. Data Length Control

DLC[5:0]	Message Data Length (Number of Bytes)
$00	1
$01	2
$02	3
...	...
$3D	62
$3E	63
$3F	64

14.6.8 SLIC Identifier and Data Registers

The SLIC identifier (SLCID) and data registers (SLCD[7:0]) comprise the transmit and receive buffer and are used to read/write the identifier and message buffer 8 data bytes. In BTM mode (BTM = 0), only the SLCID register is used to send and receive bytes, as only one byte is handled at any one time. The number of bytes to be read from or written to these registers is determined by the user software and written to the SLCDLC register. In order to obtain proper data, reads and writes to these registers must be made based on the proper length corresponding to a particular message. It is the responsibility of the user software to keep track of this value in order to prevent data corruption. For example, it is possible to read data from locations in the message buffer which contain erroneous or old data if the user software reads more data registers than were updated by the incoming message, as indicated in the SLCDLC.

NOTE: *An incorrect length value written to the SLCDLC register can result in the user software misreading or miswriting data in the message buffer. An incorrect length value might also result in SLIC error messages. For example, if a 4-byte message is to be received, but the user software incorrectly reports a 3-byte length to the DLC, the SLIC will assume the 4th data byte is actually a checksum value and attempt to validate it as such. If this value doesn't match the calculated value, an incorrect checksum error will occur. If it does happen to match the expected value, then the message would be received as a 3-byte message with valid checksum. Either case is incorrect behavior for the application and can be avoided by ensuring that the correct length code is used for each identifier.*

The first data byte received after the LIN identifier in a LIN message frame will be loaded into SLCD0. The next byte (if applicable) will be loaded into SLCD1, and so forth.

Address: $0048

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-12. SLIC Identifier Register (SLCID)

The SLIC identifier register is used to capture the incoming LIN identifier and when the SLCSV value indicates that the identifier has been received successfully, this register contains the received identifier value. If the incoming identifier contained a parity error, this register value will not contain valid data.

In byte transfer mode (BTM = 1), this register is used for sending and receiving each byte of data.

Address: $0049

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-13. SLIC Data Register 7 (SLCD7)

Address: $004A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-14. SLIC Data Register 6 (SLCD6)

Address: $004B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-15. SLIC Data Register 5 (SLCD5)

Address: $004C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-16. SLIC Data Register 4 (SLCD4)

Address: $004D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-17. SLIC Data Register 3 (SLCD3)

Address: $004E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-18. SLIC Data Register 2 (SLCD2)

Address: $004F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-19. SLIC Data Register 1 (SLCD1)

Address: $0050

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-20. SLIC Data Register 0 (SLCD0)

R — Read SLC Receive Data

T — Write SLC Transmit Data

14.7 Initialization/Application Information

The LIN specification defines a standard LIN "MESSAGE FRAME" as the basic format for transferring data across a LIN network. A standard MESSAGE FRAME is composed as shown in **Figure 14-21** (shown with 8 data bytes).

LIN transmits all data, identifier, and checksum characters as standard UART characters with 8 data bits, no parity, and 1 stop bit. Therefore, each byte has a length of 10 bits, including the start and stop bits. The data bits are transmitted least significant bit (LSB) first.

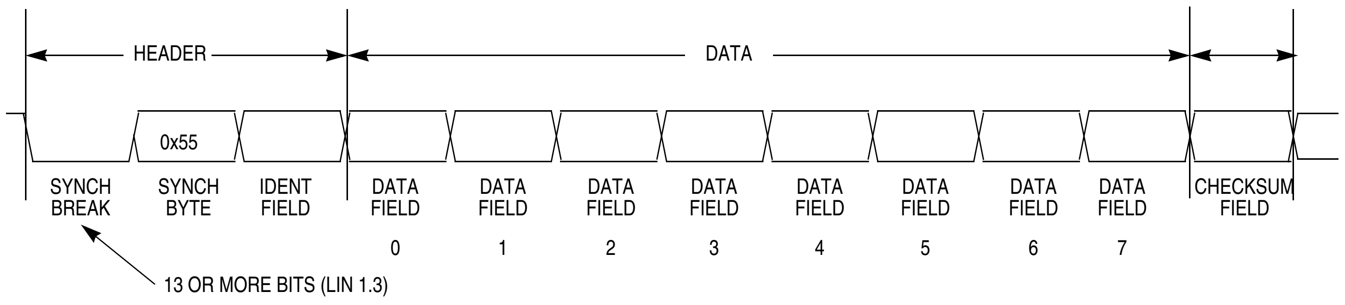


Figure 14-21. Typical LIN MESSAGE FRAME

14.7.1 LIN Message Frame Header

The HEADER section of all LIN messages is transmitted by the master node in the network and contains synchronization data, as well as the identifier to define what information is to be contained in the message frame. Formally, the header is comprised of three parts:

1. SYNCH BREAK
2. SYNCH BYTE (0x55)
3. IDENTIFIER FIELD

The first two components are present to allow the LIN slave nodes to recognize the beginning of the message frame and derive the bit rate of the master module.

The SYNCH BREAK allows the slave to see the beginning of a message frame on the bus. The SLIC module can receive a standard 10-bit break character for the SYNCH BREAK, or any break between 10–20 bit times in length. This encompasses the LIN requirement of 13 or more bits of length for the SYNCH BREAK character.

The SYNCH BYTE is always a 0x55 data byte, providing five falling edges for the slave to derive the bit rate of the master node.

The identifier byte indicates to the slave what is the nature of the data in the message frame. This data might be supplied from either the master node or the slave node, as determined at system design time. The slave node must read this identifier, check for parity errors, and determine whether it is to send or receive data in the data field.

More information on the HEADER is contained in **14.10.1 LIN Message Headers**.

14.7.2 LIN Data Field

The data field is comprised of standard bytes (8 data bits, no parity, 1 stop bit) of data, from 0–8 bytes for normal LIN frames and greater than 8 bytes for extended LIN frames. The SLIC module will either transmit or receive these bytes, depending upon the user code interpretation of the identifier byte. Data is always transmitted into the data field least significant byte (LSB) first.

The SLIC module can automatically handle up to 64 bytes in extended LIN message frames without significantly changing program execution.

14.7.3 LIN Checksum Field

The checksum field is a data integrity measure for LIN message frames, used to signal errors in data consistency. The LIN 1.3 checksum calculation only covers the data field, but the SLIC module also supports an enhanced checksum calculation which also includes the identifier field. For more information on the checksum calculation, refer to **14.16 LIN Data Integrity Checking Methods**.

14.7.4 SLIC Module Constraints

In designing a practical module, certain reasonable constraints must be placed on the LIN message traffic which are not necessarily explicitly specified in the LIN specification. The SLIC module presumes that:

- Timeout for no-bus-activity = 1 second.

14.8 SLCSV Interrupt Handling

Each change of state of the SLIC module is encoded in the SLIC state vector register (SLCSV). This is an efficient method of handling state changes, indicating to the user not only the current status of the SLIC module, but each state change will also generate an interrupt (if SLIC interrupts are enabled). For more detailed information on the SLCSV, please refer to **14.6.6 SLIC State Vector Register**.

In the software diagrams in the following subsections, when an interrupt is shown, the first step must always be reading the SLCSV register to determine what is the current status of the SLIC module. Likewise, when the diagrams indicate to "EXIT ISR", the final step to exiting the interrupt service routine is to clear the SLCF interrupt flag. This can only be done if the SLCSV has first been read, and in the case that data has been received (such as an ID byte or command message data) the SLCD has been read at least one time.

Once the SLCSV register is read, it will switch to the next pending state, so the user must be sure it is copied only once into a software variable at the beginning of the interrupt service routine in order to avoid inadvertently clearing a pending interrupt source. Additional decisions based on this value should be made from the software variable, rather than from the SLCSV itself.

After exiting the ISR, normal application code may resume. If the diagram indicates to "RETURN TO IDLE," it indicates that all processing for the current message frame has been completed. If an error was detected and the corresponding error code loaded into the SLCSV, any pending data in the data buffer will be flushed out and the SLIC returned to its idle state, seeking out the next message frame header.

14.9 SLIC Module Initialization Procedure

14.9.1 LIN Mode Initialization

The SLIC module does not require very much initialization, due to it’s self-synchronizing design. Since no prior knowledge of the bit rate is required in order to synchronize to the LIN bus, no programming of bit rate is required.

At initialization time, the user must configure:

- SLIC prescale register (SLIC digital receive filter adjustment).
- Wait clock mode operation.

The SLIC clock is the same as the CPU bus clock. The module is designed to provide better than 1% bit rate accuracy at the lowest value of the SLIC clock frequency and the accuracy improves as the SLIC clock frequency is increased. For this reason, it is advantageous to choose the fastest SLIC clock which is still within the acceptable operating range of the SLIC. Since the SLIC may be used with MCUs with internal oscillators, the tolerance of the oscillator must be taken into account to ensure that the SLIC clock frequency does not exceed the bounds of the SLIC clock operating range. This is especially important if the user wishes to use the oscillator untrimmed, where process variations might result in MCU frequency offsets of ±25%.

The acceptable range of SLIC clock frequencies is 2–8 MHz to guarantee LIN operations with greater than 1.5% accuracy across the 1–20 kbps range of LIN bit rates. The user must ensure that the fastest possible SLIC clock frequency never exceeds 8 MHz or that the slowest possible SLIC clock never falls below 2 MHz under worst case conditions. This would include, for example, oscillator frequency variations due to untrimmed oscillator tolerance, temperature variation, or supply voltage variation.

In order to initialize the SLIC module into LIN operating mode, the user should perform the following steps prior to needing to receive any LIN message traffic. These steps assume the MCU has been reset either by a power-on reset (POR) or any other MCU reset mechanism.

The steps for SLIC Initialization for LIN operation are:

1. Write SLCC1 to clear INITREQ.
2. When INITACK = 0, write SLCC1 & SLCC2 with desired values for:
   a. SLCWCM — Wait clock mode (default = leaving SLIC clock running when in CPU wait).
3. Write SLCP to set up prescalers for:
   a. RXFP — Digital receive filter clock prescaler (default = SLIC divided by 3).
4. Enable the SLIC module by writing SLCC2:
   a. SLCE = 1 to place SLIC module into run mode.
   b. BTM = 0 to disable byte transfer mode (default).
5. Write SLCC1 to enable SLIC interrupts (if desired).

14.9.2 Byte Transfer Mode Initialization

Bit rate synchronization is handled automatically in LIN mode, using the synchronization data contained in each LIN message to derive the desired bit rate. In byte transfer mode (BTM = 1); however, the user must set up the bit rate for communications using the clock selection, prescaler, and SLCBT register.

More information on byte transfer mode is described in **14.18 Byte Transfer Mode Operation**, including the performance parameters on recommended maximum speeds, bit time resolution, and oscillator tolerance requirements.

Once the desired settings of prescalers and bit time are determined, the SLIC Initialization for BTM operation is virtually identical to that of LIN operation.

The steps are:

1. Write SLCC1 to clear INITREQ.
2. When INITACK = 0, write SLCC2 with desired values for:
   a. SLCWCM — Wait clock mode (default = leaving SLIC clock running when in CPU wait).
3. Write SLCICP to set up prescalers for:
   a. RXFP — Digital receive filter clock prescaler (default = SLIC divided by 3).
4. Enable the SLIC module by writing SLCC2:
   a. SLCE = 1 to place SLIC module into run mode.
   b. BTM = 1 to enable byte transfer mode (default = disabled).
5. Write SLCC1 to enable SLIC interrupts (if desired).

14.10 Handling LIN Message Headers

Figure 14-22 shows how the SLIC module deals with incoming LIN message headers.

14.10.1 LIN Message Headers

All LIN message frame headers are comprised of three components:

- The first is the SYNCHRONIZATION BREAK (SYNCH BREAK) symbol, which is a dominant (low) pulse at least 13 or more bit times long, followed by a recessive (high) synchronization delimiter of at least one bit time. In LIN 2.0, this is allowed to be 10 or more bit times in length.
- The second part is called the SYNCHRONIZATION FIELD (SYNCH FIELD) and is a single byte with value 0x55. This value was chosen as it is the only one which provides a series of five falling (recessive to dominant) transitions on the bus.
- The third section of the message frame header is the IDENTIFIER FIELD (ID). The identifier is covered more in **14.11 Handling Command Message Frames** and **14.12 Handling Request LIN Message Frames**.

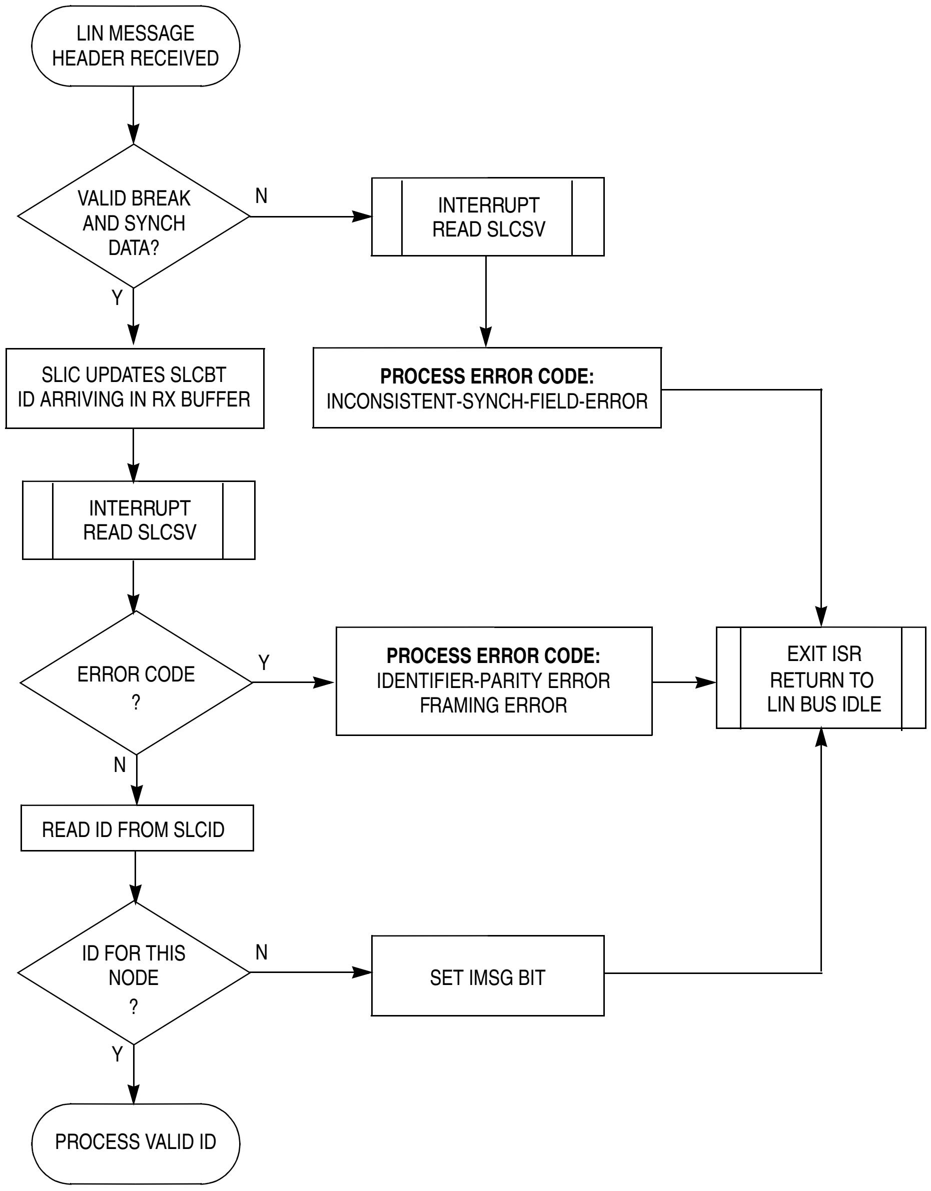

LIN MESSAGE HEADER RECEIVED
VALID BREAK AND SYNCH DATA?
N
Y
INTERRUPT READ SLCSV
SLIC UPDATES SLCBT ID ARRIVING IN RX BUFFER
PROCESS ERROR CODE: INCONSISTENT-SYNCH-FIELD-ERROR
INTERRUPT READ SLCSV
ERROR CODE ?
Y
N
PROCESS ERROR CODE: IDENTIFIER-PARITY ERROR FRAMING ERROR
EXIT ISR RETURN TO LIN BUS IDLE
READ ID FROM SLCID
ID FOR THIS NODE ?
N
Y
SET IMSG BIT
PROCESS VALID ID

Figure 14-22. Handling LIN Message Headers

The SLIC automatically reads the incoming pattern of the SYNCHRONIZATION BREAK and FIELD and determines the bit rate of the LIN data frame, as well as checking for errors in form and discerning between a genuine BREAK/FIELD combination and a similar byte pattern somewhere in the data stream. Once the header has been verified to be valid and has been processed, the SLIC module updates the SLIC bit time register (SLICBT) with the value obtained from the SYNCH FIELD and begins to receive the ID.

If there are errors in the SYNCH BREAK/FIELD pattern, then an interrupt is generated. If unmasked, it will trigger an MCU interrupt request and the resulting code in the SLIC state vector register (SLCSV) will be an "Inconsistent-Synch-Field-Error," based on the LIN protocol specification.

Once the ID for the message frame has been received, an interrupt is generated by the SLIC and will trigger an MCU interrupt request if unmasked. At this point, it might be possible that the ID was received with errors such as a parity error (based on the LIN specification) or a byte framing error. If the ID did not have any errors, it will be copied into the SLCD for the software to read. The SLCSV will indicate the type error or that the ID was received correctly.

In a LIN system, the meaning and function of all messages, and therefore all message identifiers, is pre-defined by the system designer. This information can be collected and stored in a standardized format file, called a Configuration Language Description (CLD) file. In using the SLIC module, it is the responsibility of the user software to determine the nature of the incoming message, and therefore how to further handle that message.

The simplest case is when the SLIC receives a message which the user software determines is of no interest to the application. In other words, the slave node does not need to receive or transmit any data for this message frame. This might also apply to messages with zero data bytes (which is allowed by the LIN specification). At this point, the user can set the IMSG control bit, and exit the interrupt service routine by clearing the SLCIF flag. Because there is no data to be sent or received, the SLIC will not generate another interrupt until the next message frame header or bus goes idle long enough to trigger a "No-Bus-Activity" error according to the LIN specification.

NOTE: *IMSG will prevent another interrupt from occurring for the current message frame; however, if data bytes are appearing on the bus they may be received and copied into the message buffer. This will delete any previous data which might have been present in the buffer, even though no interrupt is triggered to indicate the arrival of this data.*

At the time the ID is read, the user might also choose to read the SLCBT register and copy this value out to an application variable. This data can then be used at a time appropriate to both the application software and the LIN communications to adjust the trim of the internal oscillator. This operation must be handled very carefully to avoid adjusting the base timing of the MCU at the wrong time, adversely affecting the operation of the SLIC module or of the application itself. More information about this is contained in **14.19 Oscillator Trimming with SLIC**.

If the user software determines that the ID read out of the SLCD corresponds to a command or request message for which this node needs to receive or transmit data (respectively), it will then move on to procedures described in **14.11 Handling Command Message Frames** and **14.12 Handling Request LIN Message Frames**.

For clarification, in this document, "command" messages will refer to any message frame where the SLIC module is receiving data bytes and "request" messages refer to message frames where the SLIC module will be expected to transmit data bytes. This is a generic description and should not be confused with the terminology in the LIN specification. The LIN use of the terms "command" and "request" have the same basic meaning, but are limited in scope to specific identifier values of 0x3C and 0x3D. In the SLIC module documentation, these terms have been used to describe these functional types of messages, regardless of the specific identifier value used.

14.10.2 Possible Errors on Message Headers

Possible errors on message headers are:

- Inconsistent-Synch-Field-Error
- Identifier-Parity-Error
- Framing Error

14.11 Handling Command Message Frames

Figure 14-23 shows how to handle command message frames, where the SLIC module is receiving data from the master node.

Command message frames refer to LIN messages frames where the master node is ’commanding’ the slave node to do something. The implication is that the slave will then be receiving data from the master for this message frame. This can be a standard LIN message frame of 1–8 data bytes, a reserved LIN system message (using 0x3C identifier), or an extended command message frame utilizing the reserved 0x3E user defined identifier or perhaps the 0x3F LIN reserved extended identifier. The SLIC module is capable of handling message frames containing up to 64 bytes of data, while still automatically calculating and/or verifying the checksum.

14.11.1 Standard Command Message Frames

Once the application software has read the incoming identifier and determined that it is a valid identifier which cannot be ignored using the IMSG bit, it must determine if this message frame is a command message frame or a request message frame. (i.e., should the application receive data from the master or send data back to the master?)

The first case, shown in **Figure 14-23** deals with command messages, where the SLIC will be receiving data from the master node. If the received identifier corresponds to a standard LIN command frame (i.e., 1–8 data bytes), the user must then write the number of bytes (determined by the system designer and directly linked with this particular identifier) corresponding to the length of the message frame into the SLCDLC register. The two most significant bits of this register are used for special control bits describing the nature of this message frame.

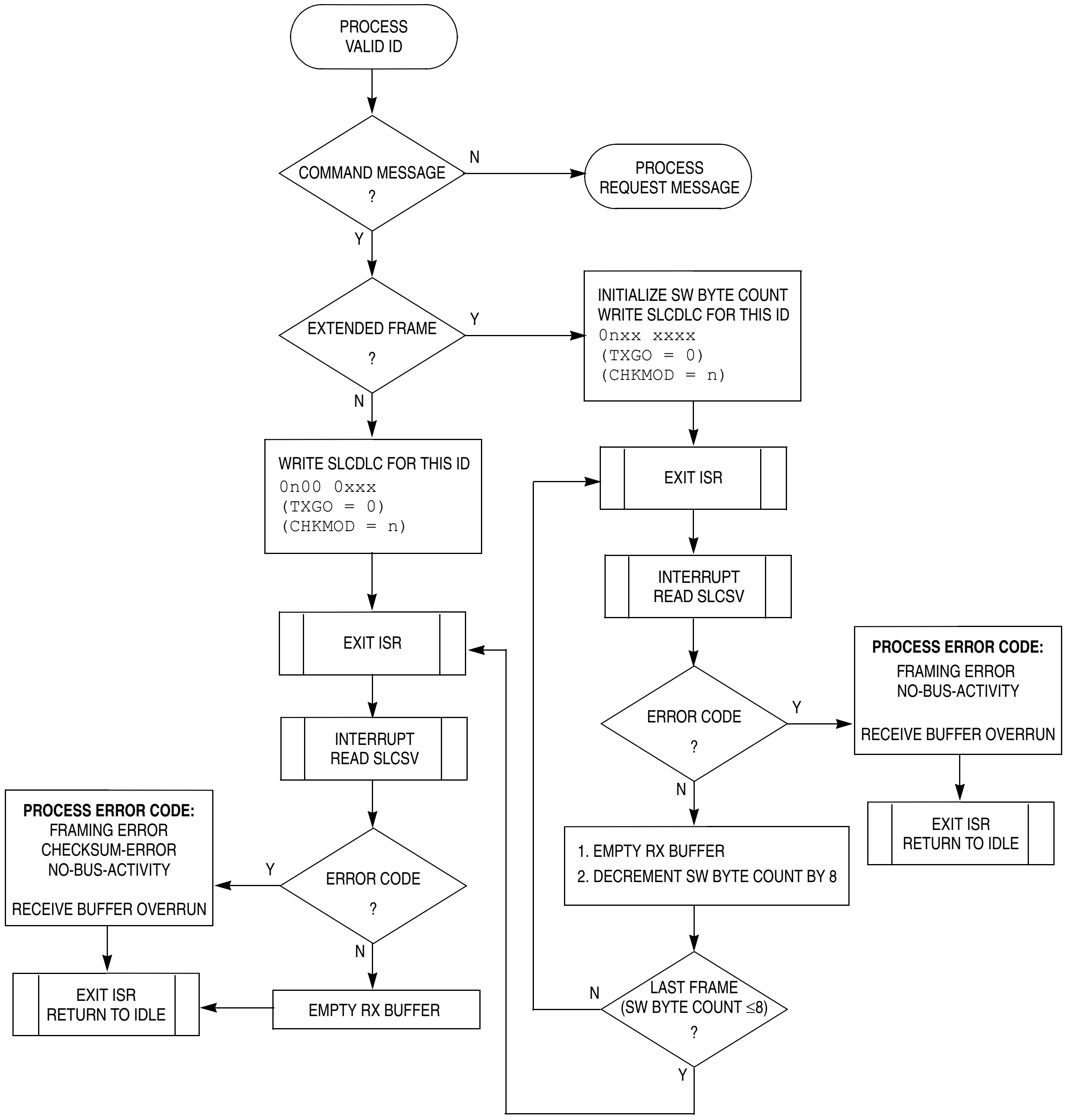


Figure 14-23. Handling Command Messages (Data Receive)

The SLIC transmit go (TXGO) bit should be 0 for command frames, indicating to the SLIC that data is coming from the master. The checksum mode control (CHKMOD) bit allows the user to select which method of checksum calculation is desired for this message frame. The LIN 1.3 checksum does not include the identifier byte in the calculation, while the SAE version does include this byte. Since the identifier is already received by the SLIC by this time, the default is to include it in the calculation. If a LIN 1.3 checksum is desired, a 1 in the CHKMOD bit will reset the checksum circuitry to begin calculating the checksum on the first data byte. Using the CHKMOD bit in this way allows the SLIC to receive messages with either method of data consistency check and change on a frame-by-frame basis. If a system uses both types of data consistency checking methods, the software must simply change the setting of this bit based on the identifier of each message. If the network only uses one type of check, the CHKMOD bit can be set as a constant value in the user's code. If CHKMOD is not written on each frame, care must be taken not to accidentally modify the bit when writing the data length and TXGO bits. This is especially true if using C code without carefully inspecting the output of the compiler and assembler.

The control bits and data length code are contained in one register, allowing the user to maximize the efficiency of the identifier processing by writing a single byte value to indicate the nature of the message frame. This allows very efficient identifier processing code, which is important in a command frame, as the master node can be sending data immediately following the identifier byte which might be as little as one byte in length. The SLIC module uses a separate internal storage area for the incoming data bytes, so there is no danger of losing incoming data, but the user should spend as little time as possible within the ISR to ensure that the application or other ISRs are able to use the majority of the CPU bandwidth.

The identifier must be processed in a maximum of 2 byte times on the LIN bus to ensure that the ISR completes before the checksum would be received for the shortest possible message. This should be easily achievable, as the only operations required are to read the SLCID register and look up the checksum method, data length, and command/request state of that identifier, then write that value to the SLCDLC. This can be easily streamlined in code with a lookup table of identifiers and corresponding SLCDLC bytes.

14.11.2 Extended Command Message Frames

Handling of extended frames is very similar to handling of standard frames, providing that the length is less than or equal to 64 bytes. Since the SLIC module can only receive 8 bytes at a time, the receive buffer must be emptied periodically for long message frames. This is not standard LIN operation, and is likely only to be used for downloading calibration data or reprogramming FLASH devices in a factory or service facility, so the added steps required for processing are not as critical to performance. During these types of operations, the application code is likely very limited in scope and special adjustments can be made to compensate for added message processing time.

For extended command frames, the data length is still written one time at the time the identifier is decoded, along with the TXGO and CHKMOD bits. When this is done, a software counter must also be initialized to keep track of how many bytes are expected to be received in the message frame. The ISR completes, clearing the SLCF flag, and resumes application execution. The SLIC will generate an interrupt, if unmasked, after 8 bytes are received or an error is detected. At this interrupt, the SLCSV will indicate an error condition (in case of framing error, idle bus) or that the receive buffer is full. If the data is successfully received, the user must then empty the buffer by reading SLCD7-SLCD0 and then subtract 8 from the software byte count. When this software counter reaches 8 or fewer, the remaining data bytes will fit in the buffer and only one interrupt should occur. At this time, the final interrupt may be handled normally, continuing to use the software counter to read the proper number of bytes from the appropriate SLCD registers.

NOTE: *Do not write the SLCDLC register more than one time per LIN message frame. The SLIC tracks the number of sent or received bytes based on the value written to this register at the beginning of the data field and rewriting this register will corrupt the checksum calculation and cause unpredictable behavior in the SLIC module. The application software must track the number of sent or received bytes to know what the current byte count in the SLIC is. If programming in C, make sure to use the VOLATILE modifier on this variable (or make it a global variable) in order to ensure that it keeps it’s value between interrupts.*

14.11.3 Possible Errors on Command Message Data

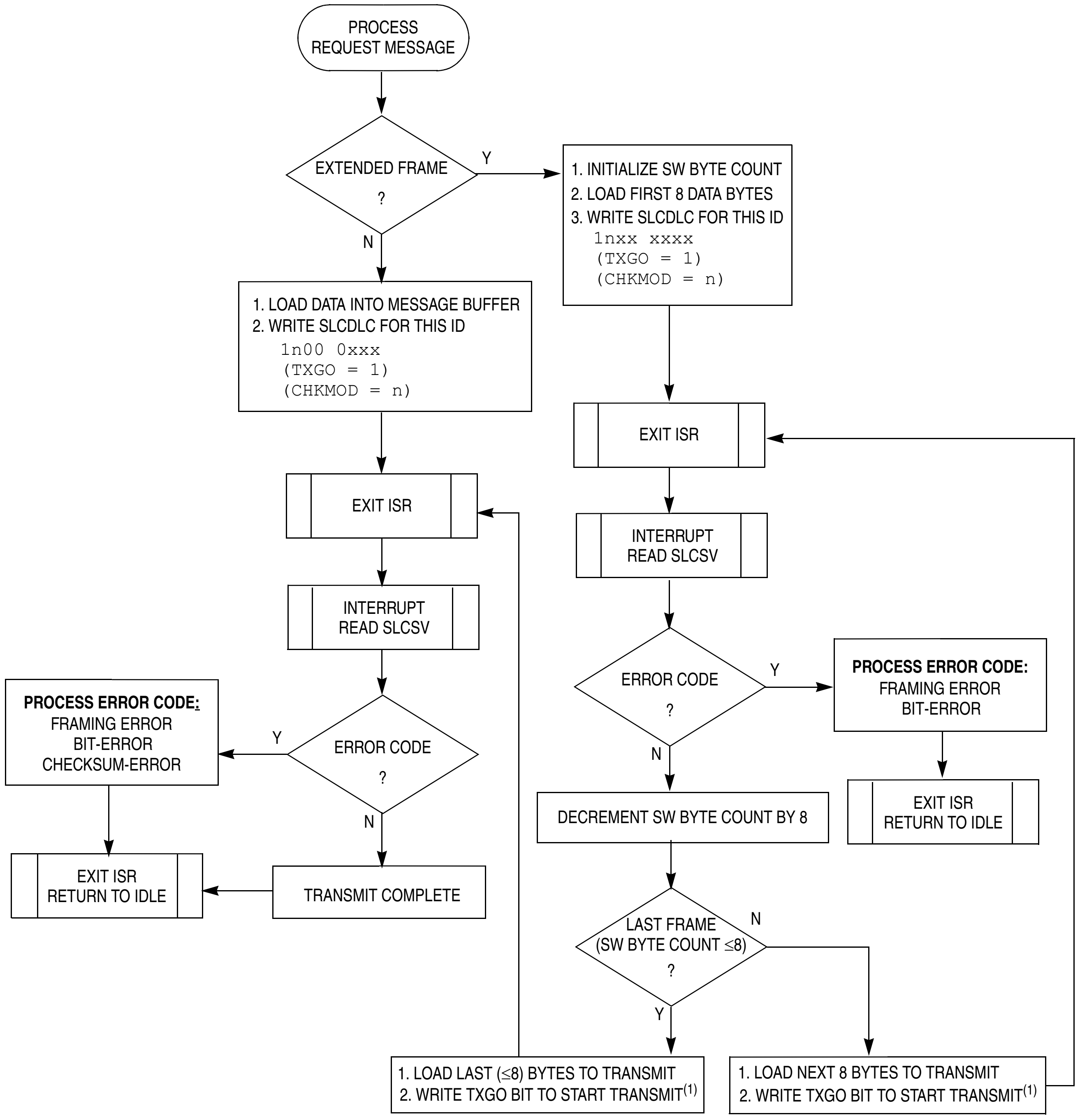
Possible errors on command message data are:

- Framing Error
- Checksum-Error (LIN specified error)
- No-Bus-Activity (LIN specified error)
- Receiver Buffer Overrun Error

14.12 Handling Request LIN Message Frames

Figure 14-24 shows how to handle request message frames, where the SLIC module is sending data to the master node.

Request message frames refer to LIN messages frames where the master node is ’requesting’ the slave node to supply information. The implication is that the slave will then be transmitting data to the master for this message frame. This can be a standard LIN message frame of 1–8 data bytes, a reserved LIN system message (using 0x3D identifier), or an extended request message frame utilizing the reserved 0x3E identifier or perhaps the 0x3F LIN reserved extended identifier. The SLIC module is capable of handling request message frames containing up to 64 bytes of data, while still automatically calculating and/or verifying the checksum.


PROCESS REQUEST MESSAGE
EXTENDED FRAME ?
Y
N
1. INITIALIZE SW BYTE COUNT
2. LOAD FIRST 8 DATA BYTES
3. WRITE SLCDLC FOR THIS ID
1nxx xxxx
(TXGO = 1)
(CHKMOD = n)
1. LOAD DATA INTO MESSAGE BUFFER
2. WRITE SLCDLC FOR THIS ID
1n00 0xxx
(TXGO = 1)
(CHKMOD = n)
EXIT ISR
EXIT ISR
INTERRUPT READ SLCSV
INTERRUPT READ SLCSV
ERROR CODE ?
Y
N
PROCESS ERROR CODE: FRAMING ERROR BIT-ERROR
EXIT ISR RETURN TO IDLE
PROCESS ERROR CODE: FRAMING ERROR BIT-ERROR CHECKSUM-ERROR
ERROR CODE ?
Y
N
DECREMENT SW BYTE COUNT BY 8
EXIT ISR RETURN TO IDLE
TRANSMIT COMPLETE
LAST FRAME (SW BYTE COUNT ≤8) ?
N
Y
1. LOAD LAST (≤8) BYTES TO TRANSMIT
2. WRITE TXGO BIT TO START TRANSMIT(1)
1. LOAD NEXT 8 BYTES TO TRANSMIT
2. WRITE TXGO BIT TO START TRANSMIT(1)

Note 1. When writing TXGO bit only, ensure that CHKMOD and data length values are not accidentally modified.

Figure 14-24. Handling Request LIN Message Frames

14.12.1 Standard Request Message Frames

Dealing with request messages with the SLIC is very similar to dealing with command messages, with one important difference. Since the SLIC is now to be transmitting data in the LIN message frame, the user software must load the data to be transmitted into the message buffer prior to initiating the transmission. This means an extra step is taken inside the interrupt service routine once the identifier has been decoded and is determined to be an ID for a request message frame.

Figure 14-24 deals with request messages, where the SLIC will be transmitting data to the master node. If the received identifier corresponds to a standard LIN command frame (i.e., 1-8 data bytes), the message processing is very simple. The user must load the data to be transmitted into the transmit buffer by writing it to the SLCD registers. The first byte to be transmitted on the LIN bus should be loaded into SLCD0, then SLCD1 for the second byte, etc. Once all of the bytes to be transmitted are loaded in this way, a single write to the SLCDLC register will allow the user to encode the number of data bytes to be transmitted (1–8 bytes for standard request frames), set the proper checksum calculation method for the data (CHKMOD), as well as signal the SLIC that the buffer is ready by writing a 1 to the TXGO bit. The TXGO bit will remain set to 1 until the buffer is sent successfully or an error is encountered, signaling to the application code that the buffer is in process of transmitting. In cases of 1–8 data bytes only being sent (standard LIN request frames), the SLIC automatically calculates and transmits the checksum byte at the end of the message frame. The user can exit the ISR once the SLCDLC register has been written and the SLCF flag has been cleared.

The next SLIC interrupt which occurs, if unmasked, will indicate the end of the request message frame and will either indicate that the frame was properly transmitted or that an error was encountered during transmission. Refer to **14.12.4 Possible Errors on Request Message Data** for more detailed explanation of these possible errors. This interrupt also signals to the application that the message frame is complete and all data bytes and the checksum value have been properly transmitted onto the bus.

The SLIC module cannot begin to transmit the data until the user writes a 1 to the TXGO bit, indicating that data is ready. If the user writes the TXGO bit without loading data into the transmit buffer, whatever data is in storage will be transmitted, where the number of bytes transmitted is based on the data length value in the data length register. Similarly, if the user writes the wrong value for the number of data bytes to transmit, the SLIC will transmit that number of bytes, potentially transmitting garbage data onto the bus. The checksum calculation is performed based on the data transmitted, and will therefore still be calculated.

The identifier must be processed, data must be loaded into the transmit buffer, and the SLCDLC value written to initiate data transmission in a certain amount of time, based on the LIN specification. If the user waits too long to start transmission, the master node will observe an idle bus and trigger a Slave Not Responding error condition. The same error can be triggered if the transmission begins too late and does not complete before the message frame times out. Refer to the LIN specification for more details on timing constraints and requirements for LIN slave devices. This is especially important when dealing with extended request frames, when the data must be loaded in 8 byte sections (maximum) to be transmitted at each interrupt.

14.12.2 Extended Request Message Frames

Handling of extended frames is very similar to handling of standard frames, providing that the length is less than or equal to 64 bytes. Since the SLIC module can only transmit 8 bytes at a time, the transmit buffer must be loaded periodically for extended message frames. This is not standard LIN operation, and is likely only to be used for special cases, so the added steps required for processing should not be as critical to performance. During these types of operations, the application code is likely very limited in scope and special adjustments can be made to compensate for added message processing time.

For extended request frames, the data length is still written only one time, at the time the identifier is decoded, along with the TXGO and CHKMOD bits, after the first 8 data bytes are loaded into the transmit buffer. When this is done, a software counter must also be initialized to keep track of how many bytes are to be transmitted in the message frame. The ISR completes, clearing the SLCF flag, and resumes application execution. The SLIC will generate an interrupt, if unmasked, after 8 bytes are transmitted or an error is detected. At this interrupt, the SLCSV will indicate an error condition (in case of framing error or bit error) or that the transmit buffer is empty. If the data is transmitted successfully, the user must then subtract 8 from the software byte count, load the next 8 bytes into the SLCD registers, and write a 1 to the TXGO bit to tell the SLIC that the buffers are loaded and transmission can commence. When this software counter reaches 8 or fewer, the remaining data bytes will fit in the transmit buffer and the SLIC will automatically append the checksum value to the frame after the last byte is sent.

NOTE: *Do not write the CHKMOD or data length values in the SLCDLC register more than one time per message frame. The SLIC tracks the number of sent or received bytes based on the value written to this register at the beginning of the data field and rewriting this register will corrupt the checksum calculation and cause unpredictable behavior in the SLIC module. The application software must track the number of sent or received bytes to know what the current byte count in the SLIC is. If programming in C, make sure to use the VOLATILE modifier on this variable (or make it a global variable) in order to ensure that it keeps it's value between interrupts.*

14.12.3 Transmit Abort

The transmit abort bit (TXABRT) in SLCC1 allows the user to cease transmission of data on the next byte boundary. When this bit is set to 1, it will finish transmitting the byte currently being transmitted, then cease transmission. Once the transmission is successfully aborted, the TXABRT bit will automatically be reset by the SLIC to 0. If the SLIC is not in process of transmitting at the time TXABRT is written to 1, there is no effect and TXABRT will read back as 0.

14.12.4 Possible Errors on Request Message Data

Possible errors on request message data are:

- Framing Error.
- Checksum-Error (LIN specified error).
- Bit-Error.

14.13 Handling IMSG to Minimize Interrupts

The IMSG feature is designed to minimize the number of interrupts required to maintain LIN communications. On a network with many slave nodes, it is very likely that a particular slave will observe messages which are not intended for that node. When the SLIC module detects any message header, it synchronizes to that message frame and bit rate, then interrupts the CPU once the identifier byte has been successfully received and parity checked. At this time, if the software determines that the message may be ignored, the IMSG bit may be set to indicate to the module that the data field of the message frame is to be ignored and no additional interrupts should be generated until the next valid message header is received. The bit is automatically reset to 0 once the current message frame is complete and the LIN bus returns to idle state. This reduces the load on the CPU and allows the application software to immediately begin performing any operations which might otherwise not be allowed while receiving messaging.

NOTE: *IMSG will prevent another interrupt from occurring for the current message frame, however if data bytes are appearing on the bus they may be received and copied into the message buffer. This will delete any previous data which might have been present in the buffer, even though no interrupt is triggered to indicate the arrival of this data.*

14.14 Sleep and Wakeup Operation

The SLIC module itself has no special sleep mode, but does support low-power modes and wake-up on network activity. For low-power operations, the user must select whether or not to allow the SLIC clock to continue operating when the MCU issues a wait instruction through the SLC wait clock mode (SLCWCM) bit in SLCC1 register. If SLCWCM = 1, the SLIC will enter SLIC STOP mode when the MCU executes a WAIT instruction. If SLCWCM = 0, the SLIC will enter SLIC WAIT mode when the MCU executes a WAIT instruction. For more information on these modes, as well as wakeup options from these modes, please refer to **14.3 Modes of Operation**.

When network activity occurs, the SLIC module will wake the MCU out of stop or wait mode, and return the SLIC module to SLIC run mode. The SLCSV register will indicate wakeup as the interrupt source so that the user knows that the SLIC module brought the MCU out of stop or wait.

In a LIN system, a system message is generally sent to all nodes to indicate that they are to enter low-power network sleep mode. Once a node enters sleep mode, it waits for outside events, such as switch or sensor inputs or network traffic to bring it out of network sleep mode. If the node using the SLIC module is awakened by a source other than network traffic, such as a switch input, the LIN specification requires this node to issue a wake-up signal to the rest of the network. The SLIC module supports this feature using the WAKETX bit in the SLCC2 register. The user software may set this bit and one LIN wake-up signal is immediately transmitted on the bus, then the bit is automatically cleared by the SLIC module. If another wake-up signal is required to be sent, the user must set the WAKETX bit again.

In a LIN system, the LIN physical interface can often also provide an output to the $\overline{\text{IRQ}}$ pin to provide a wake-up mechanism on network activity. The physical layer might also control voltage regulation supply to the MCU, cutting power to the MCU when the physical layer is placed in its low-power mode. The user must take care to ensure that the interaction between the physical layer, $\overline{\text{IRQ}}$ pin, SLIC transmit and receive pins, and power supply regulator is fully understood and designed to ensure proper operation.

14.15 Polling Operation

It is possible to operate the SLIC module in polling mode, if desired. The primary difference is that the SLIC interrupt request should not be enabled (SLCIE = 0). The SLCSV will update and operate properly and interrupt requests will be indicated with the SLCF flag, which can be polled to determine status changes in the SLIC module. It is required that the polling rate be fast enough to ensure that SLIC status changes be recognized and processed in time to ensure that all application timings can be met.

14.16 LIN Data Integrity Checking Methods

The SLIC module supports two different LIN-based data integrity options:

- The first option supports LIN 1.3 and older methods of checksum calculations.
- The second option supports an optional additional enhanced checksum calculation which has greater data integrity coverage.

The LIN 1.3 and earlier specifications transmit a checksum byte in the "CHECKSUM FIELD" of the LIN message frame. This CHECKSUM FIELD contains the inverted modulo-256 sum over all data bytes. The sum is calculated by an "ADD with Carry" where the carry bit of each addition is added to the least significant bit (LSB) of it’s resulting sum. This guarantees security also for the

MSBs of the data bytes. The sum of modulo-256 sum over all data bytes and the checksum byte must be’0xFF’.

An optional checksum calculation can also be performed on a LIN data frame which is very similar to the LIN 1.3 calculation, but with one important distinction. This enhanced calculation simply includes the identifier field as the first value in the calculation, whereas the LIN 1.3 calculation begins with the least significant byte of the data field (which is the first byte to be transmitted on the bus). This enhanced calculation further ensures that the identifier field is correct and ties the identifier and data together under a common calculation, ensuring greater reliability.

In the SLIC module, either checksum calculation can be performed on any given message frame by simply writing or clearing the CHKMOD bit in the SLCDLC register, as desired, when the identifier for the message frame is decoded. The appropriate calculation for each message frame should be decided at system design time and documented in the LIN description file, indicating to the user which calculation to use for a particular identifier.

14.17 High-Speed LIN Operation

High-speed LIN operation does not necessarily require any reconfiguration of the SLIC module, depending upon what maximum LIN bit rate is desired. Several factors affect the performance of the SLIC module at LIN speeds higher than 20 kbps, all of which are functions of the speed of the SLIC clock and the prescaler of the digital filter. The tightest constraint comes from the need to maintain ±1.5% accuracy with the master node timing. This requires that the SLIC module be able to sample the incoming data stream accurately enough to guarantee that accuracy. **Table 14-6** shows the maximum LIN bit rates allowable in order to maintain this accuracy.

Table 14-6. Maximum LIN Bit Rates for High-Speed Operation

SLIC Clock (MHz)	Maximum LIN Bit Rate for ±1% SLIC Accuracy (Bits / Second)	Maximum LIN Bit Rate for ±1.5% SLIC Accuracy (Bits / Second)
8	80,000	120,000
6.4	64,000	96,000
4.8	48,000	72,000
4	40,000	60,000
3.2	32,000	48,000
2.4	24,000	36,000
2	20,000	30,000

The above numbers assume a perfect input waveforms into the SLCRX pin, where 1 and 0 bits are of equal length and are exactly the correct length for the appropriate speed. Factors such as physical layer wave shaping and ground shift can affect the symmetry of these waveforms, causing bits to appear shortened or lengthened as seen by the SLIC module. The user must take these factors into account and base the maximum speed upon the shortest possible bit time that the SLIC module may observe, factoring in all physical layer effects. On some LIN physical layer devices it is possible to turn off wave shaping circuitry for high-speed operation, removing this portion of the physical layer error.

The digital receive filter can also affect high speed operation if it is set too low and begins to filter out valid message traffic. Under ideal conditions, this will not happen, as the digital filter maximum speeds allowable are higher than the speeds allowed for ±1.5% accuracy. If the digital receive filter prescaler is set to divide-by-4; however, the filter delay is very close to the ±1.5% accuracy maximum bit time.

For example, with a SLIC clock of 4 MHz, the SLIC module is capable of maintaining ±1.5% accuracy up to 60,000 bps. If the digital receive filter prescaler is set to divide-by-4, this means that the filter will only pass message traffic which is 62,500 bps or slower under ideal circumstances. This is only a difference of 2,500 bps (4.17% of the nominal valid message traffic speed). In this case, the user must ensure that with all errors accounted for, no bit will appear shorter than 16 μs (1 bit at 62,500 bps) or the filter will block that bit. This is far too narrow a margin for safe design practices. The better solution would be to reduce the filter prescaler, increasing the gap between the filter cut-off point and the nominal speed of valid message traffic. Changing the prescaler to divide by 2 in this example gives a filter cut-off of 125,000 bps, which is 60,000 bps faster than the nominal speed of the LIN bus and much less likely to interfere with valid message traffic.

To ensure that all valid messages pass the filter stage in high-speed operation, it is best to ensure that the filter cut-off point is at least 2 times the nominal speed of the fastest message traffic to appear on the bus. Refer to **Table 14-6** for a more complete list of the digital receive filter delays as they relate to the maximum LIN bus frequency. **Table 14-7** repeats much of the data found in **Table 14-6**; however, the filter delay values have been converted to the frequency domain.

Table 14-7. Maximum LIN Bit Rates for High-Speed Operation Due to Digital Receive Filter

SLIC Clock (MHz)	Maximum LIN Bit Rate for ±1.5% SLIC Accuracy (for Master-Slave Communication (Bits / Second) DIGITAL RX FILTER NOT CONSIDERED	Maximum LIN Bit Rate with Digital RX Filter Set to ÷4 (Bits / Second)	Maximum LIN Bit Rate with Digital RX Filter Set to ÷3 (Bits / Second)	Maximum LIN Bit Rate with Digital RX Filter Set to ÷2 (Bits / Second)	Maximum LIN Bit Rate with Digital RX Filter Set to ÷1 (Bits / Second)
		THESE PRESCALERS NOT RECOMMENDED FOR HIGH-SPEED LIN OPERATION			
8	120,000	125,000	166,667	250,000	500,000
6.4	96,000	100,000	133,333	200,000	400,000
4.8	72,000	75,000	100,000	150,000	300,000
4	60,000	62,500	83,333	125,000	250,000
3.2	48,000	50,000	66,667	100,000	200,000
2.4	36,000	37,500	50,000	75,000	150,000
2	30,000	31,250	41,667	62,500	125,000

14.18 Byte Transfer Mode Operation

This subsection describes the operation and limitations of the optional UART-like byte transfer mode (BTM). This mode allows sending and receiving individual bytes, but changes the behavior of the SLCBT registers (now read/write registers) and locks the SLCDLC to 1 byte data length. The SLCBT value now becomes the bit time reference for the SLIC, where the software sets the length of one bit time rather than the SLIC module itself. This is similar to an input capture/output compare (IC/OC) count in a timer module, where the count value represents the number of SLIC clock counts in one bit time.

Byte transfer mode assumes that the user has a very stable, precise oscillator, resonator, or clock reference input into the MCU and is therefore not appropriate for use with internal oscillators. There is no synchronization method available to the user in this mode and the user must tell the SLIC how many clock counts comprise a bit time. **Figure 14-25**, **Figure 14-26**, **Figure 14-27**, and **Figure 14-28** show calculations to determine the SLCBT value for different settings.

In the example in **Figure 14-25**, the user should write 0x16, as a write of 0x15 (decimal value of 21) would automatically revert to 0x14, resulting in transmitted bit times that are 1.33 SLIC clock periods too short rather than 0.667 SLIC clock periods too long. The optimal choice, which gives the smallest resolution error, is the closest even number of SLIC clocks to the exact calculated SLCBT value.

There is a trade-off between maximum bit rate and resolution with the SLIC in BTM mode. Faster SLIC clock speeds improve resolution, but require higher numbers to be written to the SLCBT registers for a given desired bit rate. It is up to the user to determine what level of resolution is acceptable for the given application.

Desired Bit Rate: 57,600 bps
External Crystal Frequency: 4.9152 MHz

$$\frac{\text{1 Second}}{\text{57,600 Bits}} = \frac{\text{17.36111 ms}}{\text{1 Bit}}$$

$$\frac{\text{1 Second}}{\text{4,915,200 CGMXCLK Periods}} \text{ X } \frac{\text{4 CGMXCLK Period}}{\text{1 SLIC Clock Period}} = \frac{\text{813.802 ns}}{\text{1 SLIC Clock Period}}$$

$$\frac{\text{17.36111 ms}}{\text{1 Bit}} \text{ X } \frac{\text{1 SLIC Clock Period}}{\text{813.802 ns}} = \frac{\text{21.33 SLIC Clock Periods}}{\text{1 Bit}}$$

Therefore, the closest SLCBT value would be 21 SLIC clocks (SLCBT = 0x0015).
Since you can only use even values in SLCBT, the closest acceptable value is 22 (0x0016).

Figure 14-25. SLCBT Value Calculation Example 1

Desired Bit Rate: 57,600 bps
External Crystal Frequency: 9.8304 MHz

$$\frac{\text{1 Second}}{\text{57,600 Bits}} = \frac{\text{17.36111 ms}}{\text{1 Bit}}$$

$$\frac{\text{1 Second}}{\text{9,830,400 CGMXCLK Periods}} \text{ X } \frac{\text{4 CGMXCLK Period}}{\text{1 SLIC Clock Period}} = \frac{\text{406.90 ns}}{\text{1 SLIC Clock Period}}$$

$$\frac{\text{17.36111 ms}}{\text{1 Bit}} \text{ X } \frac{\text{1 SLIC Clock Period}}{\text{406.90 ns}} = \frac{\text{42.67 SLIC Clock Periods}}{\text{1 Bit}}$$

Therefore, the closest SLCBT value would be 42 SLIC clocks (SLCBT = 0x002A).

Figure 14-26. SLCBT Value Calculation Example 2

Desired Bit Rate: 15,625 bps
External Crystal Frequency: 8.000 MHz

$$\frac{\text{1 Second}}{\text{15,625 Bits}} = \frac{\text{64 ms}}{\text{1 Bit}}$$

$$\frac{\text{1 Second}}{\text{8,000,000 CGMXCLK Periods}} \text{ X } \frac{\text{4 CGMXCLK Period}}{\text{1 SLIC Clock Period}} = \frac{\text{500 ns}}{\text{1 SLIC Clock Period}}$$

$$\frac{\text{64 ms}}{\text{1 Bit}} \text{ X } \frac{\text{1 SLIC Clock Period}}{\text{500 ns}} = \frac{\text{128 SLIC Clock Periods}}{\text{1 Bit}}$$

Therefore, the closest SLCBT value would be 128 SLIC clocks (SLCBT = 0x0080).

Figure 14-27. SLCBT Value Calculation Example 3

Desired Bit Rate:	9.615 bps
External Crystal Frequency:	8.000 MHz

$$\frac{\text{1 Second}}{\text{9,615 Bits}} = \frac{\text{104.004 ms}}{\text{1 Bit}}$$

$$\frac{\text{1 Second}}{\text{8,000,000 CGMXCLK Periods}} \times \frac{\text{4 CGMXCLK Period}}{\text{1 SLIC Clock Period}} = \frac{\text{500 ns}}{\text{1 SLIC Clock Period}}$$

$$\frac{\text{104.004 ms}}{\text{1 Bit}} \times \frac{\text{1 SLIC Clock Period}}{\text{500 ns}} = \frac{\text{208.008 SLIC Clock Periods}}{\text{1 Bit}}$$

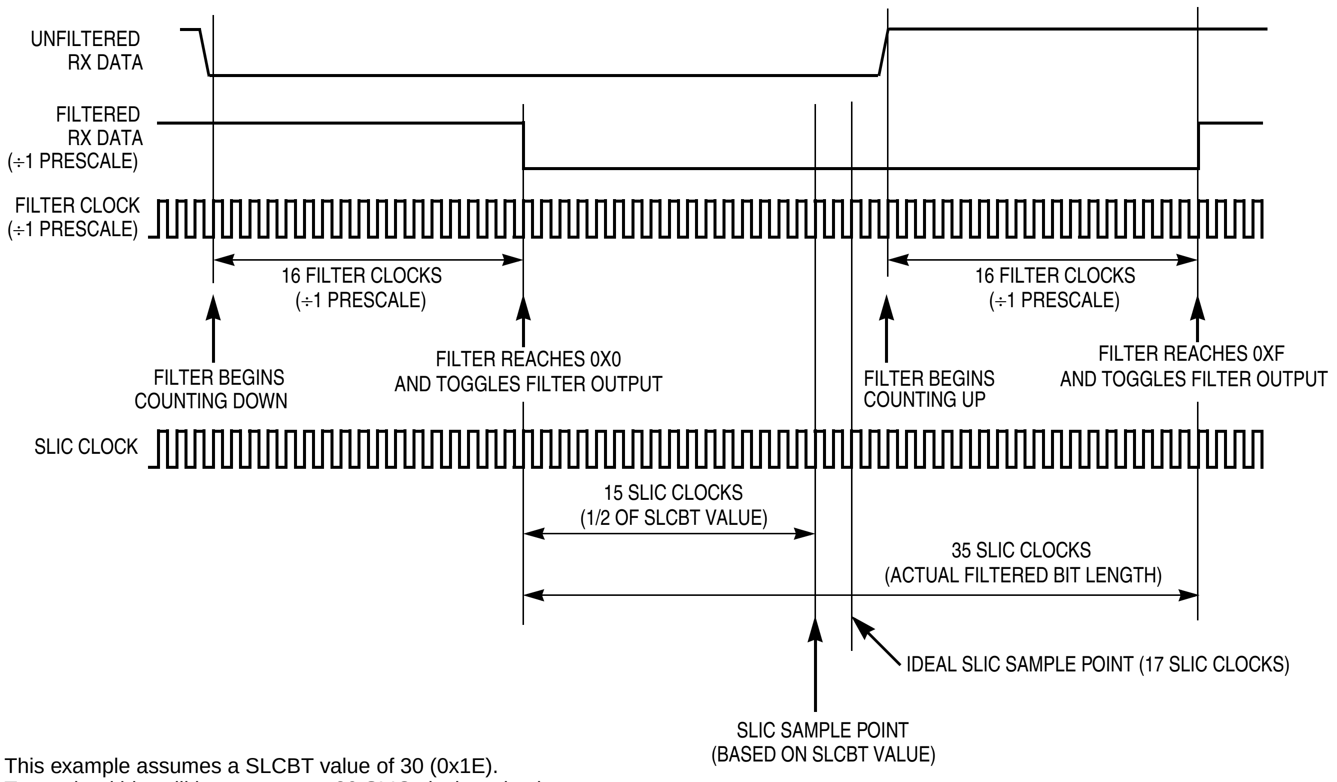
Therefore, the closest SLCBT value would be 42 SLIC clocks (SLCBT = 0x00D0).

Figure 14-28. SLCBT Value Calculation Example 4

This resolution affects the sampling accuracy of the SLIC module on receiving bytes, but only as far as locating the sample point of each bit within a given byte. The best sample point of the bit may be off by as much as one SLIC clock period from the exact center of the bit, if the proper SLCBT value for the desired bit rate is an odd number of SLIC clock periods.

Figure 14-29 shows an example of this error. In this example, the user has additionally chosen an incorrect value of 30 SLIC clocks for the length of one bit time, and a filter prescaler of 1. This makes little difference in the receive sampling of this particular bit, as the sample point is still within the bit and the digital filter will catch any noise pulses shorter than 16 filter clocks long.The ideal value of SLCBT would be 35 SLIC clocks, but the closest available value is 34, placing the sample point at 17 SLIC clocks into the bit.

The error in the bit time value chosen by the user in the above example will grow throughout the byte, as the sample point for the next bit will be only 30 SLIC clock cycles later (1 full bit time at this bit rate setting). The SLIC resynchronizes upon every falling edge received. In a 0x00 data byte, however, there are no falling edges after the beginning of the start bit. This means that the accumulated error of the sampling point over the data byte with these settings could be as high as 30 SLIC clock cycles (10 bits x {2 SLIC clocks due to user error + 1 SLIC clock resolution error}) placing it at the boundary between the last bit and the stop bit. This could result in missampling and missing a framing error on the last bit on high speed communications when the SLCBT count is relatively low. A properly chosen SLCBT value would result in a maximum error of 10 SLIC clock counts over a given byte. This is less than one filter delay time, and will not cause missampling of any of the bits in that byte. At the falling edge of the next start bit, the SLIC will resynchronize and any accumulated sampling error returns to 0. The sampling error becomes even less significant at lower speeds, when higher values of SLCBT are used to define a bit time, as the worst case bit time resolution error is still only one SLIC clock per bit (or maximum of 10 SLIC clocks per byte).


UNFILTERED RX DATA
FILTERED RX DATA (÷1 PRESCALE)
FILTER CLOCK (÷1 PRESCALE)
16 FILTER CLOCKS (÷1 PRESCALE)
16 FILTER CLOCKS (÷1 PRESCALE)
FILTER BEGINS COUNTING DOWN
FILTER REACHES 0X0 AND TOGGLES FILTER OUTPUT
FILTER BEGINS COUNTING UP
FILTER REACHES 0XF AND TOGGLES FILTER OUTPUT
SLIC CLOCK
15 SLIC CLOCKS (1/2 OF SLCBT VALUE)
35 SLIC CLOCKS (ACTUAL FILTERED BIT LENGTH)
IDEAL SLIC SAMPLE POINT (17 SLIC CLOCKS)
SLIC SAMPLE POINT (BASED ON SLCBT VALUE)

This example assumes a SLCBT value of 30 (0x1E).
Transmitted bits will be sent out as 30 SLIC clock cycles long.

The proper closest SLCBT setting would be 34 (0x22), which gives the ideal sample point of 17 SLIC clocks and transmitted bits are 34 SLIC clocks long.

Figure 14-29. BTM Mode Receive Byte Sampling Example

The error also comes into effect with transmitted bit times. Using the previous example with a SLCBT value of 34, transmitted bits will appear as 34 SLIC clock periods long. This is one SLIC clock short of the proper length. Depending on the frequency of the SLIC clock, one period of the SLIC clock might be a large or a small fraction of one ideal bit time. Raising the frequency of the SLIC clock will reduce this error relative to the ideal bit time, improving the resolution of the SLIC clock relative to the bit rate of the bus. In any case, the error is still one SLIC clock cycle. Raising the SLIC clock frequency, however, requires programming a higher value for SLCBT to maintain the same target bit rate.

Smaller values of SLCBT combined with higher values of the SLIC clock frequency (smaller clock period) will give faster bit rates, but the SLIC clock period becomes an increasingly significant portion of one bit time.

Since BTM mode does not perform any synchronization and relies on the accuracy of the data provided by the user software to set its sample point and generate transmitted bits, the constraint on maximum speeds is only limited to the limits imposed by the digital filter delay and the SLIC input clock. Since the digital filter delay cannot be less than 16 SLIC clock cycles, the fastest possible pulse which would pass the filter is 16 clock periods at 8 MHz, or 500,000 bits/second. The values shown in **Table 14-8** are the same values shown in **Table 14-9** and indicate the absolute fastest bit rates which could just pass the minimum digital filter settings (prescaler = divide by 1) under perfect conditions.

Table 14-8. Digital Receive Filter Absolute Cutoff Frequencies

SLIC Clock (MHz)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷4 (Bits / Second)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷3 (Bits / Second)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷2 (Bits / Second)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷1 (Bits / Second)
8	125,000	166,667	250,000	500,000
6.4	100,000	133,333	200,000	400,000
4.8	75,000	100,000	150,000	300,000
4	62,500	83,333	125,000	250,000
3.2	50,000	66,667	100,000	200,000
2.4	37,500	50,000	75,000	150,000
2	31,250	41,667	62,500	125,000

Since perfect conditions are almost impossible to attain, more robust values must be chosen for bit rates. For reliable communication, it is best to ensure that a bit time is no smaller 2x–3x longer than the filter delay on the digital receive filter. This is true in LIN or BTM mode and ensures that valid data bits which have been shortened due to ground shift, asymmetrical rise and fall times, etc., are accepted by the filter without exception. This would translate to 2x to 3x reduction in the maximum speeds shown in **Table 14-8**. Recommended maximum bit rates are shown in **Table 14-9**, and ensure that a single bit time is at least twice the length of one filter delay value. If system noise is not adequately filtered out it might be necessary to change the prescaler of the filter and lower the bit rate of the communication. If valid communications are being absorbed by the filter, corrective action must be taken to ensure that either the bit rate is reduced or whatever physical fault is causing bit times to shorten is corrected (ground offset, asymmetrical rise/fall times, insufficient physical layer supply voltage, etc.).

Table 14-9. Recommended Maximum Bit Rates for BTM Operation Due to Digital Filter

SLIC Clock (MHz)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷4 (Bits / Second)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷3 (Bits / Second)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷2 (Bits / Second)	Maximum BTM Bit Rate with Digital RX Filter Set to ÷1 (Bits / Second)
8	62,500	83,333	125,000	250,000
6.4	50,000	66,667	100,000	200,000
4.8	37,500	50,000	75,000	150,000
4	31,250	41,667	62,500	125,000
3.2	25,000	33,333	50,000	100,000
2.4	18,750	25,000	37,500	125,000
2	15,625	20,833	31,250	62,500

14.19 Oscillator Trimming with SLIC

The SLCACT bit can be used as an indicator of LIN bus activity. SLCACT tells the user that the SLIC is currently processing a message header (therefore synchronizing to the bus) or processing a message frame (including checksum). Therefore, at idle times between message frames or during a message frame which has been marked as a "don’t care" by writing the IMSG bit, it is possible to trim the oscillator circuit of the MCU with no impact to the LIN communications.

It is important to note the exact mechanisms with which the SLIC sets and clears the SLCACT bit. Any falling edge which successfully passes through the digital receive filter will cause the SLCACT bit to become set. This might even include noise pulses, if they are of sufficient length to pass through the digital RX filter. Although in these cases the SLCACT bit is becoming set on a noise spike, it is very probable that noise of this nature will cause other system issues as well such as corruption of the message frame. The software can then further qualify if it is appropriate to trim the oscillator.

The SLCACT bit will only be cleared by the SLIC upon successful completion of a normal LIN message frame (see **14.6.3 SLIC Status Register** description for more detail). This means that in some cases, if a message frame terminates with an error condition or some source other than those cited in the SLCACT bit description, the SLCACT might remain set during an otherwise idle bus time. The SLCACT will then clear upon the successful completion of the next LIN message frame.

These mechanisms might result in SLCACT being set when it is safe (from the SLIC module perspective) to trim the oscillator. However, the SLCACT bit will only be clear when the SLIC considers it safe to trim the oscillator.

In a particular system, it might also be possible to improve the opportunities for trimming by utilizing system knowledge and use of the IMSG bit. If a message ID is known to be considered a "don’t care" by this particular node, it should be safe to trim the oscillator during that message frame (provided that it is safe for the application software as well). After the software has done an identifier lookup and determined that the ID corresponds to a "don’t care" message, the software might choose to set the IMSG bit. From that time, the application software should have at least one byte time of message traffic in which to trim the oscillator before that ignored message frame expires, regardless of the state of the SLCACT bit. If the length of that ignored message frame is known, that knowledge might also be utilized to extend the time of this oscillator trimming opportunity.

Now that the mechanisms for recognizing when the SLIC module indicates safe oscillator trimming opportunities are understood, it is important to understand how to derive the information needed to perform the trimming.

The value in the SLCBT register will indicate how many SLIC clock cycles comprise one bit time and for any given LIN bus speed, this will be a fixed value if the oscillator is running at its ideal frequency. It is possible to use this ideal value combined with the measured value in the SLCBT register to determine how to adjust the oscillator of the microcontroller.

The actual oscillator trimming algorithm is very specific to each particular implementation, and applications might or might not require the oscillator even to be trimmed. The SLIC can maintain communications even with input oscillator variation of ±50% (with 4 MHz nominal, that means that any input clock into the SLIC from 2 MHz to 6 MHz will still guarantee communications). Since most Motorola internal oscillators are at least within ±25% of their nominal value, even when untrimmed, this means that trimming of the oscillator is not even required for LIN communications. If the application can tolerate the range of frequencies which might appear within this manufacturing range, then it is not necessary ever to trim the oscillator. This can be a tremendous advantage to the customer, enabling migration to very low-cost ROM devices which have no non-volatile memory in which to store the trim value.

NOTE: *Even though most internal oscillators are within ±25% before trimming, they are stable at some frequency in that range, within at least ±5% over the entire operating voltage and temperature range. The trimming operation simply eliminates the offset due to factory manufacturing variations to re-center the base oscillator frequency to the nominal value. Please refer to the electrical specifications for the oscillator for more specific information, as exact specifications might differ from module to module.*

14.20 Digital Receive Filter

The receiver section of the SLIC module includes a digital low-pass filter to remove narrow noise pulses from the incoming message. An outline of the digital filter is shown in **Figure 14-30**.

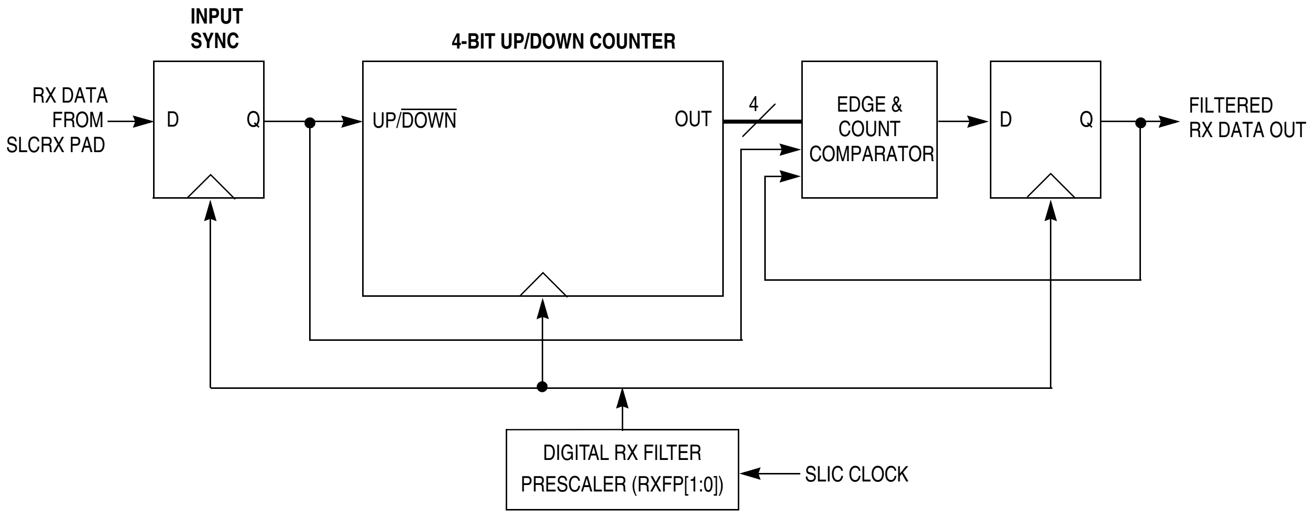


Figure 14-30. SLIC Module Rx Digital Filter Block Diagram

14.20.1 Operation

The clock for the digital filter is provided by the SLIC Interface clock. At each positive edge of the clock signal, the current state of the receiver input signal from the SLCRX pad is sampled. The SLCRX signal state is used to determine whether the counter should increment or decrement at the next positive edge of the clock signal.

The counter will increment if the input data sample is high but decrement if the input sample is low. The counter will thus progress up towards ‘15’ if, on average, the SLCRX signal remains high or progress down towards ‘0’ if, on average, the SLCRX signal remains low.

When the counter eventually reaches the value ‘15’, the digital filter decides that the condition of the SLCRX signal is at a stable logic level 1 and the data latch is set, causing the filtered Rx data signal to become a logic level 1. Furthermore, the counter is prevented from overflowing and can only be decremented from this state.

Alternatively, should the counter eventually reach the value ‘0’, the digital filter decides that the condition of the SLCRX signal is at a stable logic level 0 and the data latch is reset, causing the filtered Rx data signal to become a logic level 0. Furthermore, the counter is prevented from underflowing and can only be incremented from this state.

The data latch will retain its value until the counter next reaches the opposite end point, signifying a definite transition of the SLCRX signal.

14.20.2 Performance

The performance of the digital filter is best described in the time domain rather than the frequency domain.

If the signal on the SLCRX signal transitions, then there will be a delay before that transition appears at the filtered Rx data output signal. This delay will be between 15 and 16 clock periods, depending on where the transition occurs with respect to the sampling points. This 'filter delay' is not an issue for SLIC operation, as there is no need for message arbitration.

The effect of random noise on the SLCRX signal depends on the characteristics of the noise itself. Narrow noise pulses on the SLCRX signal will be completely ignored if they are shorter than the filter delay. This provides a degree of low-pass filtering. **Figure 14-30** shows the configuration of the digital receive filter and the consequential effect on the filter delay. This filter delay value indicates that for a particular setup, only pulses of which are greater than the filter delay will pass the filter.

For example, if the frequency of the SLIC clock (f_{SLIC}) is 3.2 MHz, then the period (t_{SLIC}) is of the SLIC clock is 313 ns. With the default receive filter prescaler setting of division by 3, the resulting maximum filter delay in the absence of noise will be 15.00 μs. By simply changing the prescaler of the receive filter, the user can then select alternatively 5 μs, 10 μs, or 20 μs as a minimum filter delay according to the systems requirements.

If noise occurs during a symbol transition, the detection of that transition may be delayed by an amount equal to the length of the noise burst. This is just a reflection of the uncertainty of where the transition is truly occurring within the noise.

NOTE: *The user must always account for the worst case bit timing of their LIN bus when configuring the digital receive filter, especially if running at faster speeds. Ground offset and other physical layer conditions can cause shortening of bits as seen at the digital receive pin, for example. If these shortened bit lengths are less than the filter delay, the bits will be interpreted by the filter as noise and will be blocked, even though the nominal bit timing might be greater than the filter delay.*

Section 15. Timer Interface Module (TIM)

15.1 Introduction

This section describes the timer interface module (TIM). The TIM is a two-channel timer that provides a timing reference with input capture, output compare, and pulse-width-modulation functions. **Figure 15-2** is a block diagram of the TIM.

15.2 Features

Features of the TIM include the following:

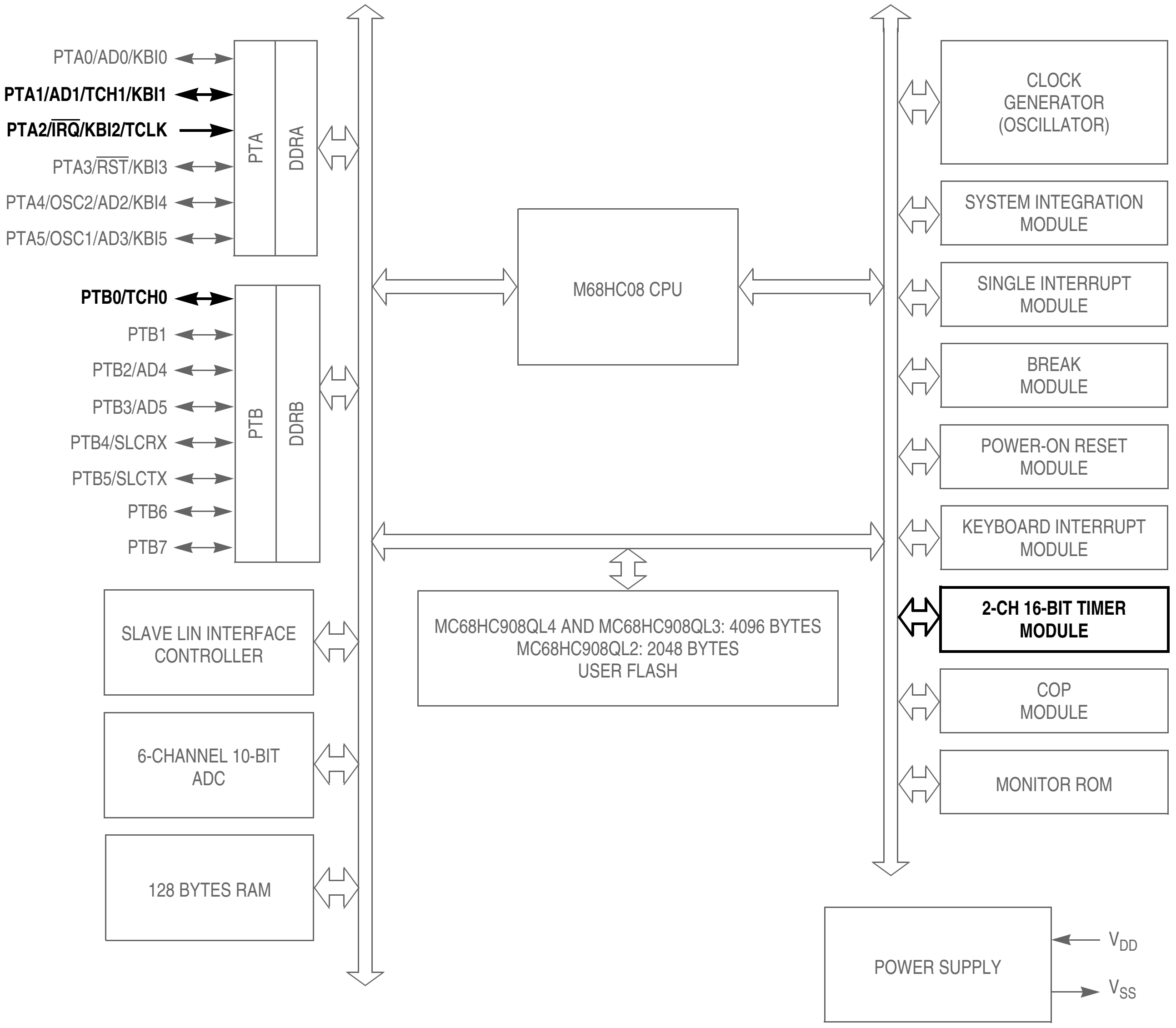
- Two input capture/output compare channels
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
- Buffered and unbuffered pulse width modulation (PWM) signal generation
- Programmable TIM clock input
  - 7-frequency internal bus clock prescaler selection
  - External TIM clock input
- Free-running or modulo up-count operation
- Toggle any channel pin on overflow
- TIM counter stop and reset bits

15.3 Pin Name Conventions

The TIM shares two input/output (I/O) pins with two port A I/O pins. The full names of the TIM I/O pins are listed in **Table 15-1**. The generic pin name appear in the text that follows.

Table 15-1. Pin Name Conventions

TIM Generic Pin Names:	TCH0	TCH1	TCLK
Full TIM Pin Names:	PTB0/TCH0	PTA1/TCH1	PTA2/TCLK



$\overline{\text{RST}}$, $\overline{\text{IRQ}}$: Pins have internal (about 30 kΩ) pull up
PTA0, PTA1, PTA3–PTA5: High current sink and source capability
PTA0–PTA5: Pins have programmable keyboard interrupt and pull up
ADC pins only available on MC68HC908QL4 and MC68HC908QL2

Figure 15-1. Block Diagram Highlighting TIM Block and Pins

15.4 Functional Description

Figure 15-2 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH:TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

The two TIM channels are programmable independently as input capture or output compare channels.

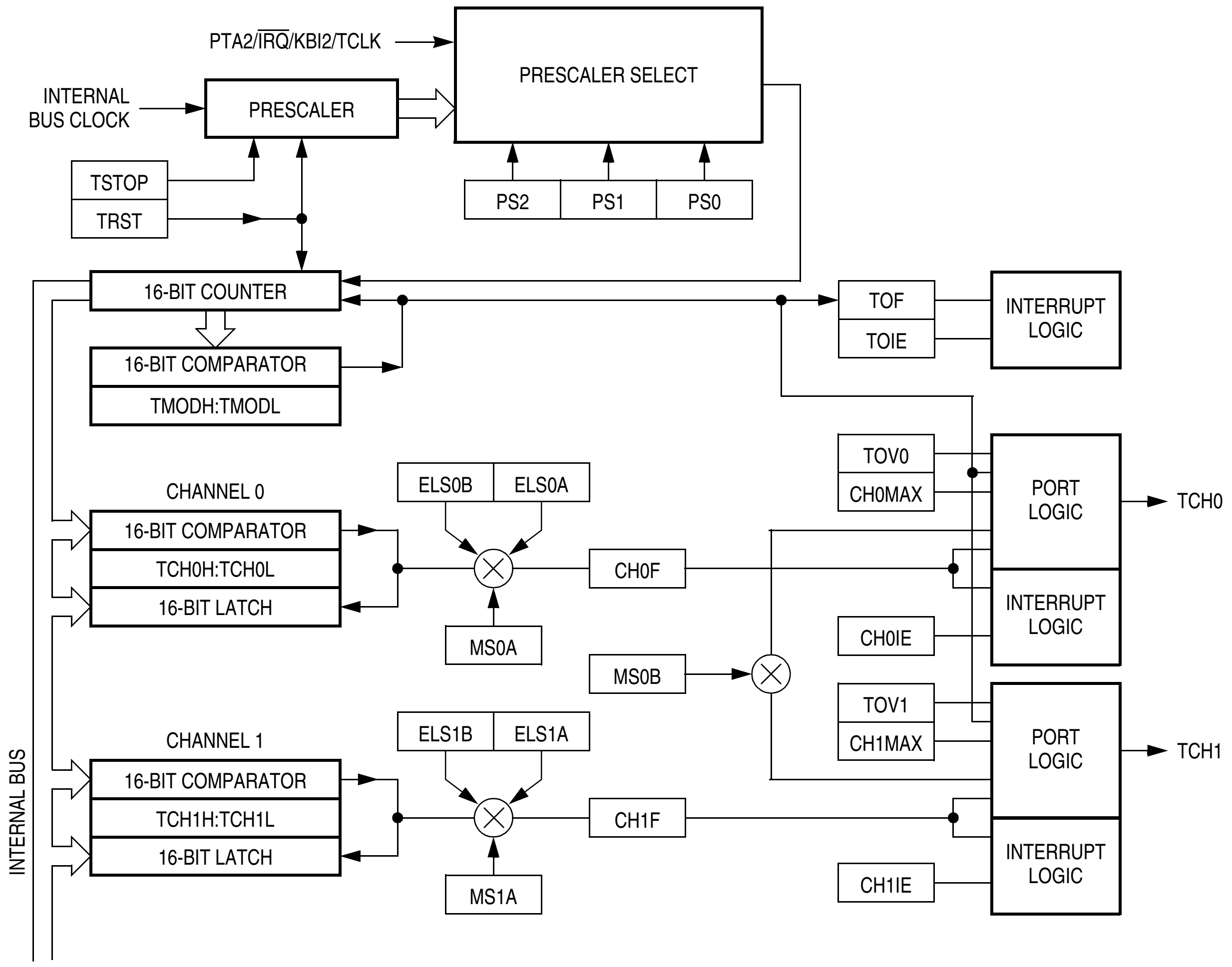


Figure 15-2. TIM Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0020	TIM Status and Control Register (TSC) See page 197.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST	▨			
		Reset:	0	0	1	0	0	0	0	0
$0021	TIM Counter Register High (TCNTH) See page 199.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$0022	TIM Counter Register Low (TCNTL) See page 199.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$0023	TIM Counter Modulo Register High (TMODH) See page 199.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0024	TIM Counter Modulo Register Low (TMODL) See page 199.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0025	TIM Channel 0 Status and Control Register (TSC0) See page 200.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	TIM Channel 0 Register High (TCH0H) See page 203.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$0027	TIM Channel 0 Register Low (TCH0L) See page 203.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$0028	TIM Channel 1 Status and Control Register (TSC1) See page 200.	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0		▨					
		Reset:	0	0	0	0	0	0	0	0
$0029	TIM Channel 1 Register High (TCH1H) See page 203.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$002A	TIM Channel 1 Register Low (TCH1L) See page 203.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							

▨ = Unimplemented

Figure 15-3. TIM I/O Register Summary

15.4.1 TIM Counter Prescaler

The TIM clock source is one of the seven prescaler outputs or the TIM clock pin, TCLK. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM status and control register (TSC) select the TIM clock source.

15.4.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH:TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM central processor unit (CPU) interrupt requests.

15.4.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests.

15.4.3.1 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in **15.4.3 Output Compare**. The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM overflow interrupt routine to write a new, smaller output compare value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the output compare value on channel x:

- When changing to a smaller value, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current output compare pulse. The interrupt routine has until the end of the counter overflow period to write the new value.
- When changing to a larger output compare value, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current counter overflow

period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same counter overflow period.

15.4.3.2 Buffered Output Compare

Channels 0 and 1 can be linked to form a buffered output compare channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The output compare value in the TIM channel 0 registers initially controls the output on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the output after the TIM overflows. At each subsequent overflow, the TIM channel registers (0 or 1) that control the output are the ones written to last. TSC0 controls and monitors the buffered output compare function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

NOTE: *In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.*

15.4.4 Pulse Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM can generate a PWM signal. The value in the TIM counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM counter modulo registers. The time between overflows is the period of the PWM signal.

As **Figure 15-4** shows, the output compare value in the TIM channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM to clear the channel pin on output compare if the state of the PWM pulse is logic 1. Program the TIM to set the pin if the state of the PWM pulse is logic 0.

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing $00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is 000. See **15.9.1 TIM Status and Control Register**.

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing $0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50%.

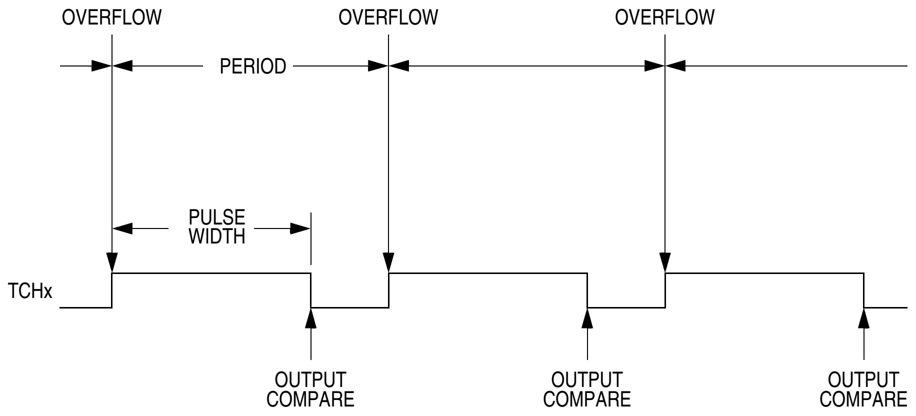


Figure 15-4. PWM Period and Pulse Width

15.4.4.1 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in **15.4.4 Pulse Width Modulation (PWM)**. The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIM overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the PWM pulse width on channel x:

- When changing to a shorter pulse width, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current pulse. The interrupt routine has until the end of the PWM period to write the new value.
- When changing to a longer pulse width, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current PWM period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same PWM period.

NOTE: *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare also can cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

15.4.4.2 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The TIM channel 0 registers initially control the pulse width on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIM channel registers (0 or 1) that control the pulse width are the ones written to last. TSC0 controls and monitors the buffered PWM function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

NOTE: *In buffered PWM signal generation, do not write new pulse width values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered PWM signals.*

15.4.4.3 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use the following initialization procedure:

1. In the TIM status and control register (TSC):
   a. Stop the TIM counter by setting the TIM stop bit, TSTOP.
   b. Reset the TIM counter and prescaler by setting the TIM reset bit, TRST.
2. In the TIM counter modulo registers (TMODH:TMODL), write the value for the required PWM period.
3. In the TIM channel x registers (TCHxH:TCHxL), write the value for the required pulse width.
4. In TIM channel x status and control register (TSCx):
   a. Write 0:1 (for unbuffered output compare or PWM signals) or 1:0 (for buffered output compare or PWM signals) to the mode select bits, MSxB:MSxA. See **Table 15-3**.
   b. Write 1 to the toggle-on-overflow bit, TOVx.
   c. Write 1:0 (to clear output on compare) or 1:1 (to set output on compare) to the edge/level select bits, ELSxB:ELSxA. The output action on compare must force the output to the complement of the pulse width level. See **Table 15-3**.

NOTE: *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0% duty cycle generation and removes the ability of the channel to self-correct in the event of software error* *or noise. Toggling on output compare can also cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

5. In the TIM status control register (TSC), clear the TIM stop bit, TSTOP.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM channel 0 registers (TCH0H:TCH0L) initially control the buffered PWM output. TIM status control register 0 (TSCR0) controls and monitors the PWM signal from the linked channels. MS0B takes priority over MS0A.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0% duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and setting the TOVx bit generates a 100% duty cycle output. See **15.9.4 TIM Channel Status and Control Registers**.

15.5 Interrupts

The following TIM sources can generate interrupt requests:

- TIM overflow flag (TOF) — The TOF bit is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow CPU interrupt requests. TOF and TOIE are in the TIM status and control register.
- TIM channel flags (CH1F:CH0F) — The CHxF bit is set when an input capture or output compare occurs on channel x. Channel x TIM CPU interrupt requests are controlled by the channel x interrupt enable bit, CHxIE. Channel x TIM CPU interrupt requests are enabled when CHxIE =1. CHxF and CHxIE are in the TIM channel x status and control register.

15.6 Wait Mode

The WAIT instruction puts the MCU in low power-consumption standby mode.

The TIM remains active after the execution of a WAIT instruction. In wait mode the TIM registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

15.7 TIM During Break Interrupts

A break interrupt stops the TIM counter.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See **13.8.2 Break Flag Control Register**.

To allow software to clear status bits during a break interrupt, write a 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a two-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at 0. After the break, doing the second step clears the status bit.

15.8 Input/Output Signals

Port A shares three of its pins with the TIM. Two TIM channel I/O pins are PTA0/TCH0 and PTA1/TCH1 and an alternate clock source is PTA2/TCLK.

15.8.1 TIM Clock Pin (PTA2/TCLK)

PTA2/TCLK is an external clock input that can be the clock source for the TIM counter instead of the prescaled internal bus clock. Select the PTA2/TCLK input by writing logic 1s to the three prescaler select bits, PS[2–0]. (See **15.9.1 TIM Status and Control Register**.) When the PTA2/TCLK pin is the TIM clock input, it is an input regardless of port pin initialization.

15.8.2 TIM Channel I/O Pins (PTA0/TCH0 and PTA1/TCH1)

Each channel I/O pin is programmable independently as an input capture pin or an output compare pin. PTA0/TCH0 can be configured as a buffered output compare or buffered PWM pin.

15.9 Input/Output Registers

The following I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM control registers (TCNTH:TCNTL)
- TIM counter modulo registers (TMODH:TMODL)
- TIM channel status and control registers (TSC0 and TSC1)
- TIM channel registers (TCH0H:TCH0L and TCH1H:TCH1L)

15.9.1 TIM Status and Control Register

The TIM status and control register (TSC) does the following:

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST	▨			
Reset:	0	0	1	0	0	0	0	0

▨ = Unimplemented

Figure 15-5. TIM Status and Control Register (TSC)

TOF — TIM Overflow Flag Bit

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

1 = TIM counter has reached modulo value
0 = TIM counter has not reached modulo value

TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled
0 = TIM overflow interrupts disabled

TSTOP — TIM Stop Bit

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped
0 = TIM counter active

NOTE: *Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.*

TRST — TIM Reset Bit

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from $0000. TRST is cleared automatically after the TIM counter is reset and always reads as logic 0. Reset clears the TRST bit.

1 = Prescaler and TIM counter cleared
0 = No effect

NOTE: *Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of $0000.*

PS[2:0] — Prescaler Select Bits

These read/write bits select either the PTA2/TCLK pin or one of the seven prescaler outputs as the input to the TIM counter as **Table 15-2** shows. Reset clears the PS[2:0] bits.

Table 15-2. Prescaler Selection

PS2	PS1	PS0	TIM Clock Source
0	0	0	Internal bus clock ÷ 1
0	0	1	Internal bus clock ÷ 2
0	1	0	Internal bus clock ÷ 4
0	1	1	Internal bus clock ÷ 8
1	0	0	Internal bus clock ÷ 16
1	0	1	Internal bus clock ÷ 32
1	1	0	Internal bus clock ÷ 64
1	1	1	PTA2/TCLK

15.9.2 TIM Counter Registers

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers.

NOTE: *If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.*

Address: $0021 TCNTH

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0

Address: $0022 TCNTL

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 15-6. TIM Counter Registers (TCNTH:TCNTL)

15.9.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from $0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

Address: $0023 TMODH

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Address: $0024 TMODL

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 15-7. TIM Counter Modulo Registers (TMODH:TMODL)

NOTE: *Reset the TIM counter before writing to the TIM counter modulo registers.*

15.9.4 TIM Channel Status and Control Registers

Each of the TIM channel status and control registers does the following:

- Flags input captures and output compares
- Enables input capture and output compare interrupts
- Selects input capture, output compare, or PWM operation
- Selects high, low, or toggling output on output compare
- Selects rising edge, falling edge, or any edge as the active input capture trigger
- Selects output toggling on TIM overflow
- Selects 0% and 100% PWM duty cycle
- Selects buffered or unbuffered output compare/PWM operation

Address: $0025 TSC0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Address: $0028 TSC1

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
Write:	0		▨					
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 15-8. TIM Channel Status and Control Registers (TSC0:TSC1)

CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM counter registers matches the value in the TIM channel x registers.

Clear CHxF by reading the TIM channel x status and control register with CHxF set and then writing a 0 to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing 0 to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a 1 to CHxF has no effect.

1 = Input capture or output compare on channel x
0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM CPU interrupt service requests on channel x. Reset clears the CHxIE bit.

1 = Channel x CPU interrupt requests enabled
0 = Channel x CPU interrupt requests disabled

MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MSxB exists only in the TIM channel 0 status and control register.

Setting MS0B disables the channel 1 status and control register and reverts TCH1 to general-purpose I/O.
Reset clears the MSxB bit.

1 = Buffered output compare/PWM operation enabled
0 = Buffered output compare/PWM operation disabled

MSxA — Mode Select Bit A

When ELSxB:A ≠ 00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation.
See **Table 15-3**.

1 = Unbuffered output compare/PWM operation
0 = Input capture operation

When ELSxB:A = 00, this read/write bit selects the initial output level of the TCHx pin (see **Table 15-3**). Reset clears the MSxA bit.

1 = Initial output level low
0 = Initial output level high

NOTE: *Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).*

Table 15-3. Mode, Edge, and Level Selection

MSxB	MSxA	ELSxB	ELSxA	Mode	Configuration
X	0	0	0	Output preset	Pin under port control; initial output level high
X	1	0	0		Pin under port control; initial output level low
0	0	0	1	Input capture	Capture on rising edge only
0	0	1	0		Capture on falling edge only
0	0	1	1		Capture on rising or falling edge
0	1	0	0	Output compare or PWM	Software compare only
0	1	0	1		Toggle output on compare
0	1	1	0		Clear output on compare
0	1	1	1		Set output on compare
1	X	0	1	Buffered output compare or buffered PWM	Toggle output on compare
1	X	1	0		Clear output on compare
1	X	1	1		Set output on compare

ELSxB and ELSxA — Edge/Level Select Bits

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to an I/O port, and pin TCHx is available as a general-purpose I/O pin. **Table 15-3** shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

NOTE: *After initially enabling a TIM channel register for input capture operation and selecting the edge sensitivity, clear CHxF to ignore any erroneous edge detection flags.*

TOVx — Toggle-On-Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the TIM counter overflows. When channel x is an input capture channel, TOVx has no effect. Reset clears the TOVx bit.

1 = Channel x pin toggles on TIM counter overflow.
0 = Channel x pin does not toggle on TIM counter overflow.

NOTE: *When TOVx is set, a TIM counter overflow takes precedence over a channel x output compare if both occur at the same time.*

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at 1, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As **Figure 15-9** shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at the 100% duty cycle level until the cycle after CHxMAX is cleared.

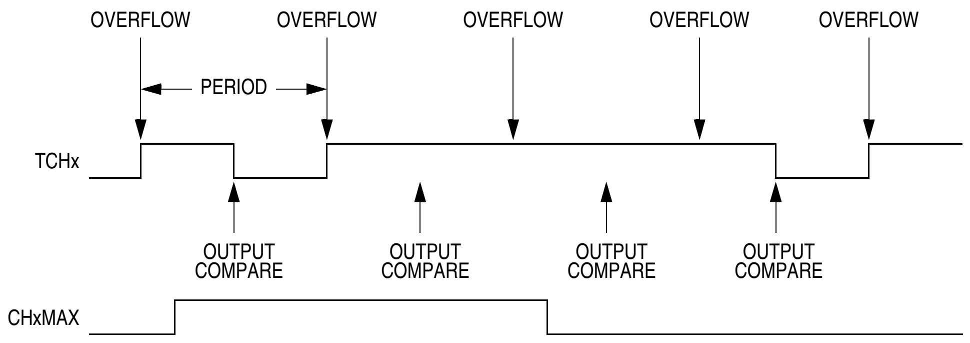


Figure 15-9. CHxMAX Latency

15.9.5 TIM Channel Registers

These read/write registers contain the captured TIM counter value of the input capture function or the output compare value of the output compare function. The state of the TIM channel registers after reset is unknown.

In input capture mode (MSxB:MSxA = 0:0), reading the high byte of the TIM channel x registers (TCHxH) inhibits input captures until the low byte (TCHxL) is read.

In output compare mode (MSxB:MSxA ≠ 0:0), writing to the high byte of the TIM channel x registers (TCHxH) inhibits output compares until the low byte (TCHxL) is written.

Address: $0026 TCH0H

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	Indeterminate after reset							

Address: $0027 TCH0L

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Indeterminate after reset							

Address: $0029 TCH1H

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	Indeterminate after reset							

Address: $02A TCH1L

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Indeterminate after reset							

Figure 15-10. TIM Channel Registers (TCH0H/L:TCH1H/L)

Section 16. Development Support

16.1 Introduction

This section describes the break module, the monitor read-only memory (MON), and the monitor mode entry methods.

16.2 Break Module (BRK)

The break module can generate a break interrupt that stops normal program flow at a defined address to enter a background program.

Features include:

- Accessible input/output (I/O) registers during the break Interrupt
- Central processor unit (CPU) generated break interrupts
- Software-generated break interrupts
- Computer operating properly (COP) disabling during break interrupts

16.2.1 Functional Description

When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal ($\overline{\text{BKPT}}$) to the system integration module (SIM). The SIM then causes the CPU to load the instruction register with a software interrupt instruction (SWI). The program counter vectors to \$FFFC and \$FFFD (\$FEFC and \$FEFD in monitor mode).

The following events can cause a break interrupt to occur:

- A CPU generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a 1 to the BRKA bit in the break status and control register.

When a CPU generated address matches the contents of the break address registers, the break interrupt is generated. A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the microcontroller unit (MCU) to normal operation.

Figure 16-1 shows the structure of the break module.

Figure 16-2 provides a summary of the I/O registers.

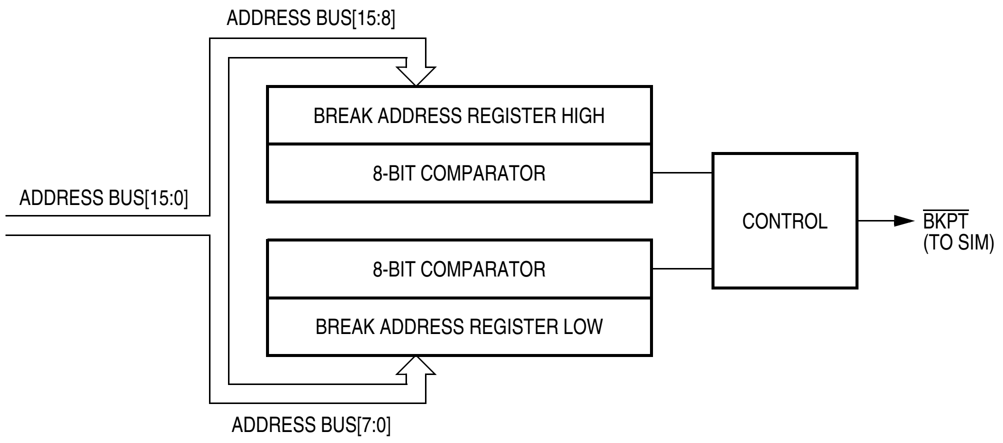


Figure 16-1. Break Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE00	Break Status Register (BSR) See page 210.	Read:	R	R	R	R	R	R	SBSW	R
		Write:	R	R	R	R	R	R	Note[1]	R
		Reset:							0	
$FE02	Break Auxiliary Register (BRKAR) See page 209.	Read:	0	0	0	0	0	0	0	BDCOP
		Write:	▨	▨	▨	▨	▨	▨	▨	BDCOP
		Reset:	0	0	0	0	0	0	0	0
$FE03	Break Flag Control Register (BFCR) See page 210.	Read:	BCFE	R	R	R	R	R	R	R
		Write:	BCFE	R	R	R	R	R	R	R
		Reset:	0							
$FE09	Break Address High Register (BRKH) See page 209.	Read:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Write:	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
		Reset:	0	0	0	0	0	0	0	0
$FE0A	Break Address Low Register (BRKL) See page 209.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$FE0B	Break Status and Control Register (BRKSCR) See page 208.	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:	BRKE	BRKA	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0

1. Writing a 0 clears SBSW.

▨ = Unimplemented R = Reserved

Figure 16-2. Break I/O Register Summary

When the internal address bus matches the value written in the break address registers or when software writes a 1 to the BRKA bit in the break status and control register, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC and $FFFD ($FEFC and $FEFD in monitor mode)

The break interrupt timing is:

- When a break address is placed at the address of the instruction opcode, the instruction is not executed until after completion of the break interrupt routine.
- When a break address is placed at an address of an instruction operand, the instruction is executed before the break interrupt.
- When software writes a 1 to the BRKA bit, the break interrupt occurs just before the next instruction is executed.

By updating a break address and clearing the BRKA bit in a break interrupt routine, a break interrupt can be generated continuously.

CAUTION: *A break address should be placed at the address of the instruction opcode. When software does not change the break address and clears the BRKA bit in the first break interrupt routine, the next break interrupt will not be generated after exiting the interrupt routine even when the internal address bus matches the value written in the break address registers.*

16.2.1.1 Flag Protection During Break Interrupts

The system integration module (SIM) controls whether or not module status bits can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See **13.8.2 Break Flag Control Register** and the **Break Interrupts** subsection for each module.

16.2.1.2 TIM During Break Interrupts

A break interrupt stops the timer counter.

16.2.1.3 COP During Break Interrupts

The COP is disabled during a break interrupt with monitor mode when BDCOP bit is set in break auxiliary register (BRKAR).

16.2.2 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- Break status register (BSR)
- Break flag control register (BFCR)

16.2.2.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.

Address: $FE0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BRKE	BRKA	0	0	0	0	0	0
Write:			▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 16-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit
This read/write bit enables breaks on break address register matches. Clear BRKE by writing a 0 to bit 7. Reset clears the BRKE bit.
1 = Breaks enabled on 16-bit address match
0 = Breaks disabled

BRKA — Break Active Bit
This read/write status and control bit is set when a break address match occurs. Writing a 1 to BRKA generates a break interrupt. Clear BRKA by writing a 0 to it before exiting the break routine. Reset clears the BRKA bit.
1 = Break address match
0 = No break address match

16.2.2.2 Break Address Registers

The break address registers (BRKH and BRKL) contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

Address: $FE09

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	0	0	0	0	0	0	0	0

Figure 16-4. Break Address Register High (BRKH)

Address: $FE0A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 16-5. Break Address Register Low (BRKL)

16.2.2.3 Break Auxiliary Register

The break auxiliary register (BRKAR) contains a bit that enables software to disable the COP while the MCU is in a state of break interrupt with monitor mode.

Address: $FE02

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	BDCOP
Write:	▨	▨	▨	▨	▨	▨	▨	
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 16-6. Break Auxiliary Register (BRKAR)

BDCOP — Break Disable COP Bit
This read/write bit disables the COP during a break interrupt. Reset clears the BDCOP bit.
1 = COP disabled during break interrupt
0 = COP enabled during break interrupt

16.2.2.4 Break Status Register

The break status register (BSR) contains a flag to indicate that a break caused an exit from wait mode. This register is only used in emulation mode.

Address: $FE00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							Note(1)	
Reset:							0	

R = Reserved

1. Writing a 0 clears SBSW.

Figure 16-7. Break Status Register (BSR)

SBSW — SIM Break Stop/Wait

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it.

1 = Wait mode was exited by break interrupt

0 = Wait mode was not exited by break interrupt

16.2.2.5 Break Flag Control Register

The break control register (BFCR) contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: $FE03

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BCFE	R	R	R	R	R	R	R
Reset:	0							

R = Reserved

Figure 16-8. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break

16.2.3 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power- consumption standby modes. If enabled, the break module will remain enabled in wait and stop modes. However, since the internal address bus does not increment in these modes, a break interrupt will never be triggered.

16.3 Monitor Module (MON)

This subsection describes the monitor module (MON) and the monitor mode entry methods. The monitor allows debugging and programming of the microcontroller unit (MCU) through a single-wire interface with a host computer. Monitor mode entry can be achieved without use of the higher test voltage, V_{TST}, as long as vector addresses \$FFFE and \$FFFF are blank, thus reducing the hardware requirements for in-circuit programming.

Features include:

- Normal user-mode pin functionality on most pins
- One pin dedicated to serial communication between MCU and host computer
- Standard non-return-to-zero (NRZ) communication with host computer
- Execution of code in random-access memory (RAM) or FLASH
- FLASH memory security feature(1)
- FLASH memory programming interface
- Use of external 9.8304 MHz crystal or clock to generate internal frequency of 2.4576 MHz
- Simple internal oscillator mode of operation (no external clock or high voltage)
- Monitor mode entry without high voltage, V_{TST}, if reset vector is blank (\$FFFE and \$FFFF contain \$FF)
- Standard monitor mode entry if high voltage is applied to $\overline{\text{IRQ}}$

16.3.1 Functional Description

Figure 16-9 shows a simplified diagram of monitor mode entry.

The monitor module receives and executes commands from a host computer. **Figure 16-10**, **Figure 16-11**, and **Figure 16-12** show example circuits used to enter monitor mode and communicate with a host computer via a standard RS-232 interface.

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

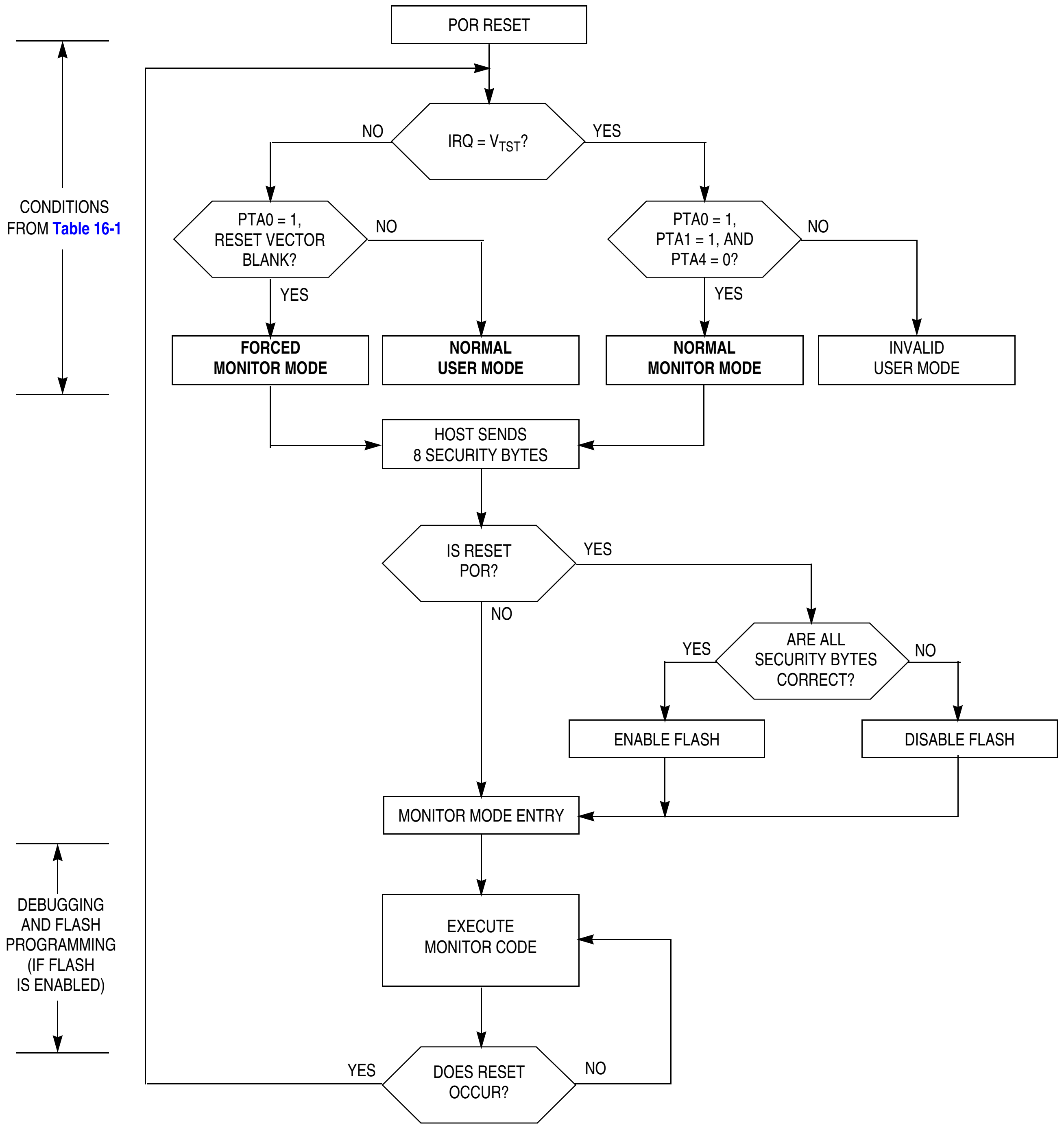


Figure 16-9. Simplified Monitor Mode Entry Flowchart

Simple monitor commands can access any memory address. In monitor mode, the MCU can execute code downloaded into RAM by a host computer while most MCU pins retain normal operating mode functions. All communication between the host computer and the MCU is through the PTA0 pin. A level-shifting and multiplexing interface is required between PTA0 and the host computer. PTA0 is used in a wired-OR configuration and requires a pullup resistor.

The monitor code has been updated from previous versions of the monitor code to allow enabling the internal oscillator to generate the internal clock. This addition, which is enabled when $\overline{IRQ}$ is held low out of reset, is intended to support serial communication/programming at 9600 baud in monitor mode by using the internal oscillator, and the internal oscillator user trim value OSCTRIM (FLASH location $FFC0, if programmed) to generate the desired internal frequency (3.2 MHz). Since this feature is enabled only when $\overline{IRQ}$ is held low out of reset, it cannot be used when the reset vector is programmed (i.e., the value is not $FFFF) because entry into monitor mode in this case requires V_{TST} on $\overline{IRQ}$. The $\overline{IRQ}$ pin must remain low during this monitor session in order to maintain communication.

Table 16-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a power-on reset (POR) and will allow communication at 9600 baud provided one of the following sets of conditions is met:

- If $FFFE and $FFFF do not contain $FF (programmed state):
  - The external clock is 9.8304 MHz
  - $\overline{IRQ} = V_{TST}$
- If $FFFE and $FFFF contain $FF (erased state):
  - The external clock is 9.8304 MHz
  - $\overline{IRQ} = V_{DD}$ (this can be implemented through the internal $\overline{IRQ}$ pullup)
- If $FFFE and $FFFF contain $FF (erased state):
  - $\overline{IRQ} = V_{SS}$ (internal oscillator is selected, no external clock required)

The rising edge of the internal $\overline{RST}$ signal latches the monitor mode. Once monitor mode is latched, the values on PTA1 and PTA4 pins can be changed.

Once out of reset, the MCU waits for the host to send eight security bytes (see **16.3.2 Security**). After the security bytes, the MCU sends a break signal (10 consecutive logic 0s) to the host, indicating that it is ready to receive a command.

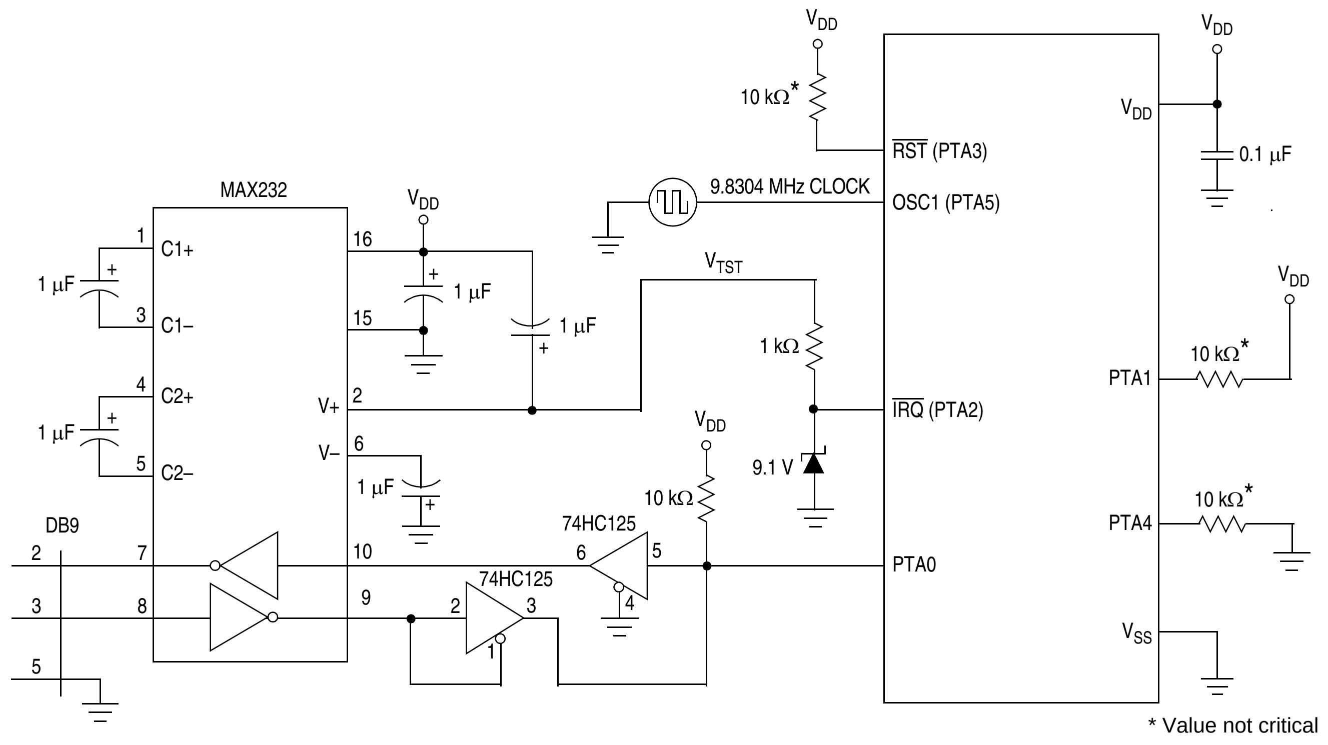


Figure 16-10. Monitor Mode Circuit (External Clock, with High Voltage)

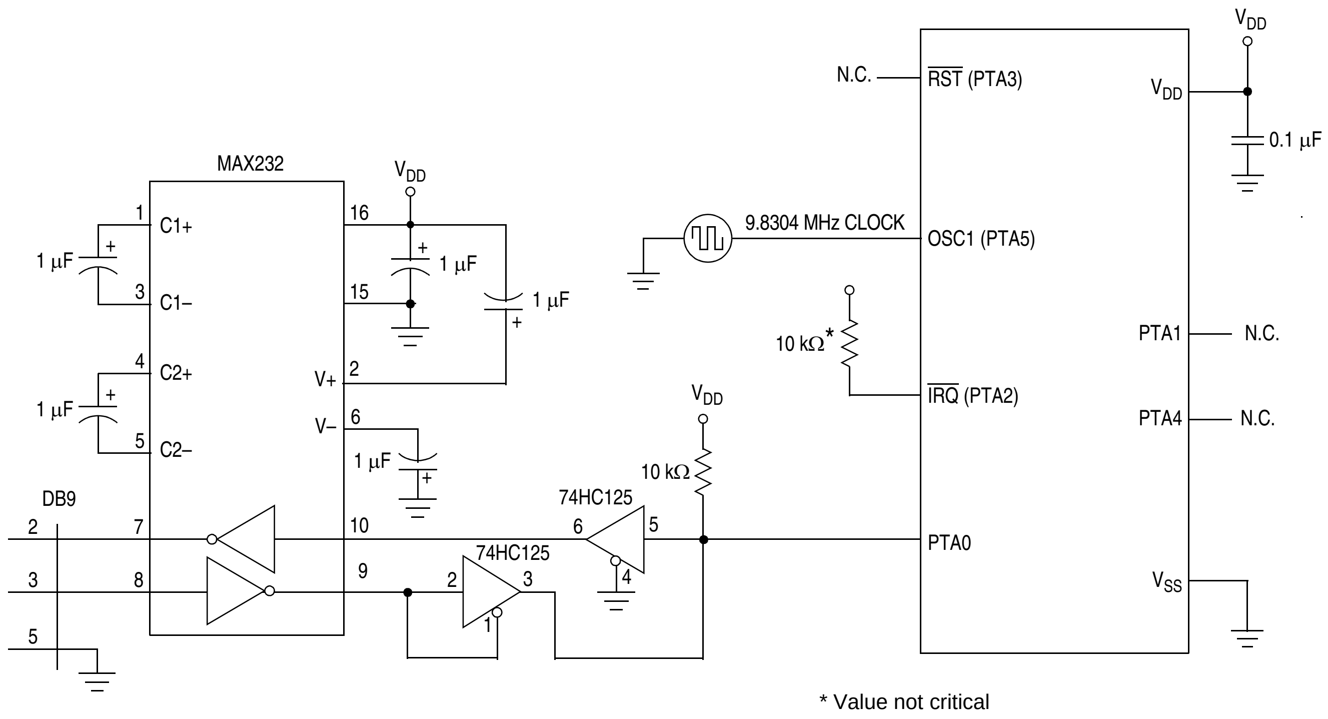


Figure 16-11. Forced Monitor Mode Circuit (External Clock, No High Voltage)

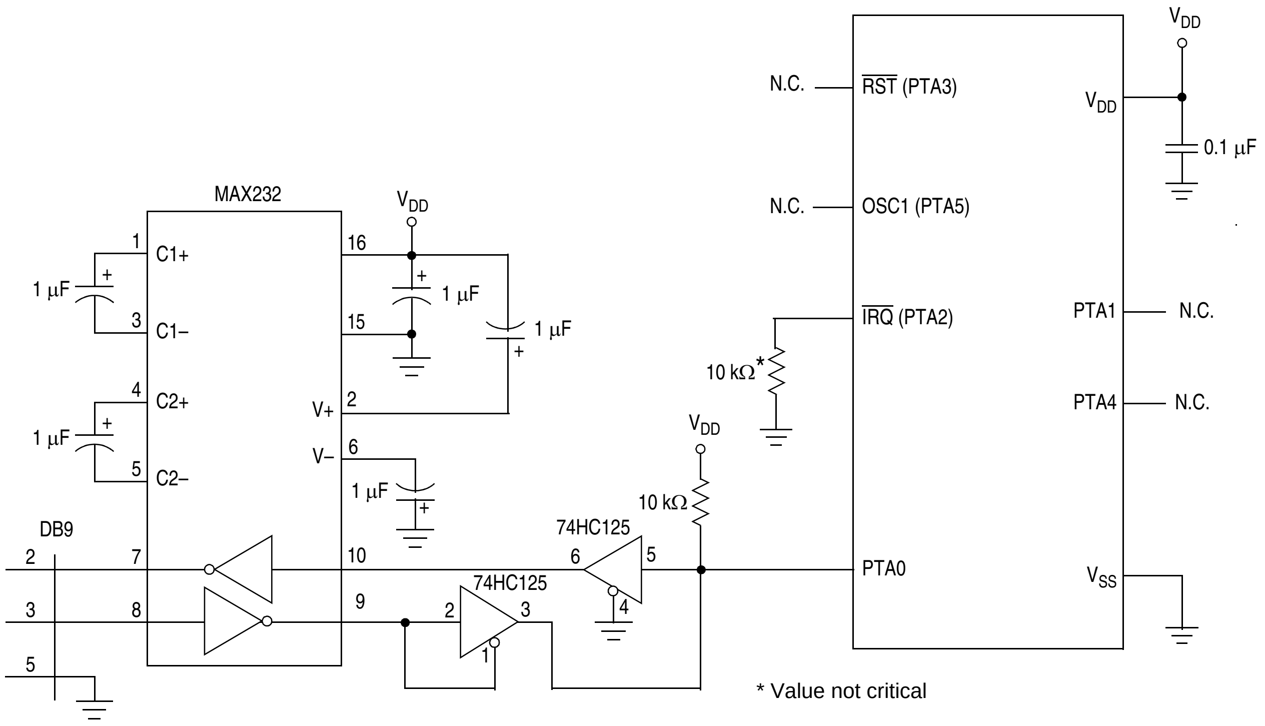


Figure 16-12. Forced Monitor Mode Circuit (Internal Clock, No High Voltage)

16.3.1.1 Normal Monitor Mode

$\overline{\text{RST}}$ and OSC1 functions will be active on the PTA3 and PTA5 pins respectively as long as V_{TST} is applied to the $\overline{\text{IRQ}}$ pin. If the $\overline{\text{IRQ}}$ pin is lowered (no longer V_{TST}) then the chip will still be operating in monitor mode, but the pin functions will be determined by the settings in the configuration registers (see **Section 5. Configuration Register (CONFIG)**) when V_{TST} was lowered. With V_{TST} lowered, the BIH and BIL instructions will read the $\overline{\text{IRQ}}$ pin state only if IRQEN is set in the CONFIG2 register.

If monitor mode was entered with V_{TST} on $\overline{\text{IRQ}}$, then the COP is disabled as long as V_{TST} is applied to $\overline{\text{IRQ}}$.

Table 16-1. Monitor Mode Signal Requirements and Options

Mode	$\overline{\text{IRQ}}$ (PTA2)	$\overline{\text{RST}}$ (PTA3)	Reset Vector	Serial Communication	Mode Selection		COP	Communication Speed			Comments
				PTA0	PTA1	PTA4		External Clock	Bus Frequency	Baud Rate	
Normal Monitor	V_{TST}	V_{DD}	X	1	1	0	Disabled	9.8304 MHz	2.4576 MHz	9600	Provide external clock at OSC1.
Forced Monitor	V_{DD}	X	\$FFFF (blank)	1	X	X	Disabled	9.8304 MHz	2.4576 MHz	9600	Provide external clock at OSC1.
	V_{SS}	X	\$FFFF (blank)	1	X	X	Disabled	X	3.2 MHz (Trimmed)	9600	Internal clock is active.
User	X	X	Not \$FFFF	X	X	X	Enabled	X	X	X	
MON08 Function [Pin No.]	V_{TST} [6]	$\overline{\text{RST}}$ [4]	—	COM [8]	MOD0 [12]	MOD1 [10]	—	OSC1 [13]	—	—	

1. PTA0 must have a pullup resistor to V_{DD} in monitor mode.
2. Communication speed in the table is an example to obtain a baud rate of 9600. Baud rate using external oscillator is bus frequency / 256 and baud rate using internal oscillator is bus frequency / 333.
3. External clock is a 9.8304 MHz oscillator on OSC1.
4. X = don't care
5. MON08 pin refers to P&E Microcomputer Systems' MON08-Cyclone 2 by 8-pin connector.

NC	1	2	GND
NC	3	4	$\overline{\text{RST}}$
NC	5	6	$\overline{\text{IRQ}}$
NC	7	8	PTA0
NC	9	10	PTA4
NC	11	12	PTA1
OSC1	13	14	NC
V_{DD}	15	16	NC

16.3.1.2 Forced Monitor Mode

If entering monitor mode without high voltage on $\overline{IRQ}$, then startup port pin requirements and conditions, (PTA1/PTA4) are not in effect. This is to reduce circuit requirements when performing in-circuit programming.

NOTE: *If the reset vector is blank and monitor mode is entered, the chip will see an additional reset cycle after the initial power-on reset (POR). Once the reset vector has been programmed, the traditional method of applying a voltage, V_{TST}, to $\overline{IRQ}$ must be used to enter monitor mode.*

If monitor mode was entered as a result of the reset vector being blank, the COP is always disabled regardless of the state of $\overline{IRQ}$.

If the voltage applied to the $\overline{IRQ}$ is less than V_{TST}, the MCU will come out of reset in user mode. Internal circuitry monitors the reset vector fetches and will assert an internal reset if it detects that the reset vectors are erased ($FF). When the MCU comes out of reset, it is forced into monitor mode without requiring high voltage on the $\overline{IRQ}$ pin. Once out of reset, the monitor code is initially executing with the internal clock at its default frequency.

If $\overline{IRQ}$ is held high, all pins will default to regular input port functions except for PTA0 and PTA5 which will operate as a serial communication port and OSC1 input respectively (refer to **Figure 16-11**). That will allow the clock to be driven from an external source through OSC1 pin.

If $\overline{IRQ}$ is held low, all pins will default to regular input port function except for PTA0 which will operate as serial communication port. Refer to **Figure 16-12**.

Regardless of the state of the $\overline{IRQ}$ pin, it will not function as a port input pin in monitor mode. Bit 2 of the Port A data register will always read 0. The BIH and BIL instructions will behave as if the $\overline{IRQ}$ pin is enabled, regardless of the settings in the configuration register. See **Section 5. Configuration Register (CONFIG)**.

The COP module is disabled in forced monitor mode. Any reset other than a power-on reset (POR) will automatically force the MCU to come back to the forced monitor mode.

16.3.1.3 Monitor Vectors

In monitor mode, the MCU uses different vectors for reset, SWI (software interrupt), and break interrupt than those for user mode. The alternate vectors are in the $FE page instead of the $FF page and allow code execution from the internal monitor firmware instead of user code.

NOTE: *Exiting monitor mode after it has been initiated by having a blank reset vector requires a power-on reset (POR). Pulling $\overline{RST}$ (when $\overline{RST}$ pin available) low will not exit monitor mode in this situation.*

Table 16-2 summarizes the differences between user mode and monitor mode regarding vectors.

Table 16-2. Mode Difference

Modes	Functions					
	Reset Vector High	Reset Vector Low	Break Vector High	Break Vector Low	SWI Vector High	SWI Vector Low
User	$FFFE	$FFFF	$FFFC	$FFFD	$FFFC	$FFFD
Monitor	$FEFE	$FEFF	$FEFC	$FEFD	$FEFC	$FEFD

16.3.1.4 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. Transmit and receive baud rates must be identical.

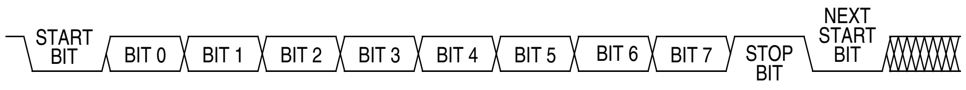


Figure 16-13. Monitor Data Format

16.3.1.5 Break Signal

A start bit (logic 0) followed by nine logic 0 bits is a break signal. When the monitor receives a break signal, it drives the PTA0 pin high for the duration of two bits and then echoes back the break signal.

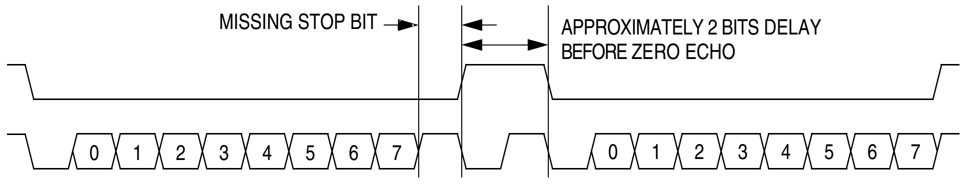


Figure 16-14. Break Transaction

16.3.1.6 Baud Rate

The monitor communication baud rate is controlled by the frequency of the external or internal oscillator and the state of the appropriate pins as shown in Table 16-1.

Table 16-1 also lists the bus frequencies to achieve standard baud rates. The effective baud rate is the bus frequency divided by 256 when using an external oscillator. When using the internal oscillator in forced monitor mode, the effective baud rate is the bus frequency divided by 335.

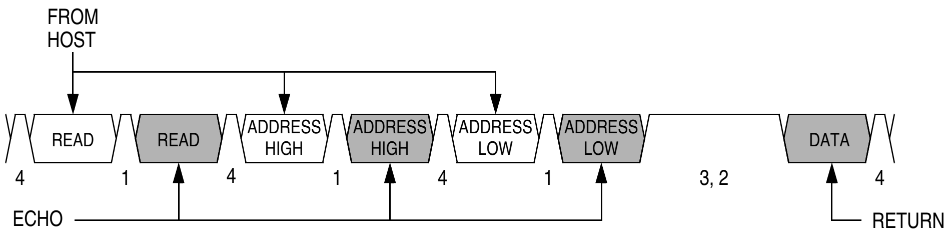
16.3.1.7 Commands

The monitor ROM firmware uses these commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

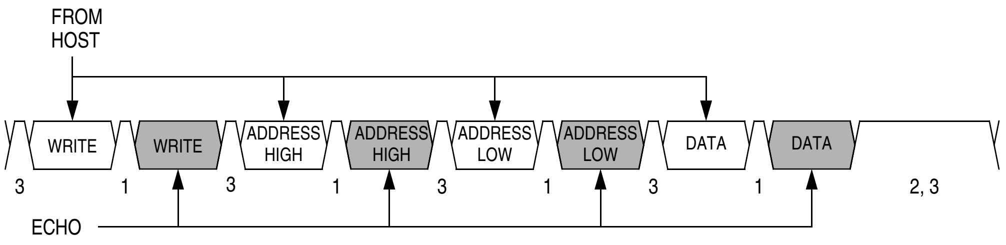
The monitor ROM firmware echoes each received byte back to the PTA0 pin for error checking. An 11-bit delay at the end of each command allows the host to send a break character to cancel the command. A delay of two bit times occurs before each echo and before READ, IREAD, or READSP data is returned. The data returned by a read command appears after the echo of the last byte of the command.

NOTE: *Wait one bit time after each echo before sending the next byte.*



Notes:
1 = Echo delay, approximately 2 bit times
2 = Data return delay, approximately 2 bit times
3 = Cancel command delay, 11 bit times
4 = Wait 1 bit time before sending next byte.

Figure 16-15. Read Transaction



Notes:
1 = Echo delay, approximately 2 bit times
2 = Cancel command delay, 11 bit times
3 = Wait 1 bit time before sending next byte.

Figure 16-16. Write Transaction

A brief description of each monitor mode command is given in Table 16-3 through Table 16-8.

Table 16-3. READ (Read Memory) Command

Description	Read byte from memory
Operand	2-byte address in high-byte:low-byte order
Data Returned	Returns contents of specified address
Opcode	$4A

Command Sequence

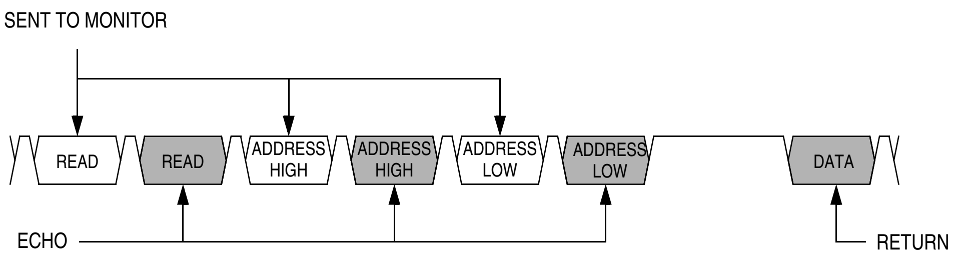


Table 16-4. WRITE (Write Memory) Command

Description	Write byte to memory
Operand	2-byte address in high-byte:low-byte order; low byte followed by data byte
Data Returned	None
Opcode	$49

Command Sequence

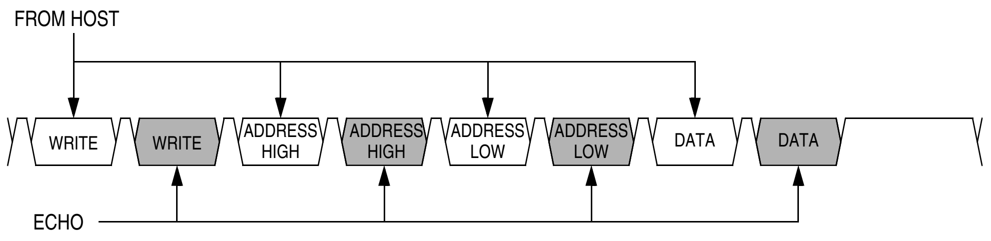


Table 16-5. IREAD (Indexed Read) Command

Description	Read next 2 bytes in memory from last address accessed
Operand	2-byte address in high byte:low byte order
Data Returned	Returns contents of next two addresses
Opcode	$1A

Command Sequence

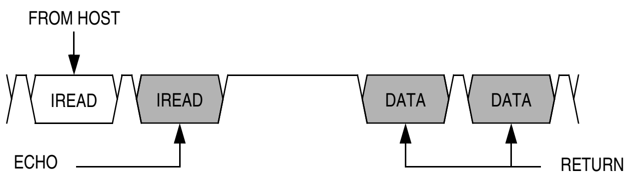
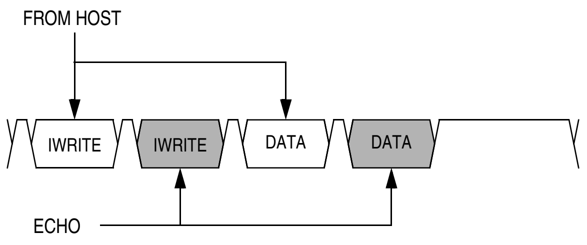


Table 16-6. IWRITE (Indexed Write) Command

Description	Write to last address accessed + 1
Operand	Single data byte
Data Returned	None
Opcode	$19
Command Sequence 	

A sequence of IREAD or IWRITE commands can access a block of memory sequentially over the full 64-Kbyte memory map.

Table 16-7. READSP (Read Stack Pointer) Command

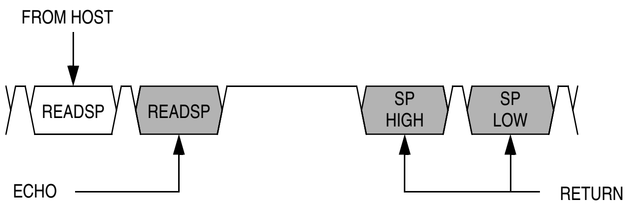
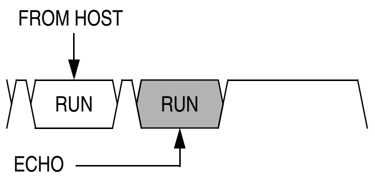
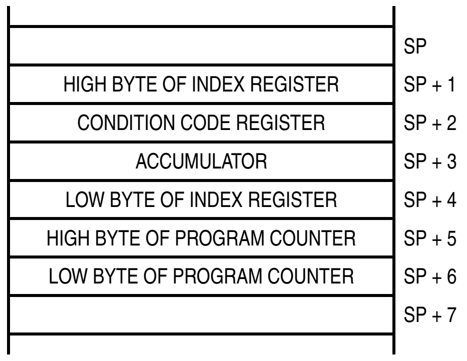
Description	Reads stack pointer
Operand	None
Data Returned	Returns incremented stack pointer value (SP + 1) in high-byte:low-byte order
Opcode	$0C
Command Sequence 	

Table 16-8. RUN (Run User Program) Command

Description	Executes PULH and RTI instructions
Operand	None
Data Returned	None
Opcode	$28
Command Sequence 	

The MCU executes the SWI and PSHH instructions when it enters monitor mode. The RUN command tells the MCU to execute the PULH and RTI instructions. Before sending the RUN command, the host can modify the stacked CPU registers to prepare to run the host program. The READSP command returns the incremented stack pointer value, SP + 1. The high and low bytes of the program counter are at addresses SP + 5 and SP + 6.



SP
HIGH BYTE OF INDEX REGISTER
SP + 1
CONDITION CODE REGISTER
SP + 2
ACCUMULATOR
SP + 3
LOW BYTE OF INDEX REGISTER
SP + 4
HIGH BYTE OF PROGRAM COUNTER
SP + 5
LOW BYTE OF PROGRAM COUNTER
SP + 6
SP + 7

Figure 16-17. Stack Pointer at Monitor Mode Entry

16.3.2 Security

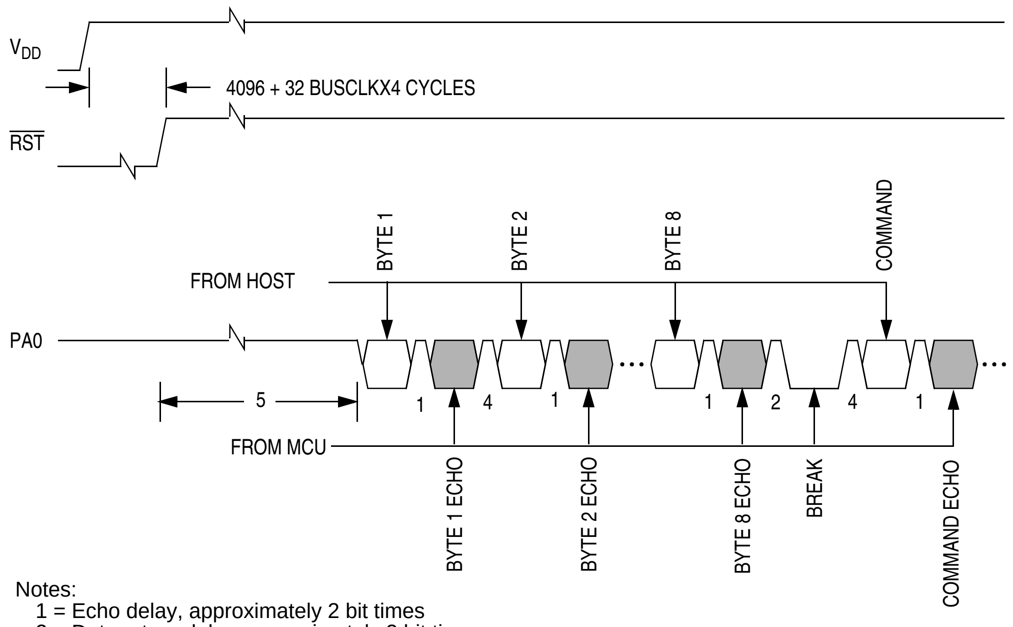
A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE: *Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors.*

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PTA0. If the received bytes match those at locations $FFF6–$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a power-on reset occurs. If the reset was not a power-on reset, security remains bypassed and security code entry is not required. See **Figure 16-18**.

Upon power-on reset, if the received bytes of the security code do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a FLASH location returns an invalid value and trying to execute code from FLASH causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

NOTE: *The MCU does not transmit a break character until after the host sends the eight security bytes.*



Notes:
1 = Echo delay, approximately 2 bit times
2 = Data return delay, approximately 2 bit times
4 = Wait 1 bit time before sending next byte
5 = Wait until the monitor ROM runs

Figure 16-18. Monitor Mode Entry Timing

To determine whether the security code entered is correct, check to see if bit 6 of RAM address $80 is set. If it is, then the correct security code has been entered and FLASH can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the FLASH module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become $FF (blank).

Section 17. Electrical Specifications

17.1 Introduction

This section contains electrical and timing specifications.

17.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the microcontroller unit (MCU) can be exposed without permanently damaging it.

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to **17.5 5-V DC Electrical Characteristics** and **17.9 3.3-V DC Electrical Characteristics** for guaranteed operating conditions.*

Characteristic[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +6.0	V
Input voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Mode entry voltage, $\overline{IRQ}$ pin	V_{TST}	V_{SS} –0.3 to +9.1	V
Maximum current per pin excluding PTA0–PTA5, V_{DD}, and V_{SS}	I	±15	mA
Maximum current for pins PTA0–PTA5	I_{PTA0}—I_{PTA5}	±25	mA
Storage temperature	T_{STG}	–55 to +150	°C
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current into V_{DD}	I_{MVDD}	100	mA

1. Voltages references to V_{SS}.

NOTE: *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}.)*

17.3 Functional Operating Range

Characteristic	Symbol	Value	Unit	Temp. Code
Operating temperature range (T_L to T_H)	T_A	– 40 to +125 – 40 to +105 – 40 to +85	°C	M V C
Operating voltage range(1) (V_{DDMIN} to V_{DDMAX})	V_{DD}	2.2 to 3.6	V	

1. V_{DD} must be above V_{TRIPR} upon power on.

17.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 16-pin PDIP 16-pin SOIC 16-pin TSSOP	θ_{JA}	 76 90 133	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD})$ $+ P_{I/O} = K/(T_J + 273°C)$	W
Constant(2)	K	$P_D \times (T_A + 273°C)$ $+ P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	T_{JM}	150	°C

1. Power dissipation is a function of temperature.
2. K constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.

17.5 5-V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage I_{Load} = –2.0 mA, all I/O pins I_{Load} = –10.0 mA, all I/O pins I_{Load} = –15.0 mA, PTA0, PTA1, PTA3–PTA5 only	V_{OH}	 V_{DD}–0.4 V_{DD}–1.5 V_{DD}–0.8	 — — —	 — — —	V
Maximum combined I_{OH} (all I/O pins)	I_{OHT}	—	—	50	mA
Output low voltage I_{Load} = 1.6 mA, all I/O pins I_{Load} = 10.0 mA, all I/O pins I_{Load} = 15.0 mA, PTA0, PTA1, PTA3–PTA5 only	V_{OL}	 — — —	 — — —	 0.4 1.5 0.8	V
Maximum combined I_{OL} (all I/O pins)	I_{OHL}	—	—	50	mA
Input high voltage PTA0–PTA5, PTB0–PTB7	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PTA0–PTA5, PTB0–PTB7	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
Input hysteresis	V_{HYS}	0.06 x V_{DD}	—	—	V
DC injection current, all ports	I_{INJ}	–2	—	+2	mA
Total dc current injection (sum of all I/O)	I_{INJTOT}	–25	—	+25	mA
Digital I/O ports Hi-Z leakage current Typical at 25 W°C	I_{IL}	–10 —	— ±0.1	+10 —	µA
Digital input only ports leakage current (PA2/$\overline{IRQ}$/$\overline{KBI2}$)	I_{IN}	–1	—	+1	µA
Capacitance Ports (as input) Ports (as input)	 C_{IN} C_{OUT}	 — —	 — —	 12 8	pF
POR rearm voltage[3]	V_{POR}	0	—	100	mV
POR rise time ramp rate[4]	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage	V_{TST}	V_{DD} + 2.5	—	9.1	V
Pullup resistors[5] PTA0–PTA5, PTB0–PTB7	R_{PU}	16	26	36	kΩ
Low-voltage inhibit reset, trip falling voltage	V_{TRIPF}	3.90	4.20	4.50	V
Low-voltage inhibit reset, trip rising voltage	V_{TRIPR}	4.00	4.30	4.60	V
Low-voltage inhibit reset/recover hysteresis	V_{HYS}	—	100	—	mV

1. V_{DD} = 3.0 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Maximum is highest voltage that POR is guaranteed.
4. If minimum V_{DD} is not reached before the internal POR reset is released, LVI will hold the part in reset until minimum V_{DD} is reached.
5. R_{PU1} and R_{PU2} are measured at V_{DD} = 5.0 V.

17.6 Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Internal operating frequency	f_{OP} (f_{Bus})	—	2	MHz
Internal clock period (1/f_{OP})	t_{cyc}	500	—	ns
$\overline{RST}$ input pulse width low	t_{RL}	175	—	ns
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	125	—	ns
$\overline{IRQ}$ interrupt pulse period	t_{ILIL}	Note[2]	—	t_{cyc}

1. V_{SS} = 0 Vdc; timing shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.
2. The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{cyc}.

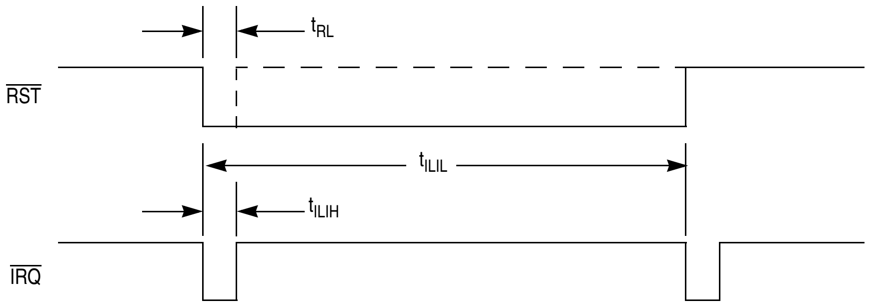


Figure 17-1. $\overline{RST}$ and $\overline{IRQ}$ Timing

17.7 Typical 5-V Output Drive Characteristics

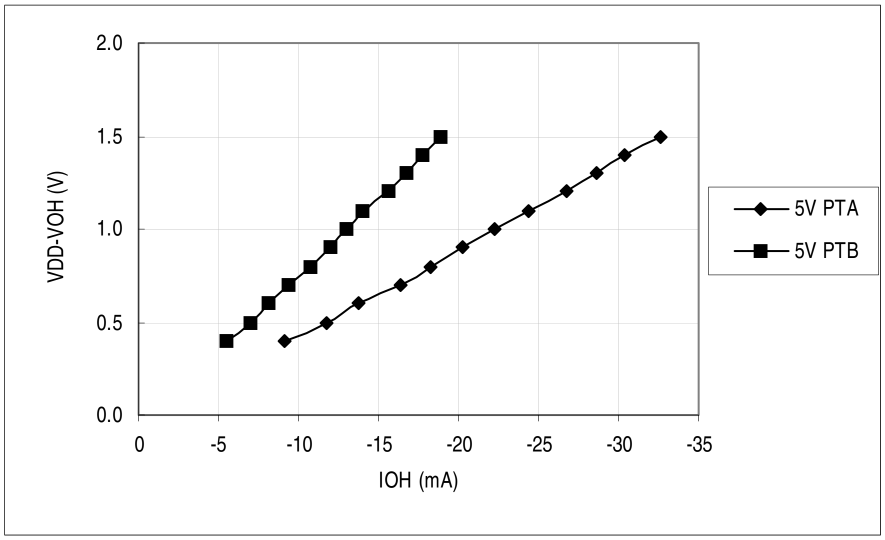


Figure 17-2. Typical 5-Volt Output High Voltage versus Output High Current (25°C)

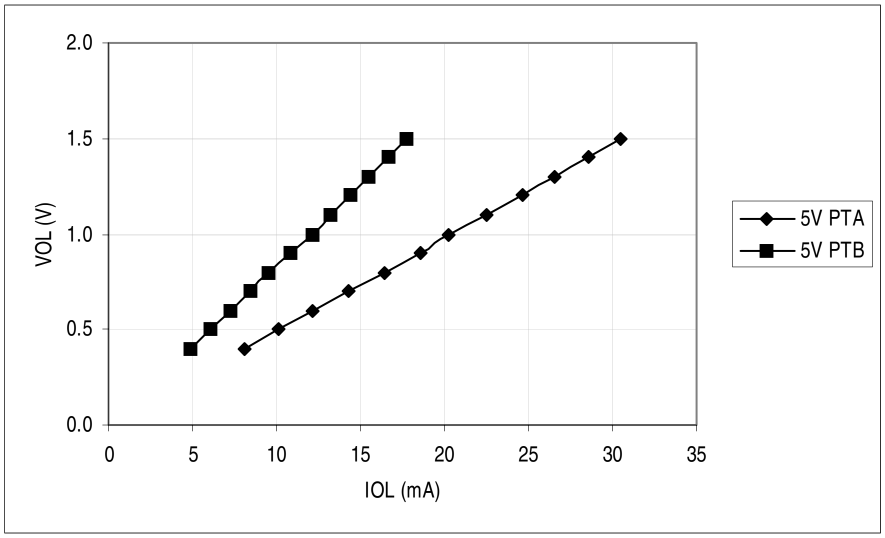


Figure 17-3. Typical 5-Volt Output Low Voltage versus Output Low Current (25°C)

17.8 5-V Oscillator Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator frequency(1)	f_{INTCLK}	—	25.6	—	MHz
Crystal frequency, XTALCLK(1)	$f_{OSCXCLK}$	8	—	32	MHz
External RC oscillator frequency, RCCLK(1)	f_{RCCLK}	2	—	12	MHz
External clock reference frequency(1) (2)	$f_{OSCXCLK}$	dc	—	32	MHz
Crystal load capacitance(3)	C_L	—	20	—	pF
Crystal fixed capacitance(2)	C_1	—	2 x C_L	—	—
Crystal tuning capacitance(2)	C_2	—	2 x C_L	—	—
Feedback bias resistor	R_B	—	10	—	MΩ
RC oscillator external resistor	R_{EXT}	See **Figure 17-4**			—

1. Bus frequency, f_{OP}, is oscillator frequency divided by 4.
2. No more than 10% duty cycle deviation from 50%.
3. Consult crystal vendor data sheet.

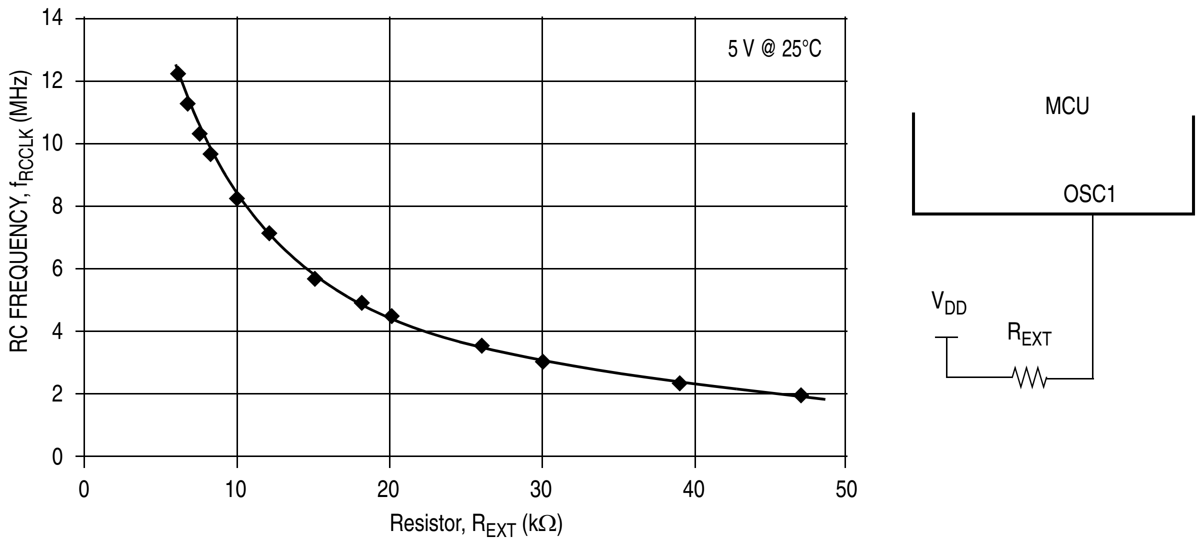


Figure 17-4. RC versus Frequency (5 Volts @ 25°C)

17.9 3.3-V DC Electrical Characteristics

Characteristic(1)	Symbol	Min	Typ(2)	Max	Unit
Output high voltage I_{Load} = –0.6 mA, all I/O pins I_{Load} = –4.0 mA, all I/O pins I_{Load} = –10.0 mA, PTA0, PTA1, PTA3–PTA5 only	V_{OH}	 V_{DD}–0.3 V_{DD}–1.0 V_{DD}–0.8	 — — —	 — — —	V
Maximum combined I_{OH} (all I/O pins)	I_{OHT}	—	—	50	mA
Output low voltage I_{Load} = 0.5 mA, all I/O pins I_{Load} = 6.0 mA, all I/O pins I_{Load} = 10.0 mA, PTA0, PTA1, PTA3–PTA5 only	V_{OL}	 — — —	 — — —	 0.3 1.0 0.8	V
Maximum combined I_{OL} (all I/O pins)	I_{OHL}	—	—	50	mA
Input high voltage PTA0–PTA5, PTB0–PTB7	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PTA0–PTA5, PTB0–PTB7	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
Input hysteresis	V_{HYS}	0.06 x V_{DD}	—	—	V
DC injection current, all ports	I_{INJ}	–2	—	+2	mA
Total dc current injection (sum of all I/O)	I_{INJTOT}	–25	—	+25	mA
Digital I/O ports Hi-Z leakage current Typical at 25°C	I_{IL}	–10 —	— ±0.5	+10 —	µA
Digital input only ports leakage current (PA2/$\overline{IRQ}$/KBI2)	I_{IN}	–1	—	+1	µA
Capacitance Ports (as input) Ports (as input)	 C_{IN} C_{OUT}	 — —	 — —	 12 8	pF
POR rearm voltage(3)	V_{POR}	0	—	100	mV
POR rise time ramp rate(4)	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage	V_{TST}	V_{DD} + 2.5	—	V_{DD} + 4.0	V
Pullup resistors(5) PTA0–PTA5, PTB0–PTB7	R_{PU}	16	26	36	kΩ
Low-voltage inhibit reset, trip falling voltage	V_{TRIPF}	2.65	2.8	3.0	V
Low-voltage inhibit reset, trip rising voltage	V_{TRIPR}	2.75	2.9	3.10	V
Low-voltage inhibit reset/recover hysteresis	V_{HYS}	—	60	—	mV

1. V_{DD} = 3.0 to 3.6 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Maximum is highest voltage that POR is guaranteed.
4. If minimum V_{DD} is not reached before the internal POR reset is released, LVI will hold the part in reset until minimum V_{DD} is reached.
5. R_{PU1} and R_{PU2} are measured at V_{DD} = 3.0 V

17.10 Typical 3.3-V Output Drive Characteristics

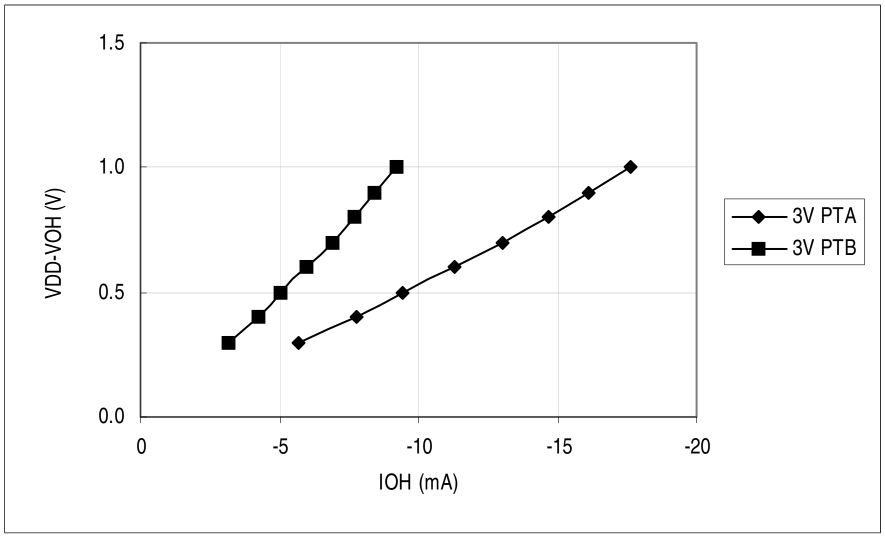


Figure 17-5. Typical 3.3-Volt Output High Voltage versus Output High Current (25°C)

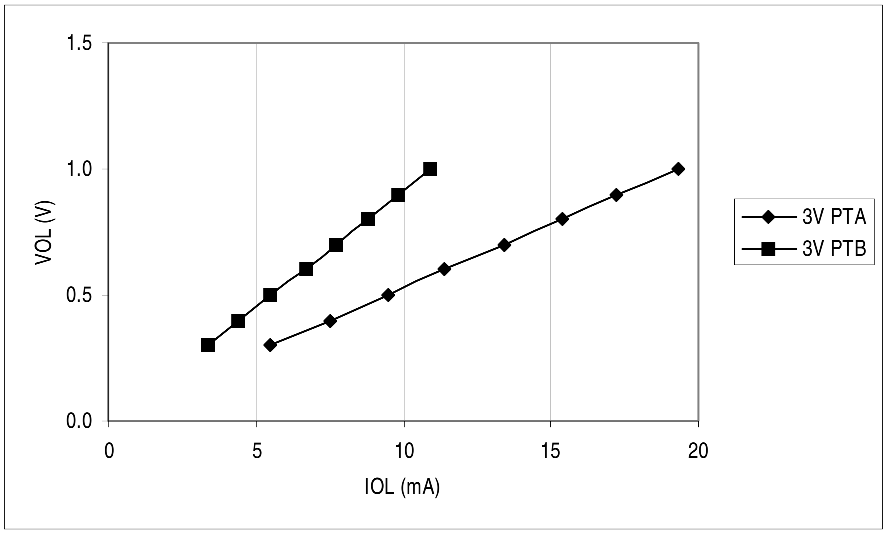


Figure 17-6. Typical 3.3-Volt Output Low Voltage versus Output Low Current (25°C)

17.11 3.3-V Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Internal operating frequency[2]	f_{OP}	—	4	MHz
$\overline{RST}$ input pulse width low[3]	t_{IRL}	1.5	—	µs

1. V_{DD} = 3.0 to 3.6 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H; timing shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.
2. Some modules may require a minimum frequency greater than dc for proper operation; see appropriate table for this information.
3. Minimum pulse width reset is guaranteed to be recognized. It is possible for a smaller pulse width to cause a reset.

17.12 3.3-V Oscillator Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Internal oscillator frequency[1]	f_{INTCLK}	—	12.8	—	MHz
Crystal frequency, XTALCLK[1]	$f_{OSCXCLK}$	8	—	16	MHz
External RC oscillator frequency, RCCLK[1]	f_{RCCLK}	2	—	12	MHz
External clock reference frequency[1] [2]	$f_{OSCXCLK}$	dc	—	16	MHz
Crystal load capacitance[3]	C_L	—	20	—	pF
Crystal fixed capacitance[2]	C_1	—	2 x C_L	—	—
Crystal tuning capacitance[2]	C_2	—	2 x C_L	—	—
Feedback bias resistor	R_B	—	10	—	MΩ
RC oscillator external resistor	R_{EXT}	See Figure 17-7			—

1. Bus frequency, f_{OP}, is oscillator frequency divided by 4.
2. No more than 10% duty cycle deviation from 50%
3. Consult crystal vendor data sheet

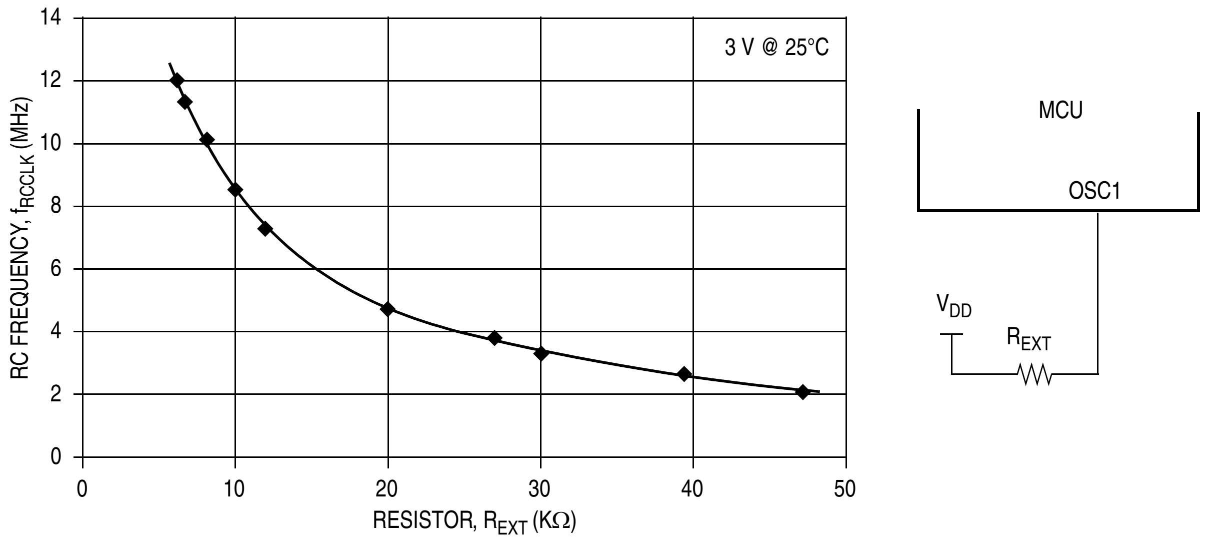


Figure 17-7. RC versus Frequency (3 Volts @ 25°C)

17.13 Supply Current Characteristics

Characteristic[1]	Voltage	Bus Freq. (MHz)	Symbol	Typ	Max	Unit
Run mode V_{DD} supply current[2]	5.0 3.3	4 4	RI_{DD}	4.5 2.7	— —	mA
WAIT mode V_{DD} supply current[3]	5.0 3.3	4 4	WI_{DD}	1.7 1.0	— —	mA
Stop mode V_{DD} supply current[4] –40 to 85°C –40 to 105°C –40 to 125°C 25°C 25°C with auto wake-up enabled Incremental current with LVI enabled at 25°C	5.0		SI_{DD}	0.10 0.22 0.34 6.50 5.70 125	— — — — — —	µA µA µA nA µA µA
–40 to 85°C –40 to 105°C –40 to 125°C 25°C 25°C with auto wake-up enabled Incremental current with LVI enabled at 25°C	3.3			0.10 0.14 0.18 4.60 1.30 102	— — — — — —	µA µA µA nA µA µA

1. V_{DD} = 3.3 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Run (operating) I_{DD} measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Measured with all modules enabled.
3. Wait (operating) I_{DD} measured using external square wave clock source. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Measured with all modules enabled.
4. Stop I_{DD} measured with all ports driven 0.2 V or less from rail. No dc loads. On the 8-pin versions, port B is configured as inputs with pullups enabled.

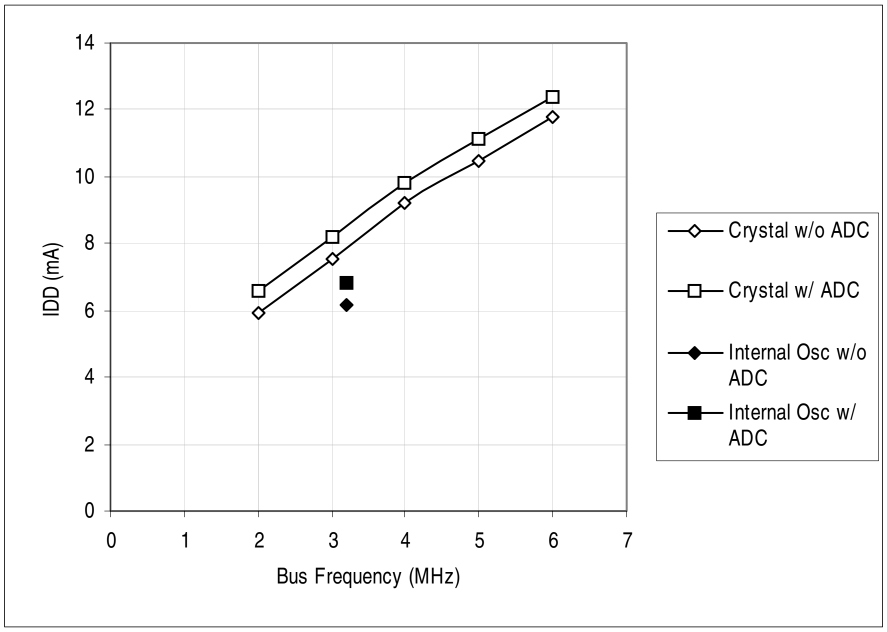


Figure 17-8. Typical 5-Volt Run Current versus Bus Frequency (25°C)

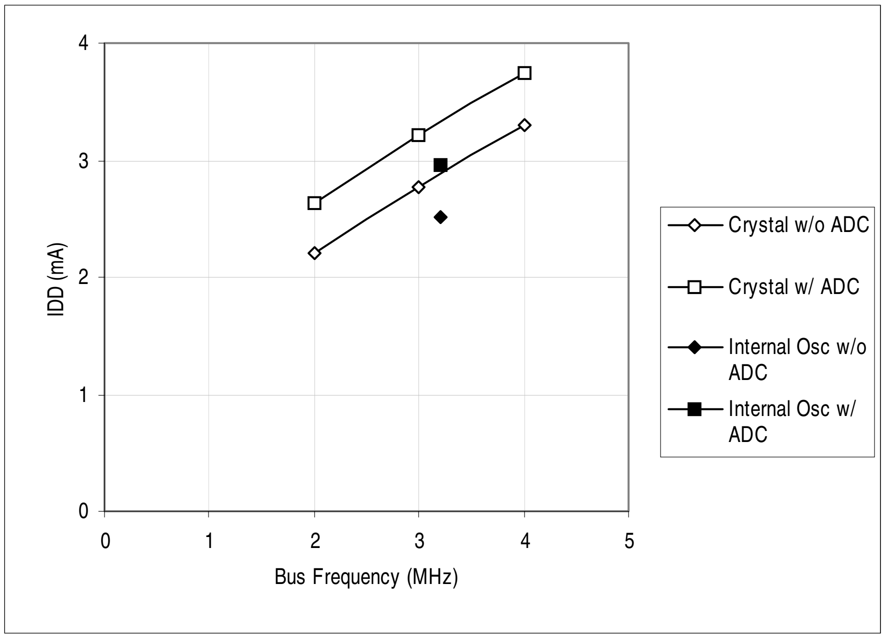


Figure 17-9. Typical 3.3-Volt Run Current versus Bus Frequency (25°C)

17.14 Analog-to-Digital Converter Characteristics

Characteristic	Symbol	Min	Max	Unit	Comments
Supply voltage	V_{DDAD}	3.0 (V_{DD} min)	5.5 (V_{DD} max)	V	—
Input voltages	V_{ADIN}	V_{SS}	V_{DD}	V	—
Resolution	B_{AD}	8	8	Bits	—
Absolute accuracy	A_{AD}	± 0.5	± 1.5	LSB	Includes quantization
ADC internal clock	f_{ADIC}	0.5	1.048	MHz	$t_{ADIC} = 1/f_{ADIC}$, tested only at 1 MHz
Conversion range	R_{AD}	V_{SS}	V_{DD}	V	—
Power-up time	t_{ADPU}	16	—	t_{ADIC} cycles	$t_{ADIC} = 1/f_{ADIC}$
Conversion time	t_{ADC}	16	17	t_{ADIC} cycles	$t_{ADIC} = 1/f_{ADIC}$
Sample time(1)	t_{ADS}	5	—	t_{ADIC} cycles	$t_{ADIC} = 1/f_{ADIC}$
Zero input reading(2)	Z_{ADI}	00	01	Hex	$V_{IN} = V_{SS}$
Full-scale reading(3)	F_{ADI}	FE	FF	Hex	$V_{IN} = V_{DD}$
Input capacitance	C_{ADI}	—	8	pF	Not tested
Input leakage(3)	$\|I_{INADC}\|$	—	± 1	µA	—

1. Source impedances greater than 10 kΩ adversely affect internal RC charging time during input sampling.
2. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.
3. The external system error caused by input leakage current is approximately equal to the product of R source and input current.

17.15 Timer Interface Module Characteristics

Characteristic	Symbol	Min	Max	Unit
Timer input capture pulse width	t_{TH}, t_{TL}	2	—	t_{cyc}
Timer Input capture period	t_{TLTL}	Note(1)	—	t_{cyc}
Timer input clock pulse width	t_{TCL}, t_{TCH}	t_{cyc} + 5	—	ns

1. The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{cyc}.

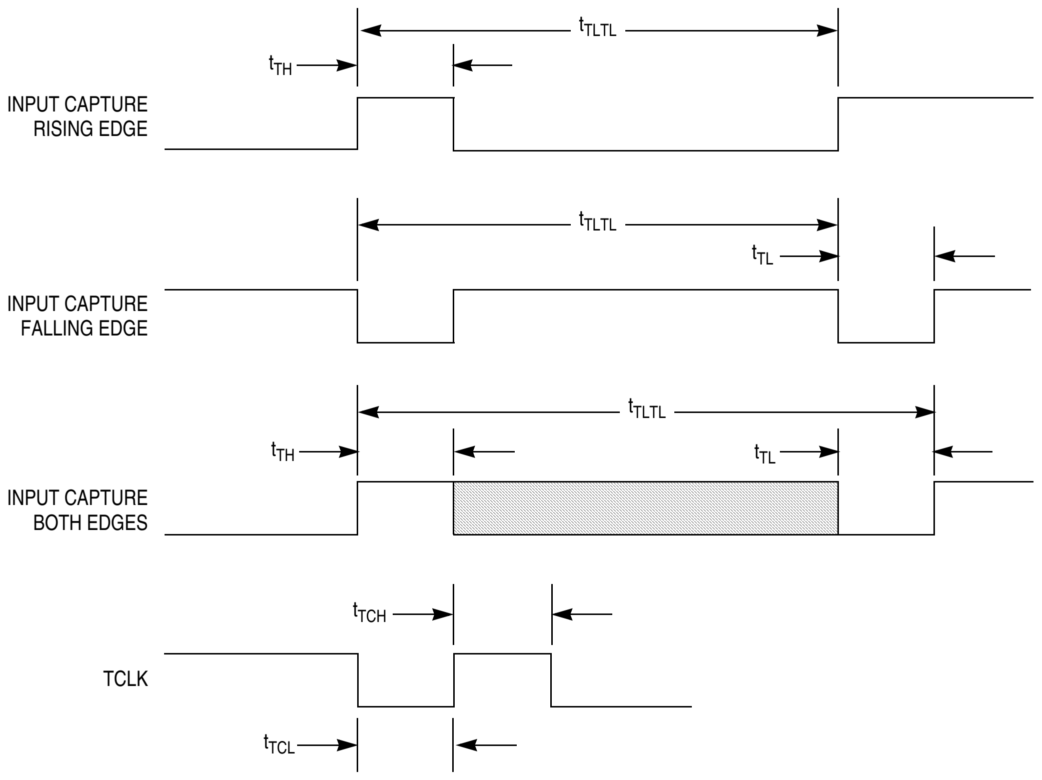


Figure 17-10. Input Capture Timing

17.16 Memory Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	—	V
FLASH program bus clock frequency	—	1	—	—	MHz
FLASH read bus clock frequency	f_{Read}(1)	0	—	8 M	Hz
FLASH page erase time <1 K cycles >1 K cycles	t_{Erase}	 0.9 3.6	 1 4	 1.1 5.5	ms
FLASH mass erase time	t_{MErase}	4	—	—	ms
FLASH PGM/ERASE to HVEN setup time	t_{NVS}	10	—	—	µs
FLASH high-voltage hold time	t_{NVH}	5	—	—	µs
FLASH high-voltage hold time (mass erase)	t_{NVHL}	100	—	—	µs
FLASH program hold time	t_{PGS}	5	—	—	µs
FLASH program time	t_{PROG}	30	—	40	µs
FLASH return to read time	t_{RCV}(2)	1	—	—	µs
FLASH cumulative program HV period	t_{HV}(3)	—	—	4	ms
FLASH endurance(4)	—	10 k	100 k	—	Cycles
FLASH data retention time(5)	—	15	100	—	Years

1. f_{Read} is defined as the frequency range for which the FLASH memory can be read.
2. t_{RCV} is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to 0.
3. t_{HV} is defined as the cumulative high voltage programming time to the same row before next erase. t_{HV} must satisfy this condition: $t_{NVS} + t_{NVH} + t_{PGS} + (t_{PROG} \times 32) \leq t_{HV}$ maximum.
4. Typical endurance was evaluated for this product family. For additional information on how Motorola defines. *Typical Endurance*, please refer to Engineering Bulletin EB619.
5. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Motorola defines *Typical Data Retention*, please refer to Engineering Bulletin EB618.

Section 18. Ordering Information and Mechanical Specifications

18.1 Introduction

This section provides ordering information for the MC68HC908QL4, MC68HC908QL3, and MC68HC908QL2 along with the dimensions for:

- 16-pin plastic dual in-line package (PDIP
- 16-pin small outline integrated circuit (SOIC) package
- 16-pin thin shrink small outline package (TSSOP)

The following figures show the latest package drawings at the time of this publication. To make sure that you have the latest package specifications, contact your local Motorola Sales Office.

18.2 MC Order Numbers

Table 18-1. MC Order Numbers

MC Order Number	ADC	FLASH Memory	Package
MC68HC908QL4	Yes	4096 bytes	16-pins PDIP, SOIC, and TSSOP
MC68HC908QL3	No	4096 bytes	
MC68HC908QL2	Yes	2048 bytes	

Temperature and package designators:
C = –40°C to +85°C
V = –40°C to +105°C (available for V_{DD} = 5 V only)
M = –40°C to +125°C (available for V_{DD} = 5 V only)
P = Plastic dual in-line package (PDIP)
DW = Small outline integrated circuit package (SOIC)
DT = Thin shrink small outline package (TSSOP)

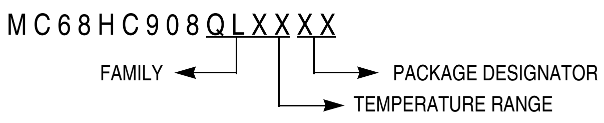
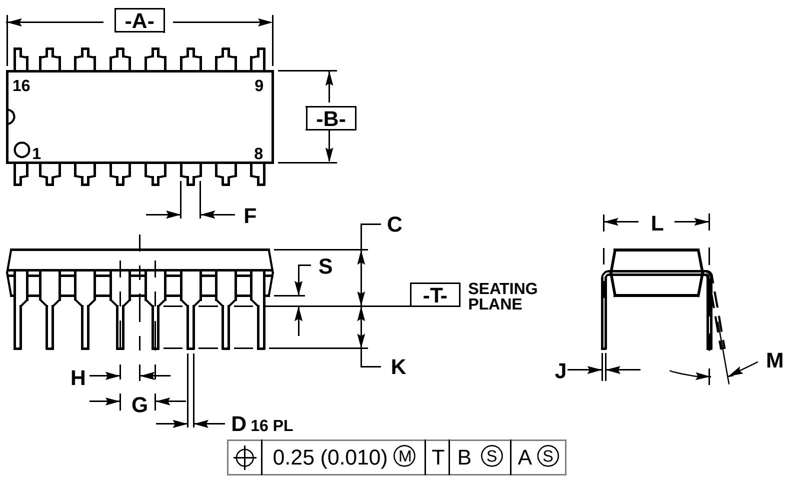


Figure 18-1. Device Numbering System

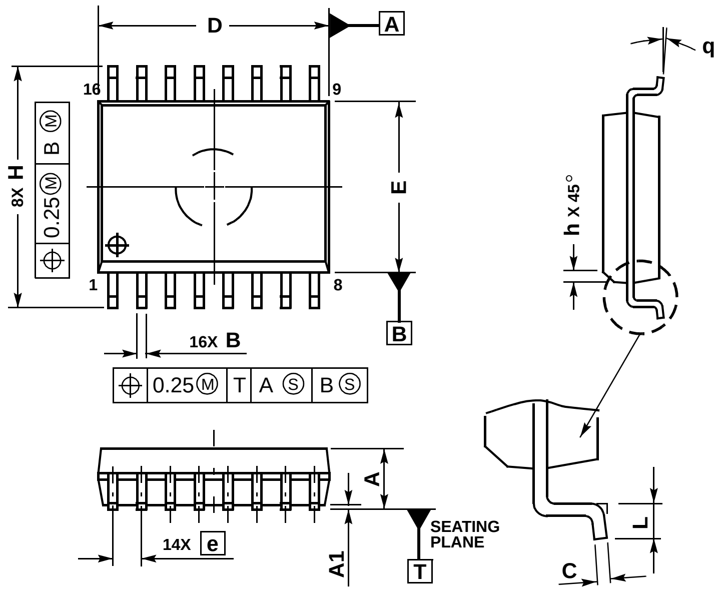
18.3 16-Pin Plastic Dual In-Line Package (Case #648D)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
6. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.760	18.80	19.30
B	0.245	0.260	6.23	6.60
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.120	0.140	3.05	3.55
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.015	0.035	0.39	0.88

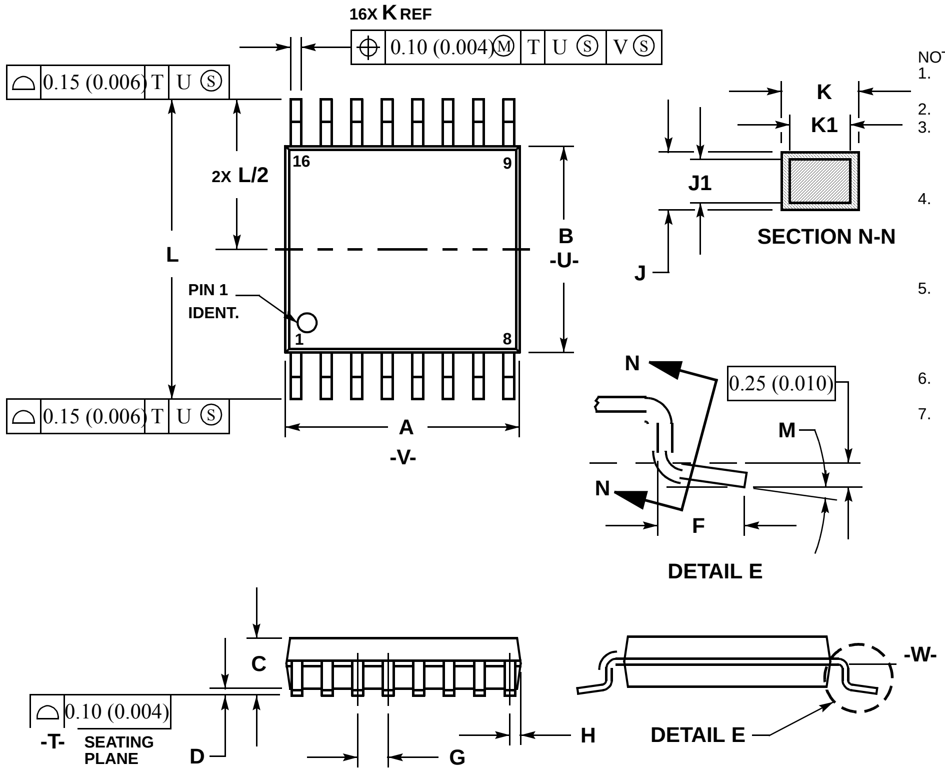
18.4 16-Pin Small Outline Integrated Circuit Package (Case #751G)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.40	1.00
q	0 °	7 °

18.5 16-Pin Thin Shrink Small Outline Package (Case #948F)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

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MC68HC908QL4/D
Rev. 0
9/2003