

#### DESCRIPTION

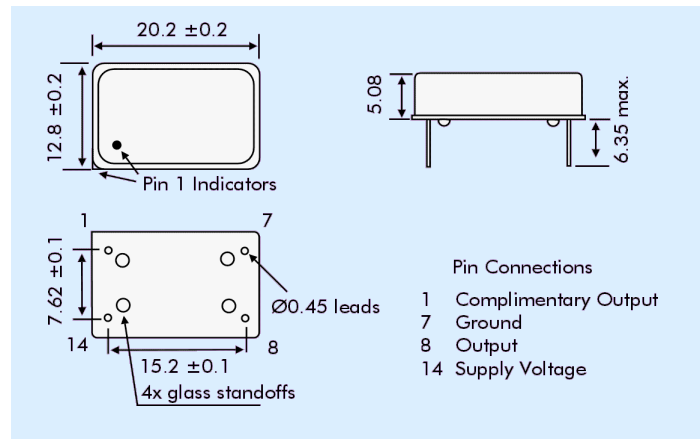
HDF14 series LVDS output oscillators cover the frequency range 38MHz to 640MHz. The design contains a high 'Q' fundamental crystal and utilizes a low jitter multiplier circuit.

#### SPECIFICATION

Frequency Range:	38.0MHz to 640.0MHz
Output Logic	LVDS
Phase Noise:	See table
Frequency Stability:	See table
Operating Temp Range	
Commercial:	-10° to +70°C
Industrial:	-40° to +85°C
Input Voltage:	+2.5V or +3.3VDC $\pm$ 5%
Output Logic	
High '1' V <sub>OH</sub> :	1.4V typical, 1.6V max.
Low '0' V <sub>OL</sub> :	0.9V min., 1.1V typical
Differential Output Voltage V <sub>OD</sub> :	247mV min., 355mV typ., 454mV max. Output 1 - Output 2
Differential Output Error dV <sub>OD</sub> :	-50mV min., 50mV max.
Output Offset Voltage V <sub>OS</sub> :	1.125V min., 1.20V typ., 1.375V max.
Offset Magnitude Error dV <sub>OS</sub> :	0mV min., 3mV typ., 25mV max.
Rise/Fall Times:	0.7ns typical, 1.0ns max. (20% to 80% of LVDS waveform)
Current Consumption (15pF load):	
38MHz to 100MHz:	45mA max.
100.01 to 320MHz:	60mA max.
320.01 to 640MHz:	70mA max.
Load:	50Ω from each output
Start-up Time:	5ms typ., 10ms max.
Duty Cycle:	50% $\pm$ 5% (at 1.5V)
Drive Capability:	100 Ohms between outputs
Input Static Discharge Prot:	2kV min.
Storage Temperature Range:	-55°C to +150°C
Ageing:	$\pm$ 3ppm per year max., $\pm$ 2ppm thereafter. At T amb +25°C
Enable/Disable:	Function not available in 4 pin package



#### OUTLINE & DIMENSIONS



#### PHASE NOISE (156.250MHz)

Offset	dBc/Hz
10Hz	-62
100Hz	-92
1kHz	-120
10kHz	-132
100kHz	-128
1MHz	-140
10MHz	-150

#### JITTER (156.520MHz)

	Typ.	Max.
Integrated Phase Jitter: (12kHz to 20MHz)	0.4ps	0.5ps
Period Jitter: (RMS)	3.0ps	5.0ps
Period Jitter: (peak to peak)	20ps	30ps

#### STABILITY OVER TEMPERATURE RANGE

Stability $\pm$ ppm	Temperature Range °C	Order Code
25	-10 to +70	A
50	-10 to +70	B
100	-10 to +70	C
25	-40 to +85	D
50	-40 to +85	E
100	-40 to +85	F

#### PART NUMBERS

HDF14 oscillator part numbers are derived as follows:

