SAMSUNG ELECTRONICS

KS24C011/021/041/081

1K/2K/4K/8K-bit Serial EEPROM

Data Sheet

OVERVIEW

The KS24C011/021/041/081 serial EEPROM has a 1,024/2,048/4,096/8,192-bit (128/256/512/1,024-byte) capacity, supporting the standard I²C™-bus serial interface. It is fabricated using Samsung's most advanced CMOS technology. One of its major feature is a hardware-based write protection circuit for the entire memory area. Hardware-based write protection is controlled by the state of the write-protect (WP) pin. Using one-page write mode, you can load up to 16 bytes of data into the EEPROM in a single write operation. Another significant feature of the KS24C011/021/041/081 is its support for fast mode and standard mode.

FEATURES

I²C-Bus Interface

- Two-wire serial interface
- Automatic word address increment

EEPROM

- 1K/2K/4K/8K-bit (128/256/512/1,024-byte) storage area
- 16-byte page buffer
- Typical 3.5 ms write cycle time with auto-erase function
- Hardware-based write protection for the entire EEPROM (using the WP pin)
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycles
- 100 years data retention

Operating Characteristics

- Operating voltage
  - 2.5 V to 5.5 V (write)
  - 2.2 V to 5.5 V (read)
- Operating current
  - Maximum write current: < 3 mA at 5.5 V
  - Maximum read current: < 200 µA at 5.5 V
  - Maximum stand-by current: < 5 µA at 3.3 V
- Operating temperature range
  - – 25°C to + 70°C (commercial)
  - – 40°C to + 85°C (industrial)
- Operating clock frequencies
  - 100 kHz at standard mode
  - 400 kHz at fast mode
- Electrostatic discharge (ESD)
  - 3,000 V (HBM)
  - 300 V (MM)

Packages

- 8-pin DIP, SOP, and TSSOP

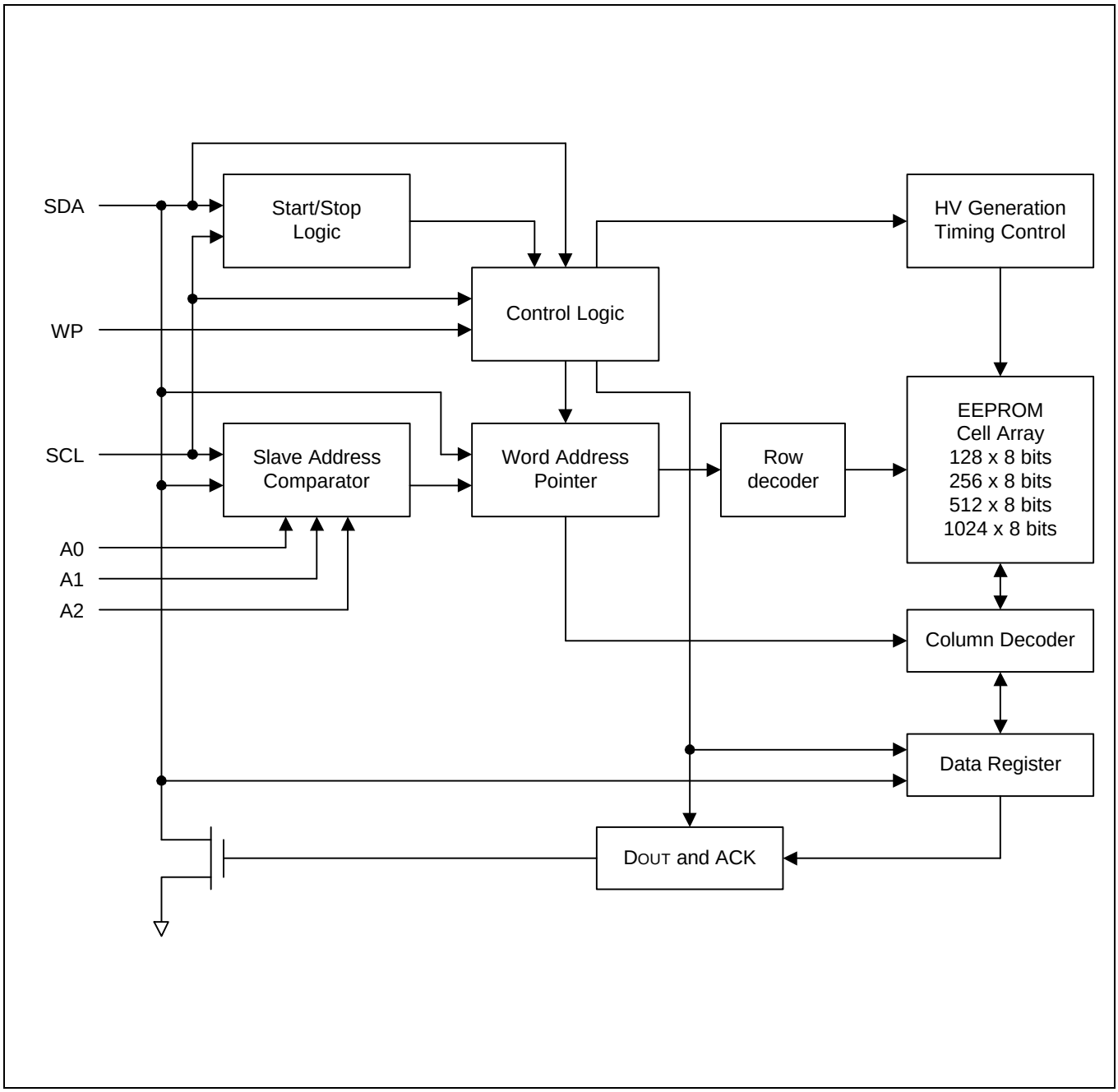
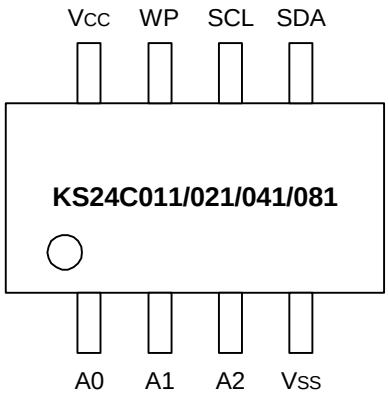


Figure 3-1. KS24C011/021/041/081 Block Diagram



NOTE: The KS24C011/021/041/081 is available in 8-pin DIP, SOP, and TSSOP package.

Figure 3-2. Pin Assignment Diagram

Table 3-1. KS24C011/021/041/081 Pin Descriptions

Name	Type	Description	Circuit Type
A0, A1, A2	Input	Input pins for device address selection. To configure a device address, these pins should be connected to the V_{CC} or V_{SS} of the device.	1
V_{SS}	–	Ground pin.	–
SDA	I/O	Bi-directional data pin for the I^2C-bus serial data interface. Schmitt trigger input and open-drain output. An external pull-up resistor must be connected to $V_{CC.}$ Typical values for this pull-up resistor are 4.7 kΩ (100 kHz) and 1 kΩ (400 kHz).	3
SCL	Input	Schmitt trigger input pin for serial clock input.	2
WP	Input	Input pin for hardware write protection control. If you tie this pin to $V_{CC,}$ the write function is disabled to protect previously written data in the entire memory; if you tie it to V_{SS}, the write function is enabled.	1
V_{CC}	–	Single power supply.	–

NOTE: See the following page for diagrams of pin circuit types 1, 2, and 3.

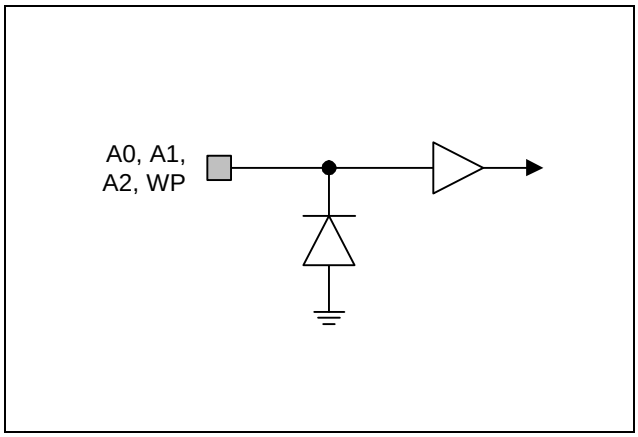


Figure 3-3. Pin Circuit Type 1

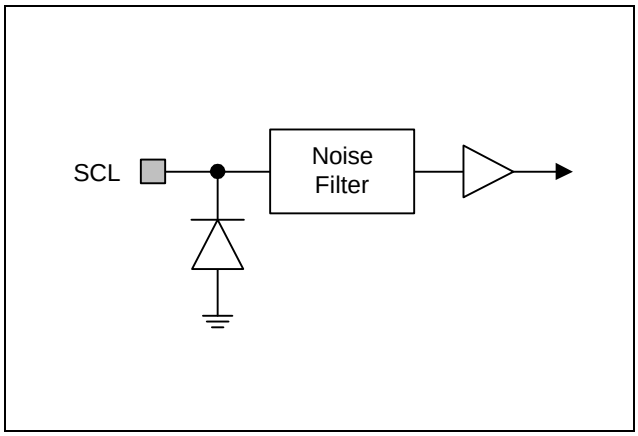


Figure 3-4. Pin Circuit Type 2

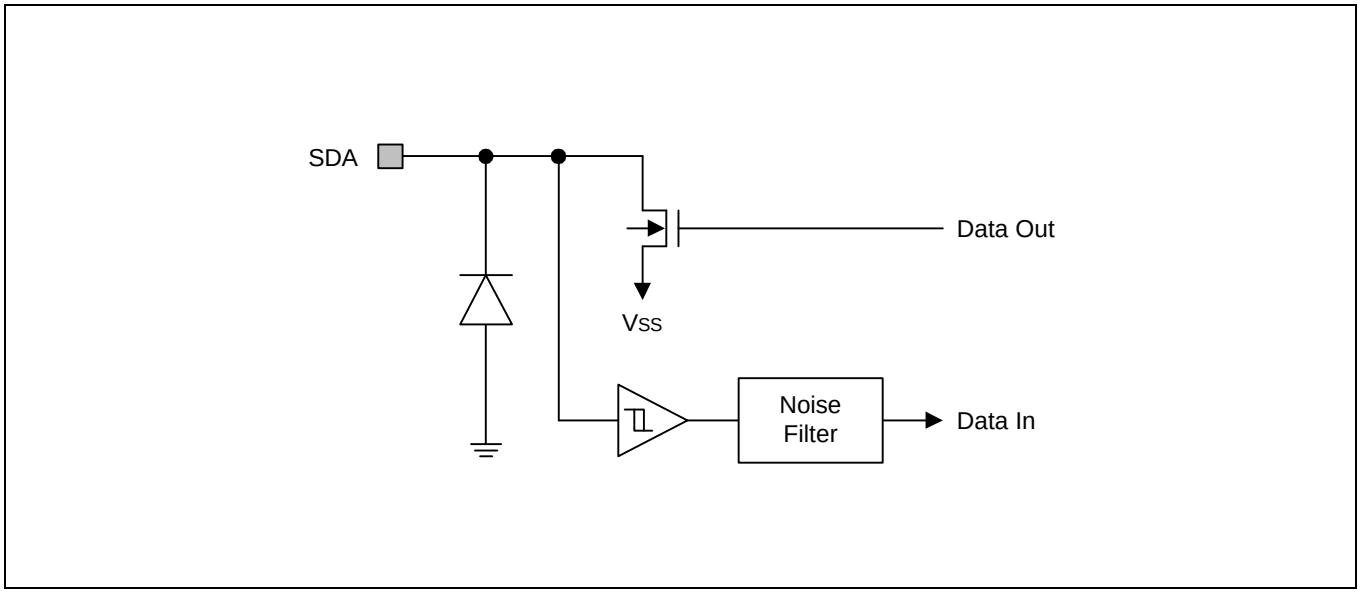


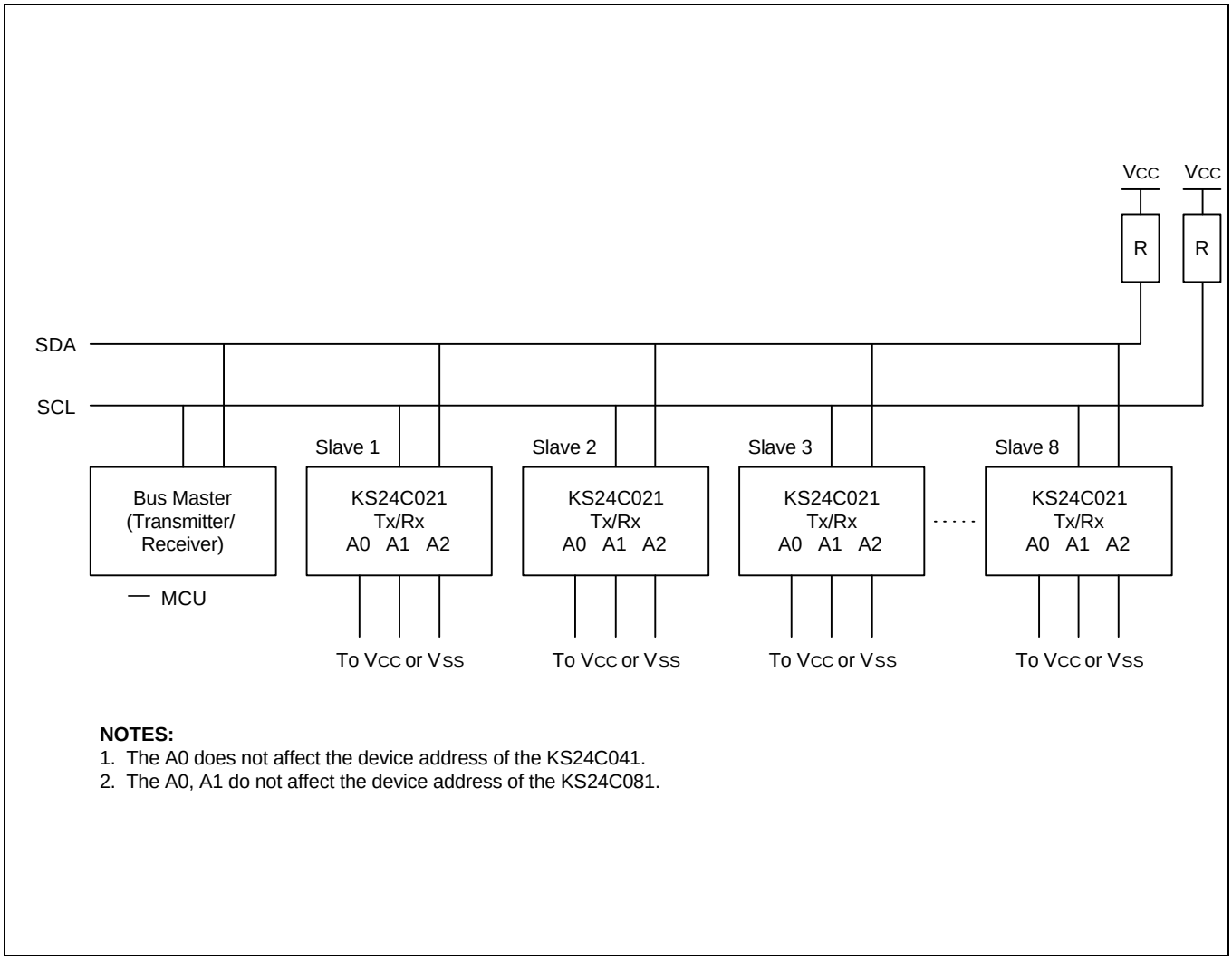
Figure 3-5. Pin Circuit Type 3

FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The KS24C011/021/041/081 supports the I²C-bus serial interface data transmission protocol. The two-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to V_{CC} by a pull-up resistor that is located somewhere on the bus.

Any device that puts data onto the bus is defined as the "transmitter" and any device that gets data from the bus is the "receiver." The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. Using the A0,A1 and A2 input pins, up to eight KS24C011/021 (four KS24C041, two for KS24C081) devices can be connected to the same I²C-bus as slaves (see Figure 3-6). Both the master and slaves can operate as transmitter or receiver, but the master device determines which bus operating mode would be active.



NOTES:
1. The A0 does not affect the device address of the KS24C041.
2. The A0, A1 do not affect the device address of the KS24C081.

Figure 3-6. Typical Configuration (16 Kbits of Memory on the I²C-Bus)

I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:

— A new data transfer can be initiated only when the bus is currently not busy.

— MSB is always transferred first in transmitting data.

— During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is High.

The I²C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain High level when the bus is not active.
- Start condition: Start condition is initiated by a High-to-Low transition of the SDA line while SCL remains High level. All bus commands must be preceded by a start condition.
- Stop condition: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains High level. All bus operations must be completed by a stop condition (see Figure 3-7).

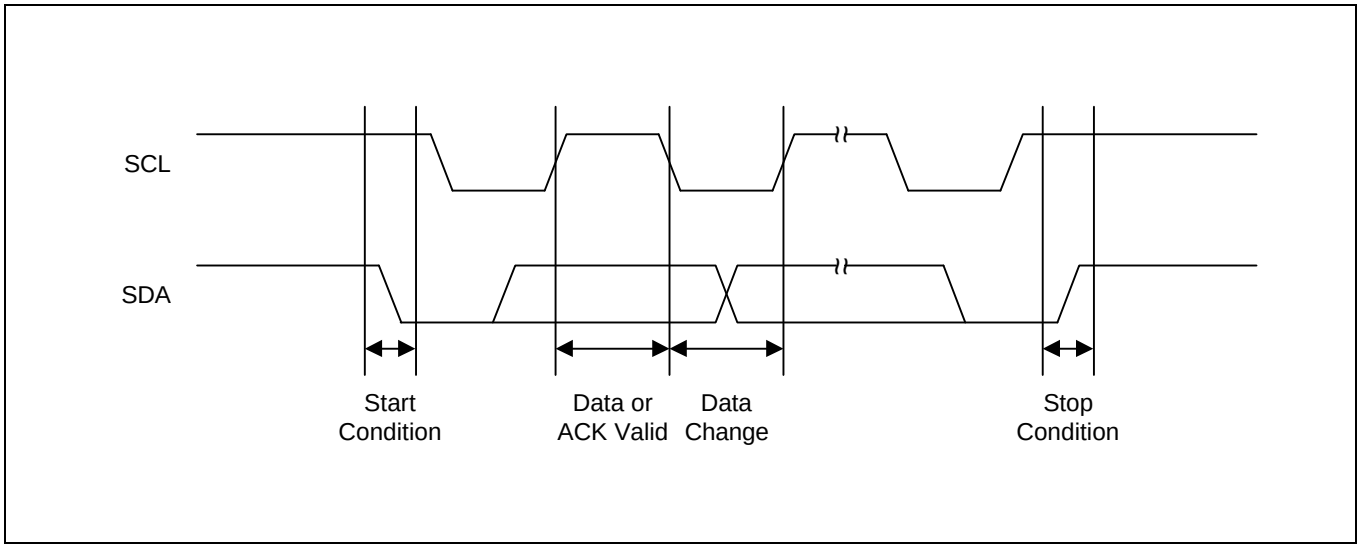


Figure 3-7. Data Transmission Sequence

- Data valid: Following a start condition, the data becomes valid if the data line remains stable for the duration of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total number of bytes that can be transferred in one operation is theoretically unlimited.
- ACK (Acknowledge): An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data (see Figure 3-8). But the slave does not send an ACK if an internal write cycle is still in progress.

  In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

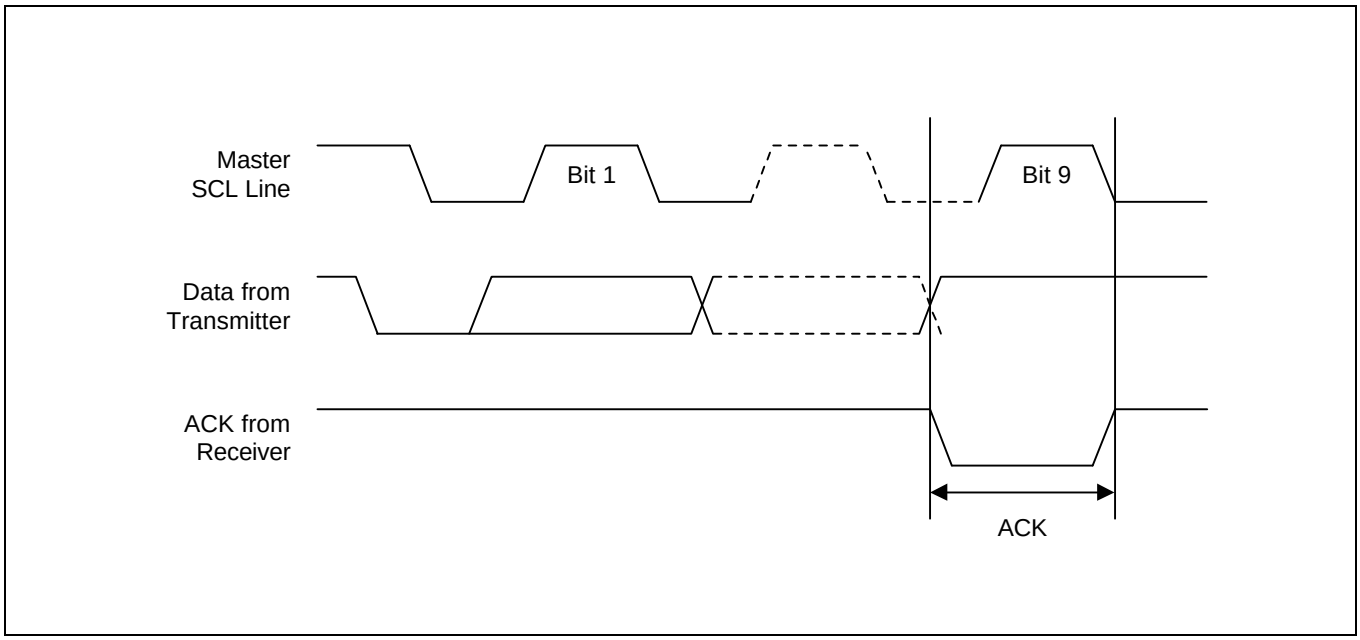


Figure 3-8. Acknowledge Response From Receiver

- Slave Address: After the master initiates a Start condition, it must output the address of the device to be accessed. The most significant four bits of the slave address are called the "device identifier". The identifier for the KS24C011/021/041/081 is "1010B". The next three bits comprise the address of a specific device. The device address is defined by the state of the A0, A1 and A2 pins. Using this addressing scheme, you can cascade up to eight KS24C011/021 or four KS24C041 or two KS24C081 on the bus (see Table 3-2 below). The b1 for the KS24C041 or the b1, b2 for KS24C081 are dont care bits. The bits which are "don't care" are used by the master to select which of the blocks of internal memory (1 block = 256 words) are to be accessed. The bits which are "don't care" are in effect the most significant bits of the word address.
- Read/Write: The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is "1", a read operation is executed. If it is "0", a write operation is executed.

Table 3-2. Slave Device Addressing

Device	Device Identifier				Device Address			R/W Bit
	b7	b6	b5	b4	b3	b2	b1	b0
KS24C011/021	1	0	1	0	A2	A1	A0	R/W
KS24C041	1	0	1	0	A2	A1	B0	R/W
KS24C081	1	0	1	0	A2	B1	B0	R/W

NOTE: The B2, B1, B0 correspond to the MSB of the memory array address word.

BYTE WRITE OPERATION

In a complete byte write operation, the master transmits the slave address, word address, and one data byte to the KS24C011/021/041/081 slave device (see Figure 3-9).

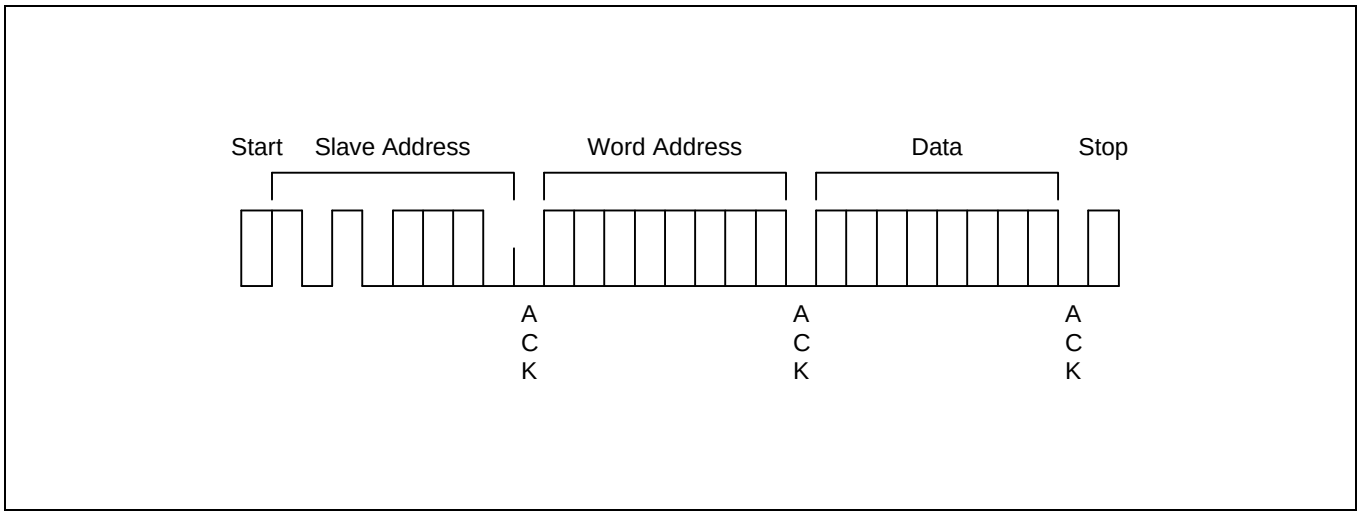


Figure 3-9. Byte Write Operation

Following the Start condition, the master sends the device identifier (4 bits), the device address (3 bits), and an R/W bit set to '0" onto the bus. Then the addressed KS24C011/021/041/081 generates an ACK and waits for the next byte. The next byte to be transmitted by the master is the word address. This 8-bit address is written into the word address pointer of the KS24C011/021/041/081.

When the KS24C011/021/041/081 receives the word address, it responds by issuing an ACK and then waits for the next 8-bit data. When it receives the data byte, the KS24C011/021/041/081 again responds with an ACK. The master terminates the transfer by generating a Stop condition, at which time the KS24C011/021/041/081 begins the internal write cycle.

While the internal write cycle is in progress, all KS24C011/021/041/081 inputs are disabled and the KS24C011/021/041/081 does not respond to additional requests from the master.

PAGE WRITE OPERATION

The KS24C011/021/041/081 can also perform 16-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 15 additional bytes. The KS24C011/021/041/081 responds with an ACK each time it receives a complete byte of data (see Figure 3-10).

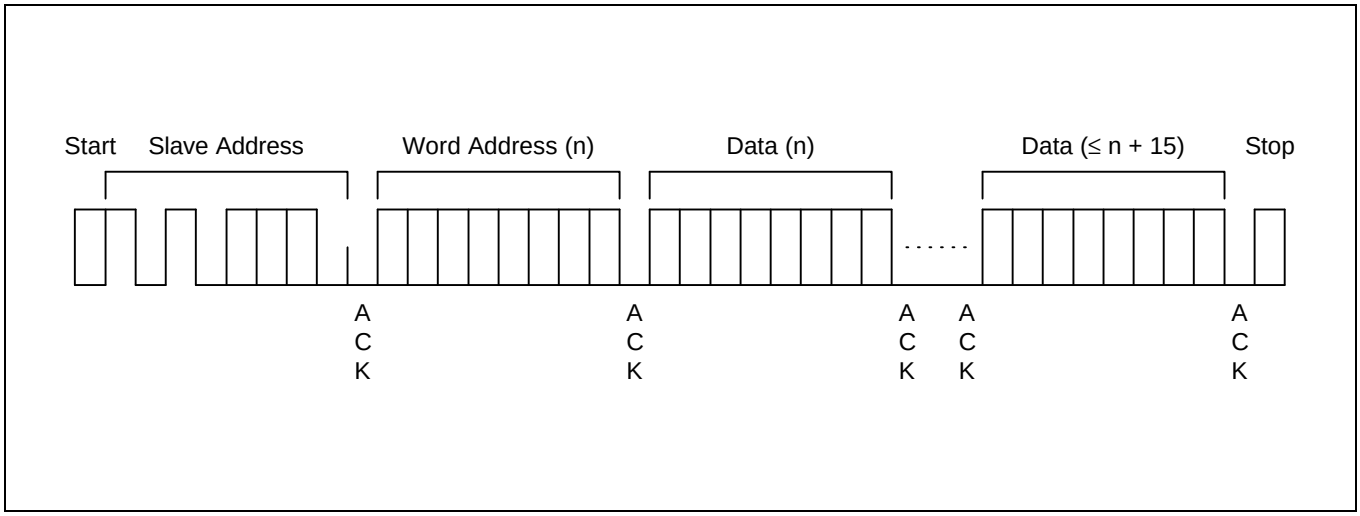


Figure 3-10. Page Write Operation

The KS24C011/021/041/081 automatically increments the word address pointer each time it receives a complete data byte. When one byte has been received, the internal word address pointer increments to the next address and the next data byte can be received.

If the master transmits more than 16 bytes before it generates a stop condition to end the page write operation, the KS24C011/021/041/081 word address pointer value "rolls over" and the previously received data is overwritten. If the master transmits less than 16 bytes and generates a stop condition, the KS24C011/021/041/081 writes the received data to the corresponding EEPROM address.

During a page write operation, all inputs are disabled and there is no response to additional requests from the master until the internal write cycle is completed.

POLLING FOR AN ACK SIGNAL

When the master issues a stop condition to initiate a write cycle, the KS24C011/021/041/081 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device.

To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the KS24C011/021/041/081 remains busy with the write operation, no ACK is returned. When the KS24C011/021/041/081 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation (see Figure 3-11).

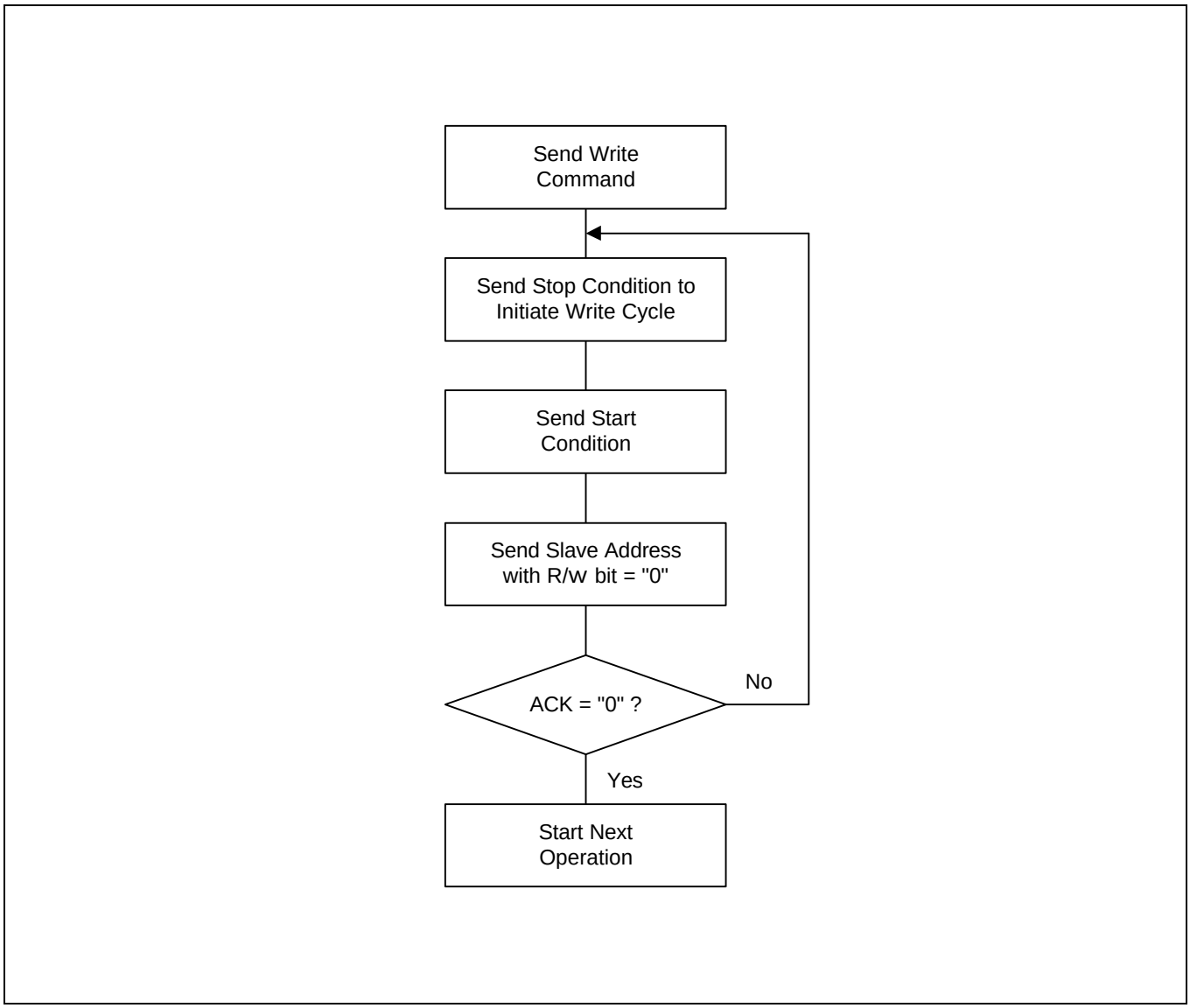


Figure 3-11. Master Polling for an ACK Signal from a Slave Device

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the KS24C011/021/041/081. This method of write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to V_{CC}, any attempt to write a value to the memory is ignored.
The KS24C011/021/041/081 will acknowledge slave and word address, but it will not generate an acknowledge after receiving the first byte of the data. Thus the write cycle will not be started when the stop condition is generated. By connecting the WP pin to V_{SS}, the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to prevent data from being overwritten. Whenever the write function is disabled, a slave address and a word address are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address "n", the next read operation would access data at address "n+1".

When the KS24C011/021/041/081 receives a slave address with the R/W bit set to "1", it issues an ACK and sends the eight bits of data. The master does not acknowledge the transfer but it does generate a Stop condition. In this way, the KS24C011/021/041/081 effectively stops the transmission (see Figure 3-12).

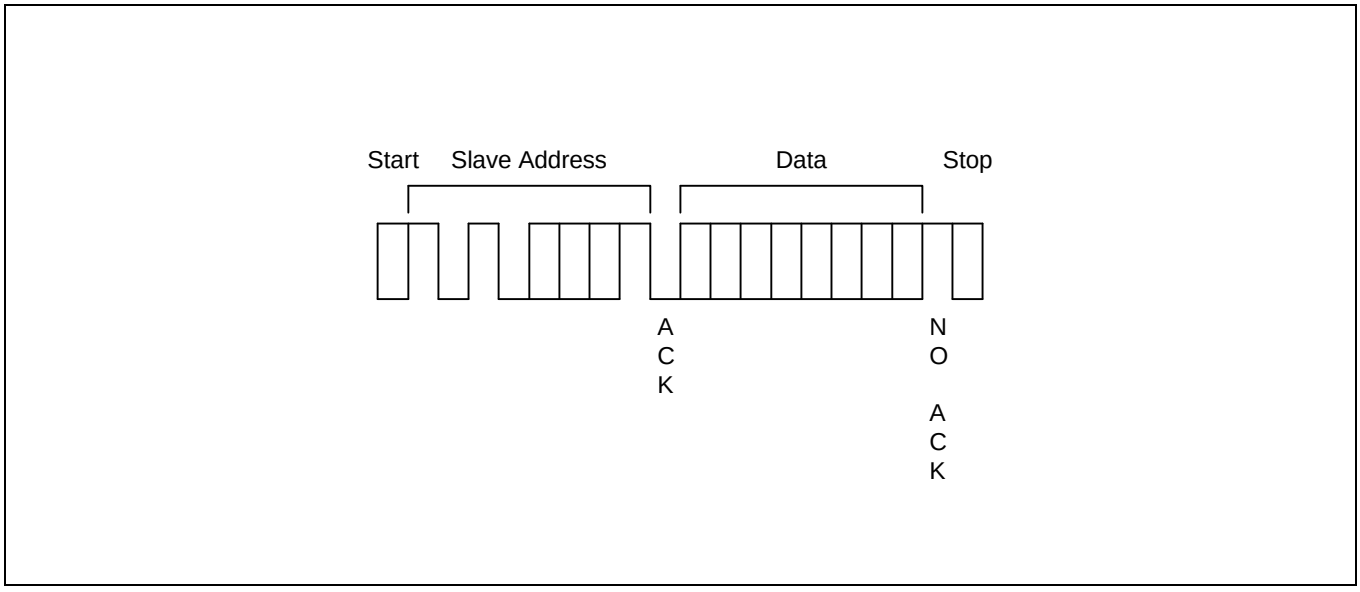


Figure 3-12. Current Address Byte Read Operation

RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. This operation is performed in the following steps:

1. The master first issues a Start condition, the slave address, and the word address to be read. (This step sets the internal word address pointer of the KS24C011/021/041/081 to the desired address.)
2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to "1".
3. The KS24C011/021/041/081 then sends an ACK and the 8-bit data stored at the desired address.
4. At this point, the master does not acknowledge the transmission, but generates a stop condition instead.
5. In response, the KS24C011/021/041/081 stops transmitting data and reverts to its stand-by mode (see Figure 3-13).

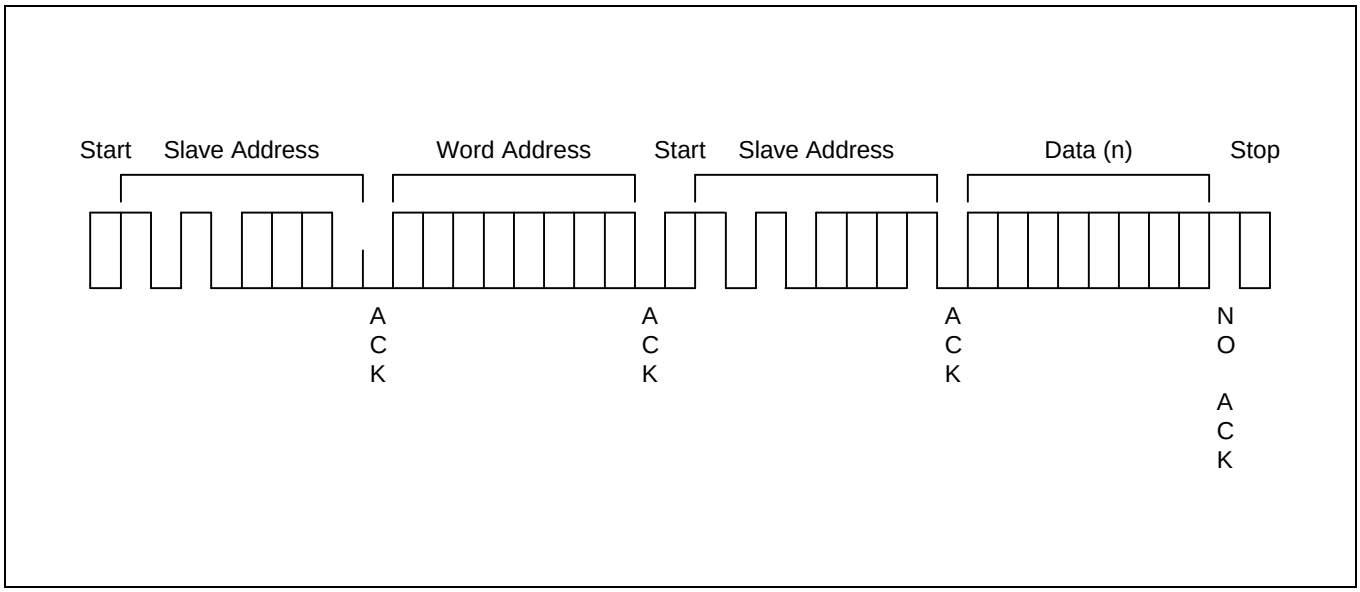


Figure 3-13. Random Address Byte Read Operation

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: as a series of current address reads or as random address reads. The first data is sent in the same way as the previous read mode used on the bus. The next time, however, the master responds with an ACK, indicating that it requires additional data.
The KS24C011/021/041/081 continues to output data for each ACK it receives. To stop the sequential read operation, the master does not respond with an ACK, but instead issues a Stop condition.

Using this method, data is output sequentially with the data from address "n" followed by the data from "n+1". The word address pointer for read operations increments all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer "rolls over" and the KS24C011/021/041/081 continues to transmit data for each ACK it receives from the master (see Figure 3-14).

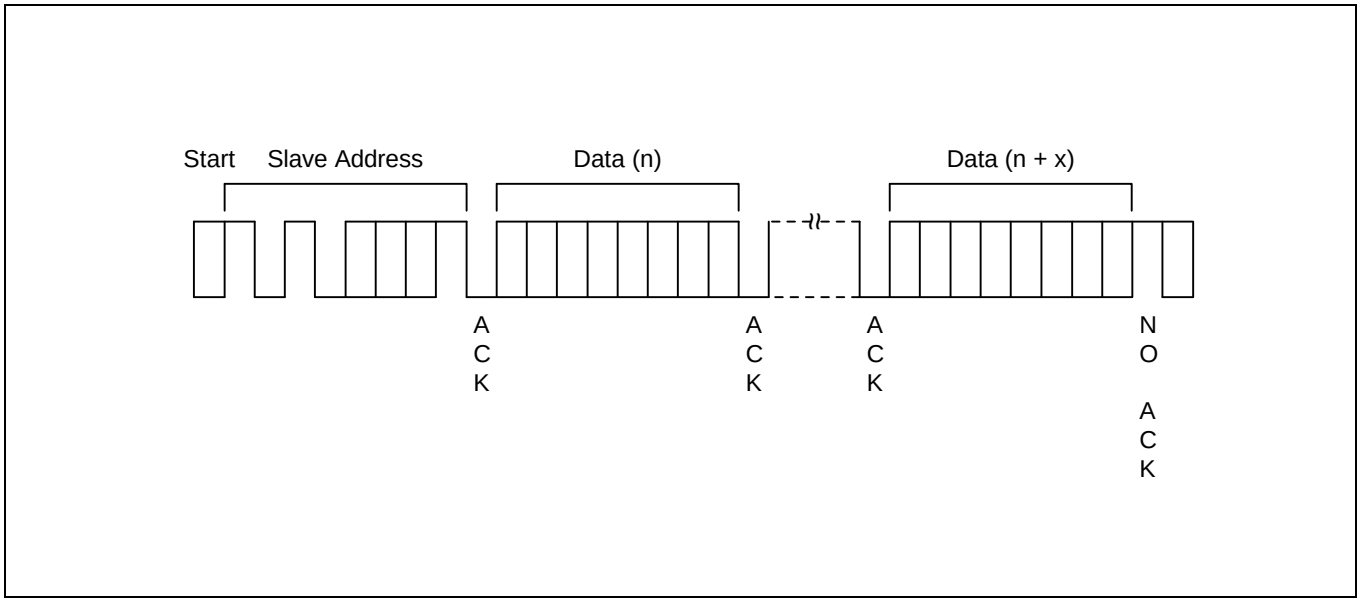


Figure 3-14. Sequential Read Operation

ELECTRICAL DATA

Table 3-3. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{CC}	–	– 0.3 to + 7.0	V
Input voltage	V_{IN}	–	– 0.3 to + 7.0	V
Output voltage	V_O	–	– 0.3 to + 7.0	V
Operating temperature	T_A	–	– 40 to + 85	°C
Storage temperature	T_{STG}	–	– 65 to + 150	°C
Electrostatic discharge	V_{ESD}	HBM	3000	V
		MM	300	

Table 3-4. D.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 2.2 V to 5.5 V when reading, 2.5 V to 5.5 V when writing)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input low voltage	V_{IL}	SCL, SDA, A0, A1, A2	–	–	0.3 V_{CC}	V
Input high voltage	V_{IH}		0.7 V_{CC}	–	–	V
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}	–	–	10	µA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}	–	–	10	µA
Output low voltage	V_{OL}	I_{OL} = 3 mA, V_{CC} = 2.5 V	–	–	0.4	V
Supply current	I_{CC1} (write)	V_{CC} = 5.5 V, 400 kHz	–	–	3	mA
	I_{CC2} (write)	V_{CC} = 3.3 V, 100 kHz	–	–	1.5	
	I_{CC3} (read)	V_{CC} = 5.5 V, 400 kHz	–	–	0.2	
	I_{CC4} (read)	V_{CC} = 3.3 V, 100 kHz	–	–	0.1	
Stand-by current	I_{CC5}	V_{CC} = SDA = SCL = 5.5 V, all other inputs = 0 V	–	–	10	µA
	I_{CC6}	V_{CC} = SDA = SCL = 3.3 V, all other inputs = 0 V	–	–	5	

Table 3-4. D.C. Electrical Characteristics (Continued)

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 2.2 V to 5.5 V when reading, 2.5 V to 5.5 V when writing)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	25 °C, 1MHz, V_{CC} = 5 V, V_{IN} = 0 V, A0, A1, A2, SCL and WP pin	–	–	10	pF
Input/output capacitance	$C_{I/O}$	25 °C, 1MHz, V_{CC} = 5 V, $V_{I/O}$ = 0 V, SDA pin	–	–	10	

Table 3-5. A.C. Electrical Characteristics

(T_A = – 25°C to + 70°C (C), – 40°C to + 85°C (I), V_{CC} = 2.2 V to 5.5 V when reading, 2.5 V to 5.5 V when writing)

Parameter	Symbol	Conditions	V_{CC} = 2.2 to 5.5 V (Standard Mode)		V_{CC} = 4.5 to 5.5 V (Fast Mode)		Unit
			Min	Max	Min	Max	
External clock frequency	F_{CLK}	–	0	100	0	400	kHz
Clock high time	t_{HIGH}	–	4	–	0.6	–	µs
Clock low time	t_{LOW}	–	4.7	–	1.3	–	
Rising time	t_R	SDA, SCL	–	1	–	0.3	
Falling time	t_F	SDA, SCL	–	0.3	–	0.3	
Start condition hold time	$t_{HD:STA}$	–	4	–	0.6	–	
Start condition setup time	$t_{SU:STA}$	–	4.7	–	0.6	–	
Data input hold time	$t_{HD:DAT}$	–	0	–	0	–	
Data input setup time	$t_{SU:DAT}$	–	0.25	–	0.1	–	
Stop condition setup time	$t_{SU:STO}$	–	4	–	0.6	–	
Bus free time	t_{BUF}	Before new transmission	4.7	–	1.3	–	
Data output valid from clock low (note)	t_{AA}	–	0.3	3.5	–	0.9	
Noise spike width	t_{SP}	–	–	100	–	50	ns
Write cycle time	t_{WR}	–	–	10	–	10	ms

NOTE: When acting as a transmitter, the KS24C011/021/041/081 must provide an internal minimum delay time to bridge the undefined period (minimum 300 ns) of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.

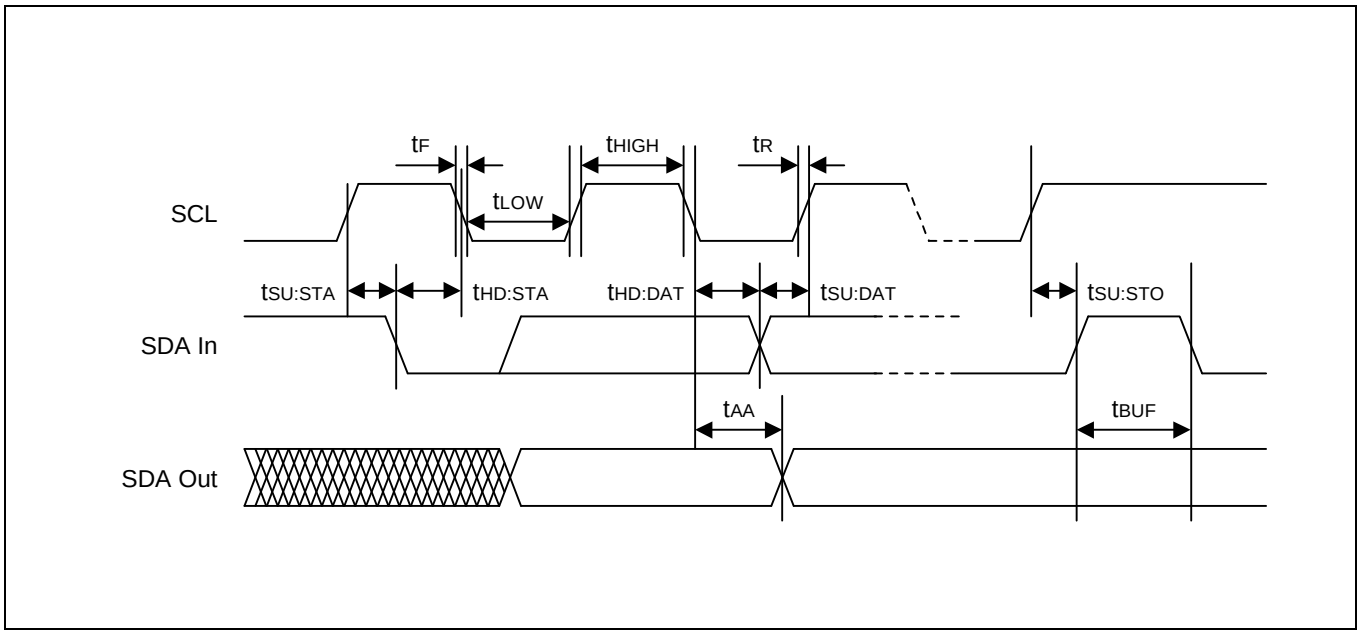


Figure 3-16. Timing Diagram for Bus Operations

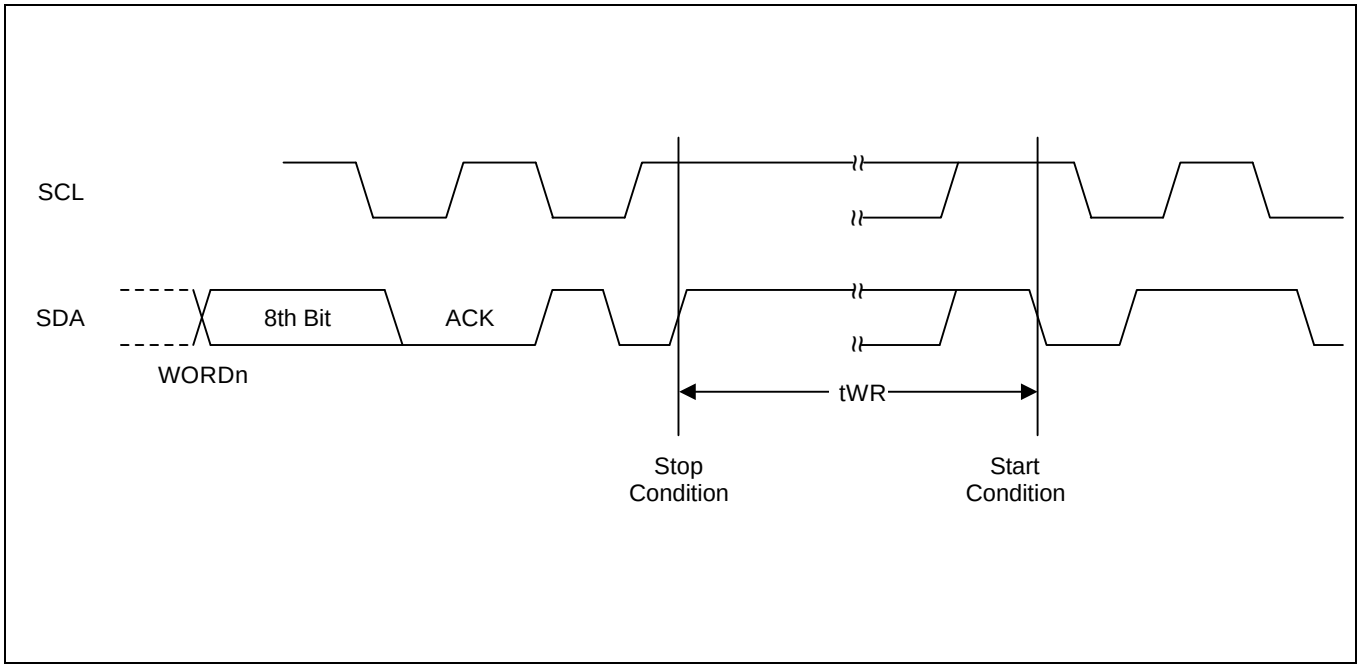


Figure 3-17. Write Cycle Timing Diagram

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

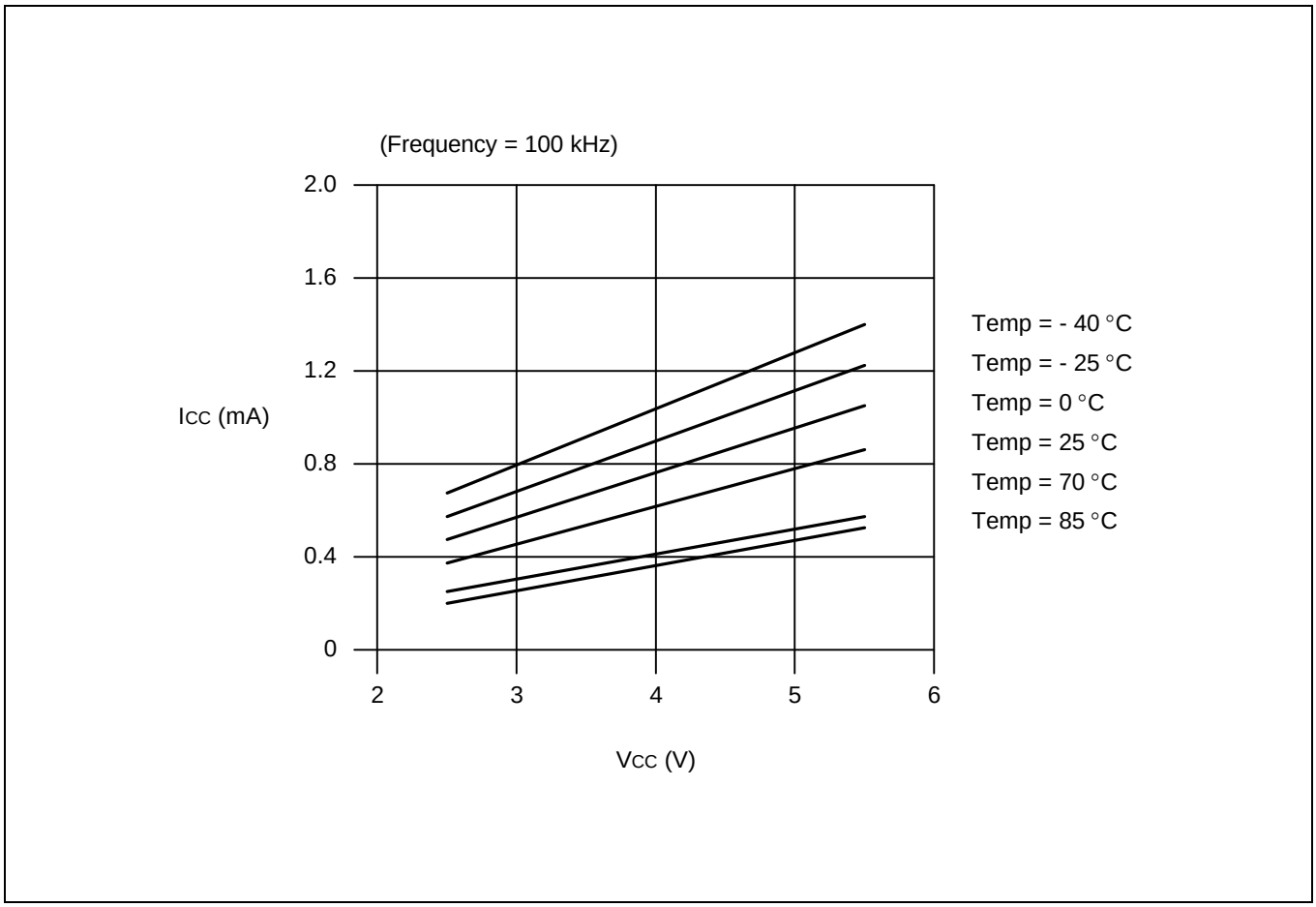


Figure 3-18. I_{CC} (Write Current) vs. V_{CC}

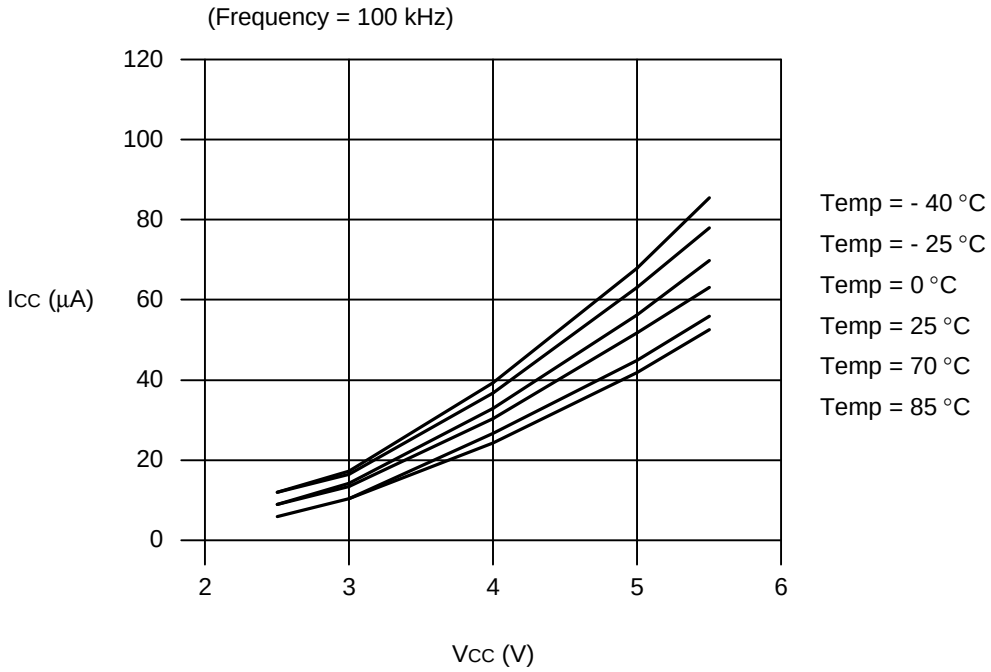


Figure 3-19. I_{CC} (Read Current) vs. V_{CC}

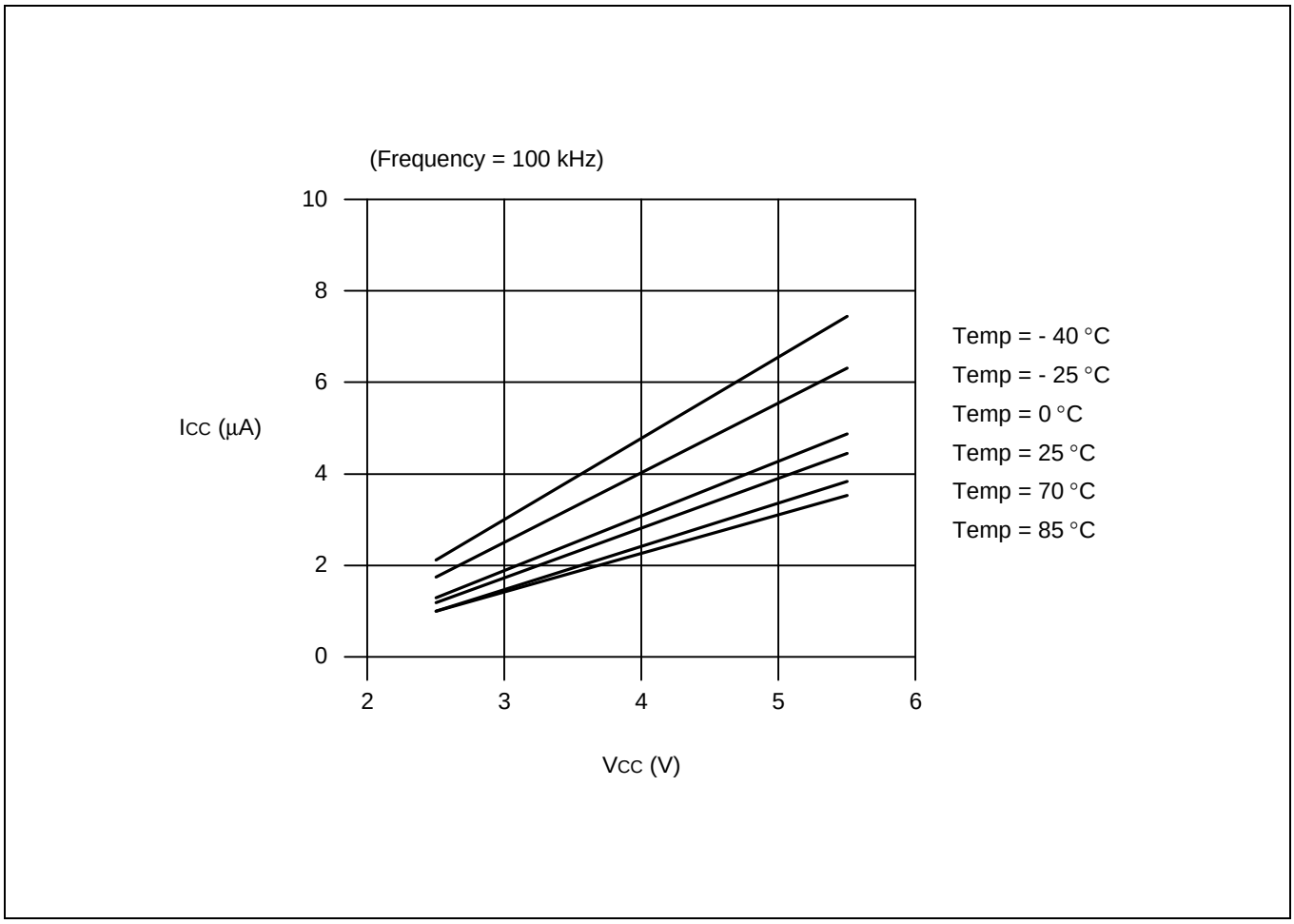


Figure 3-20. I_{CC} (Stand-by Current) vs. V_{CC}

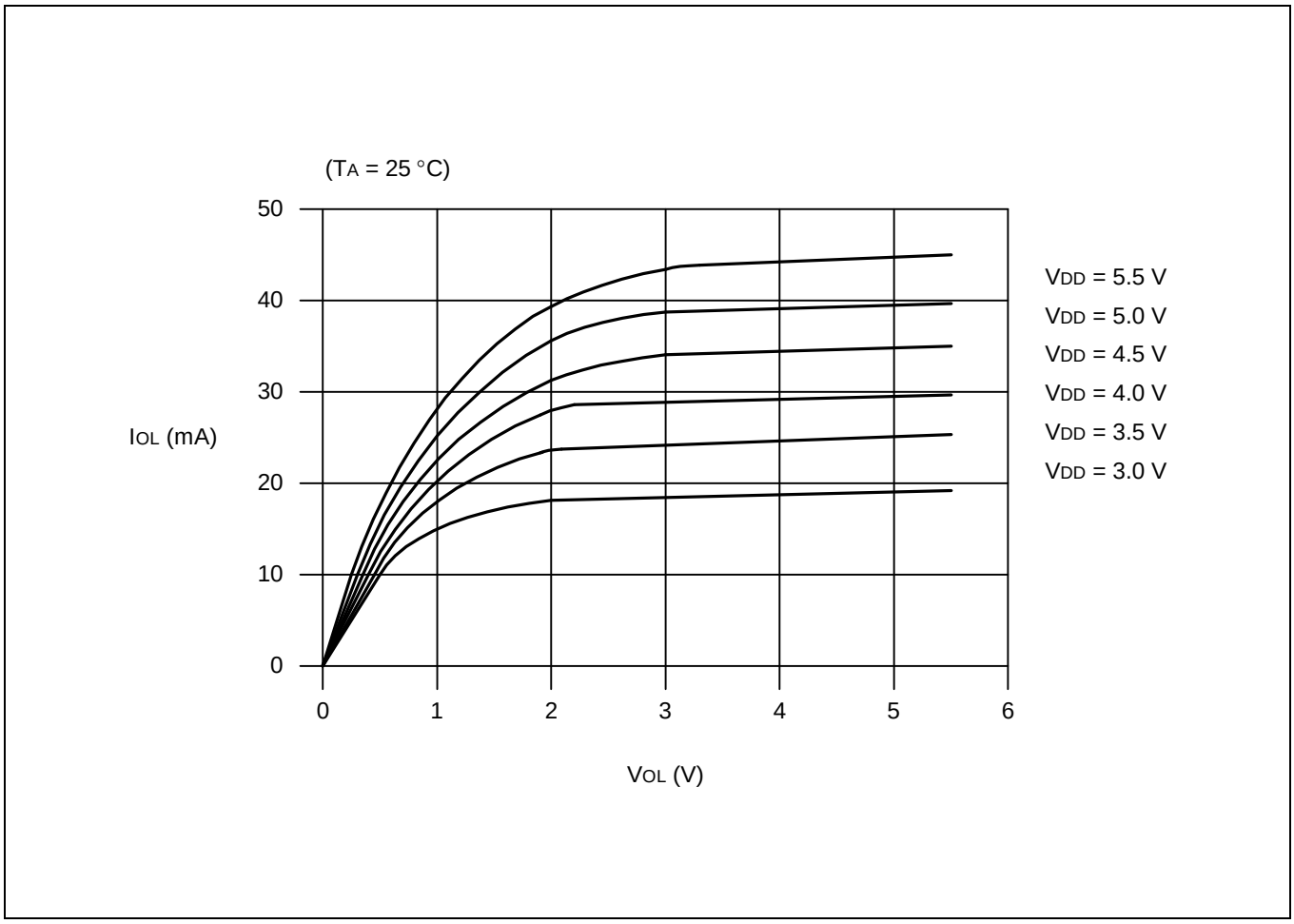


Figure 3-21. I_{OL} (Output Low Voltage) vs. V_{OL}