AOZ1342

Dual Channel USB Switch

General Description

The AOZ1342 power-distribution switches is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

The AOZ1342 offers 1.5 A of maximum continuous current.

The AOZ1342 is available in an Exposed Pad SO-8 package and is rated over a -40 °C to +85 °C ambient temperature range.

Features

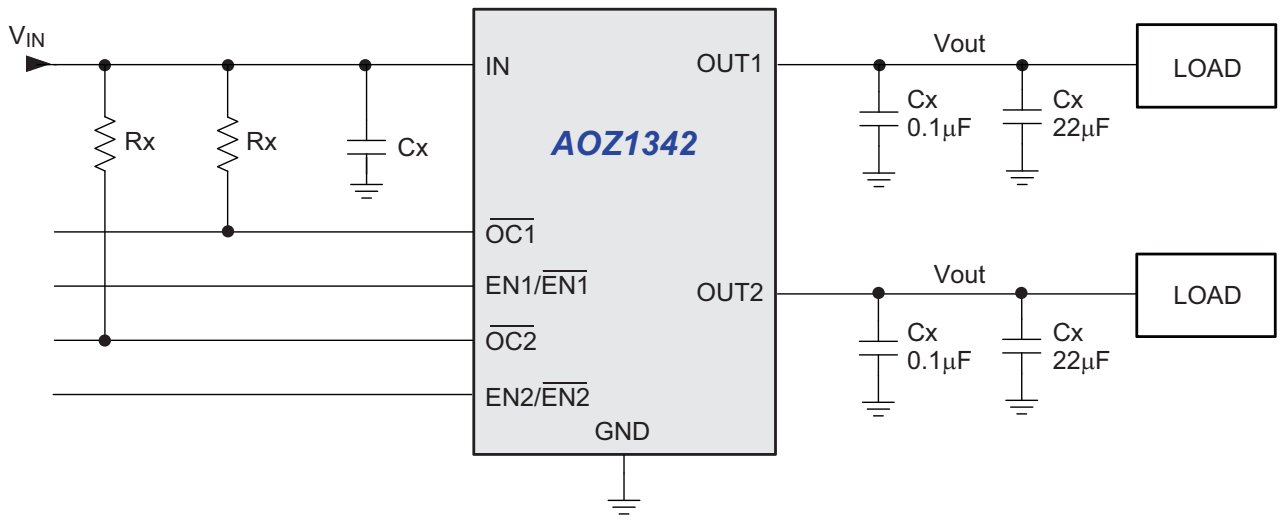
- Typical 70 mΩ (NFET)
- 1.5 A maximum continuous current
- Two enable options: EN or $\overline{EN}$
- Vin range: 2.7 V to 5.5 V
- Open Drain Fault Flag
- Fault Flag deglitched (blanking time)
- Thermal shutdown
- Reverse current blocking
- Exposed pad SO-8 package

Applications

- Notebook Computers
- Desktop Computers

Green Product

Typical Application



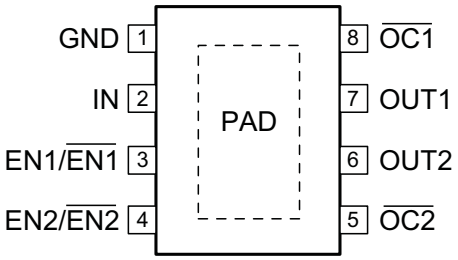
Ordering Information

Part Number	Maximum Continuous Current		Typical Short-circuit Current Limit		Enable Setting	Package	Output Discharge	Environmental
	Channel 1	Channel 2	Channel 1	Channel 2				
AOZ1341AI	1 A	1A	1.5 A	1.5 A	Active Low	SO-8	No	Green Product RoHS Compliant
AOZ1341EI						EPAD MSOP-8		
AOZ1341AI-1					Active High	SO-8		
AOZ1341EI-1						EPAD MSOP-8		
AOZ1342PI	1.5 A	1.5A	2 A	2 A	Active Low	EPAD SO-8		
AOZ1342PI-1					Active High	EPAD SO-8		
AOZ1343AI*	1.5 A	0.5A	2 A	0.75 A	Active Low	SO-8		
AOZ1343EI*						EPAD MSOP-8		
AOZ1343AI-1*					Active High	SO-8		
AOZ1343EI-1*						EPAD MSOP-8		
AOZ1312AI-1	1.5 A	None	2 A	None	Active High	SO-8		
AOZ1312EI-1						EPAD MSOP-8		
AOZ1310CI-1	0.5 A	None	0.75 A	None	Active High	SOT23-5		

*Contact factory for availability

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



Exposed Pad SO-8
(Top View)

Pin Description

Pin Name	Pin Number	Pin Function
GND	1	Ground
IN	2	Input voltage
EN1/$\overline{EN1}$	3	Enable input, logic high/logic low turns on power switch IN-OUT1
EN2/$\overline{EN2}$	4	Enable input, logic high/logic low turns on power switch IN-OUT2
$\overline{OC2}$	5	Overcurrent, open-drain output, active low, IN-OUT1
OUT2	6	Power-switch output, IN-OUT1
OUT1	7	Power-switch output, IN-OUT2
$\overline{OC1}$	8	Overcurrent, open-drain output, active low, IN-OUT2

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Input Voltage (V_{IN})	6 V
Enable Voltage (V_{EN})	6 V
Storage Temperature (T_S)	-55 °C to +150 °C
Maximum Continuous Current	1.5 A
ESD Rating(1)	2 kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model is a 100 pF capacitor discharging through a 1.5 kΩ resistor.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Recommended Operating Conditions.

Parameter	Rating
Input Voltage (V_{IN})	+2.7 V to +5.5 V
Junction Temperature (T_J)	-40 °C to +125 °C
Package Thermal Resistance Exposed Pad SO-8 (Θ_{JA})	45 °C/W

Electrical Characteristics

T_A = 25 °C, V_{IN} = V_{EN} = 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
POWER SWITCH							
$R_{DS(ON)}$	Switch On-Resistance	V_{IN} = 2.7 V to 5 V, I_O = 0.5 A/1.5 A			70	135	mΩ
t_r	Rise Time, Output	V_{IN} = 5.5 V	C_L = 1 µF, R_L = 5 Ω		0.6	1.5	ms
		V_{IN} = 2.7 V			0.4	1	
t_f	Fall time, Output	V_{IN} = 5.5 V		0.05		0.5	ms
		V_{IN} = 2.7 V		0.05		0.5	
	FET Leakage Current	Out connect to ground, 2.7 V ≤ V_{IN} ≤ 5.5 V, $V_{(\overline{ENx})}$ = V_{IN} or $V_{(ENx)}$ = 0 V	-40 °C ≤ T_J ≤ 125 °C(2)		1		µA
ENABLE INPUT $\overline{EN}$ OR EN							
V_{IH}	High-level Input Voltage	2.7 V ≤ V_{IN} ≤ 5.5 V		2.0			V
V_{IL}	Low-level Input Voltage	2.7 V ≤ V_{IN} ≤ 5.5 V				0.8	V
I_I	Input Current			-0.5		0.5	µA
t_{on}	Turn-on Time	C_L = 100 µF, R_L = 5 Ω				3	ms
t_{off}	Turn-off Time	C_L = 100 µF, R_L = 5 Ω				10	
CURRENT LIMIT							
I_{OS}	Short-circuit Output Current (per Channel)	$V_{(IN)}$ = 2.7 V to 5.5 V, OUT connected to GND, device enable into short-circuit, Channel 1 or 2		1.6	2.0	2.4	A
I_{OC_TRIP}	Overcurrent Trip Threshold (per Channel)	$V_{(IN)}$ = 5 V, current ramp (≤ 100 A/s) on OUT, Channel 1 or 2		1.6	2.2	2.5	A
SUPPLY CURRENT							
	Supply Current, Low-level Output	No load on OUT, 2.7 V ≤ V_{IN} ≤ 5.5 V, $V_{(\overline{ENx})}$ = V_{IN} or $V_{(ENx)}$ = 0 V	T_J = 25°C		0.5	1	µA
			-40 °C ≤ T_J ≤ 125 °C(2)		0.5	5	
	Supply current, High-level Output	No load on OUT, $V_{(\overline{ENx})}$ = 0 V or $V_{(ENx)}$ = 5.5 V	T_J = 25 °C		65	81	µA
			-40 °C ≤ T_J ≤ 125 °C(2)		65	90	
	Reverse Leakage Current	$V_{(OUTx)}$ = 5.5 V, IN = ground			0.2		µA

Electrical Characteristics (Continued)

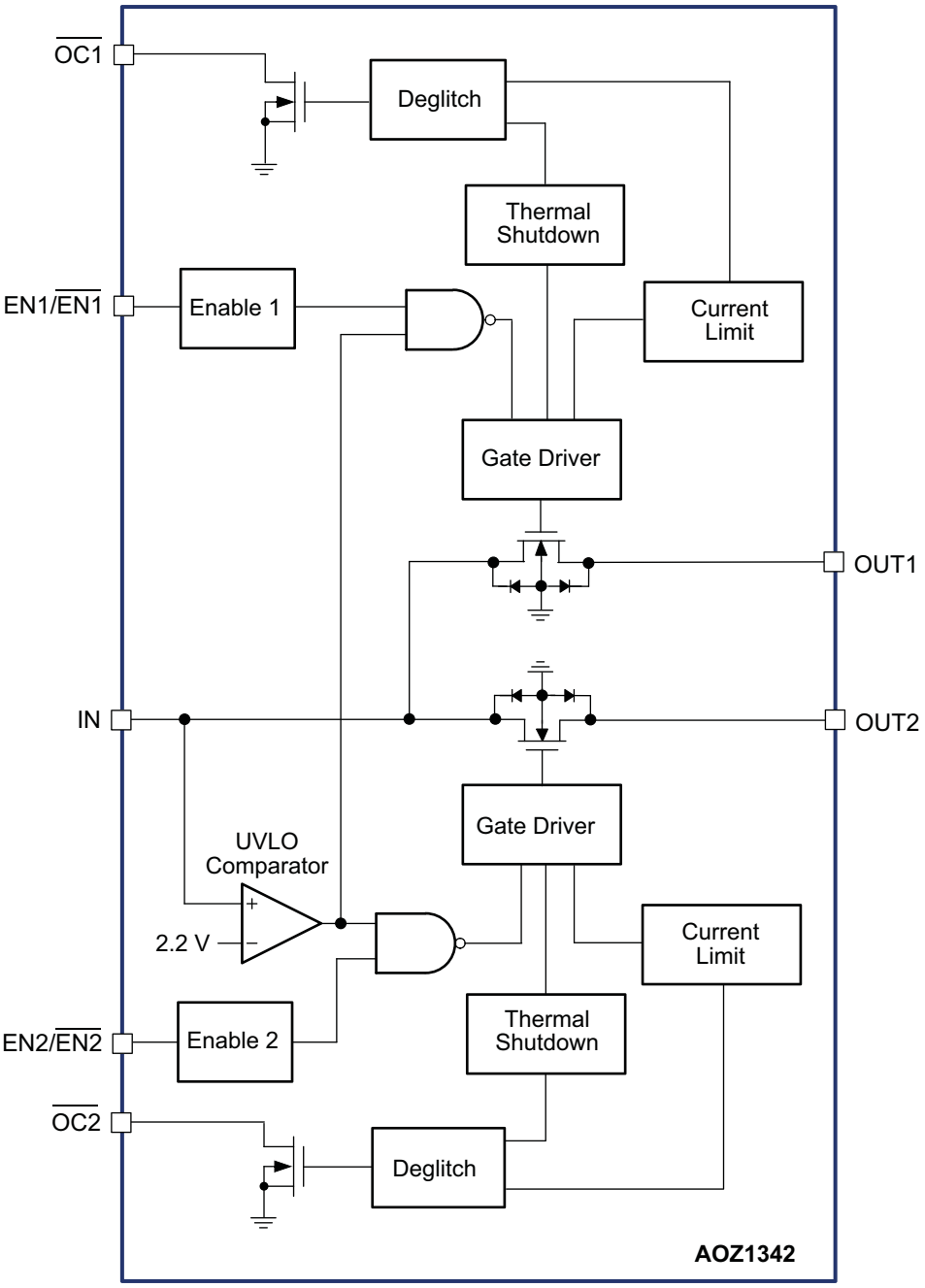
T_A = 25 °C, V_{IN} = V_{EN} = 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
UNDERVOLTAGE LOCKOUT						
	Low-level voltage, IN		2.0		2.5	V
	Hysteresis, IN			200		mV
OVERCURRENT $\overline{OC1}$ AND $\overline{OC2}$						
	Output Low Voltage $V_{OL(OCx)}$	$I_{O(OCx)}$ = 5 mA			0.4	V
	Off-state Current	$V_{O(OCx)}$ = 5 V or 3.3 V			1	µA
	OC_L Deglitch	OCx assertion or deassertion	4	8	15	ms
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		135			°C
	Recovery from Thermal Shutdown		105			°C
	Hysteresis			30		°C

Note:

2. Parameters are guaranteed by design only and not production tested.

Functional Block Diagram



Functional Characteristics

Figure 1. Turn-On Delay and Rise Time with 1µF Load (Active High)

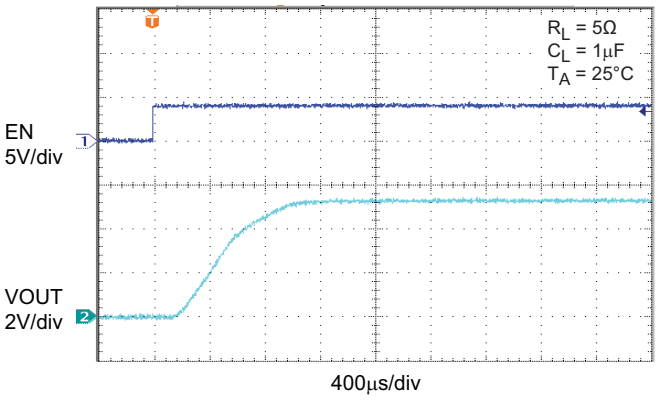


Figure 2. Turn-Off Delay and Fall Time with 1µF Load (Active High)

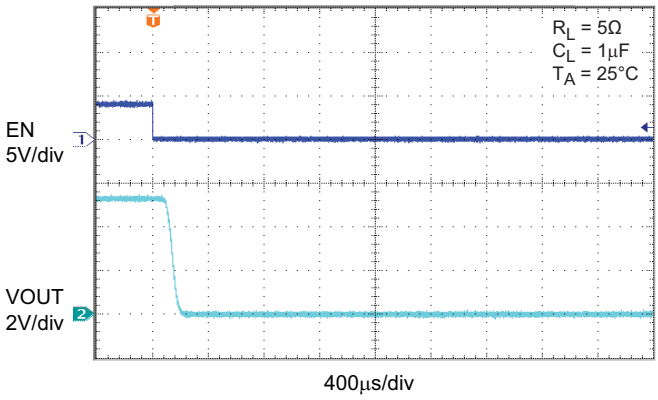


Figure 3. Turn-On Delay and Rise Time with 100µF Load (Active High)

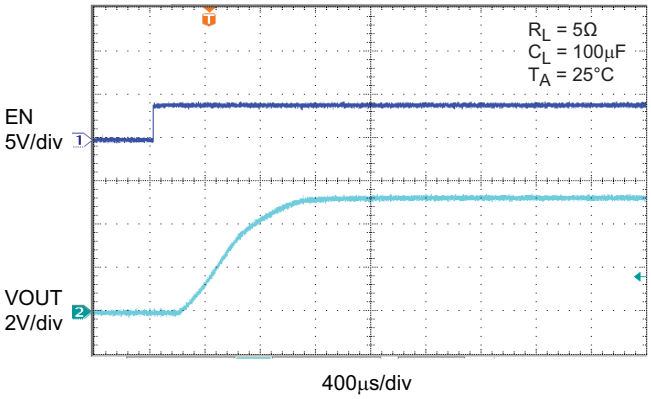


Figure 4. Turn-Off Delay and Fall Time with 100µF Load (Active High)

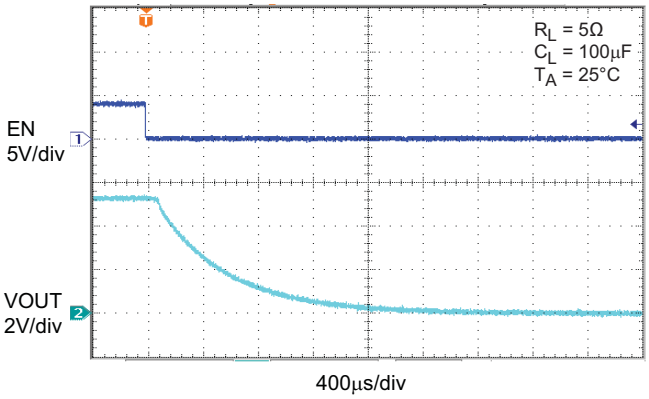


Figure 5. Short-circuit Current, Device Enable to Short (Active High)

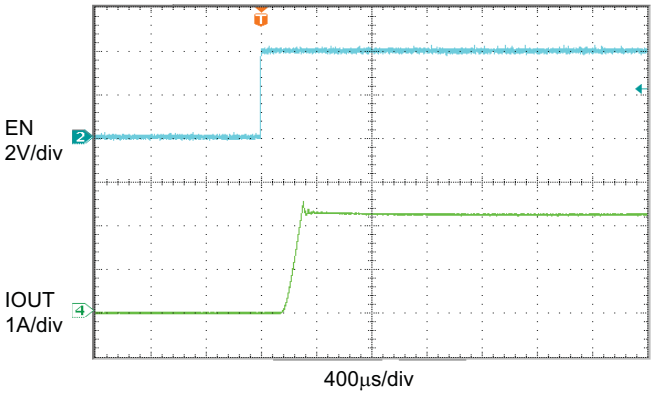
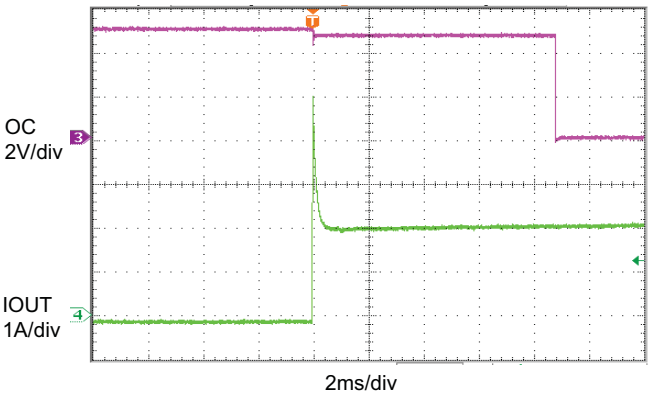


Figure 6. 0.6Ω Load Connected to Enable to Device (Active High)



Typical Characteristics

Figure 7. Supply Current, Output Enabled vs. Junction Temperature

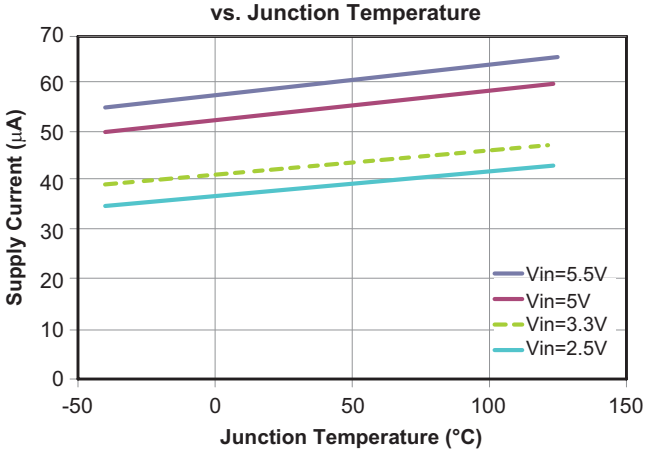


Figure 8. Supply Current, Output Disabled vs. Junction Temperature

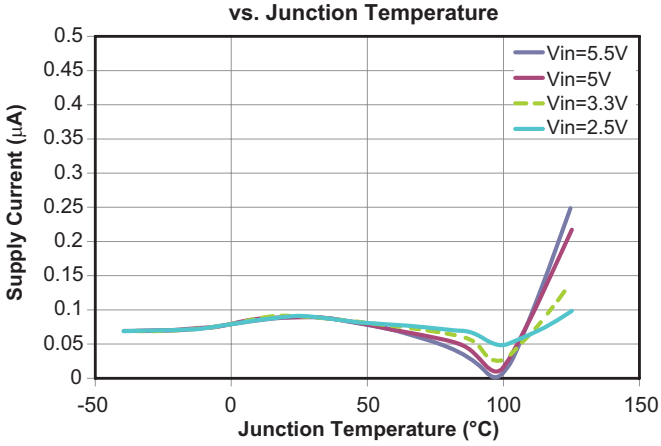


Figure 9. Rds(on) vs. Ambient Temperature

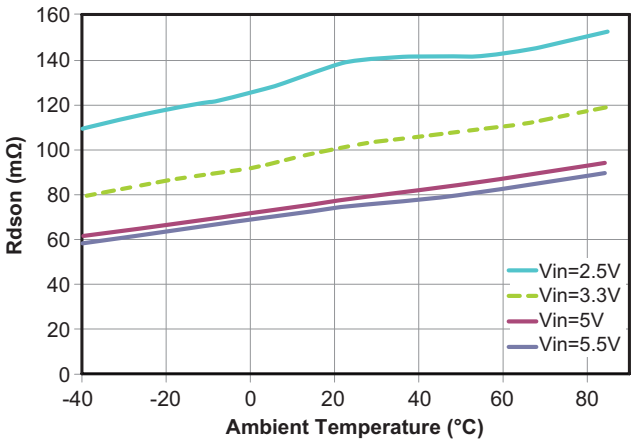
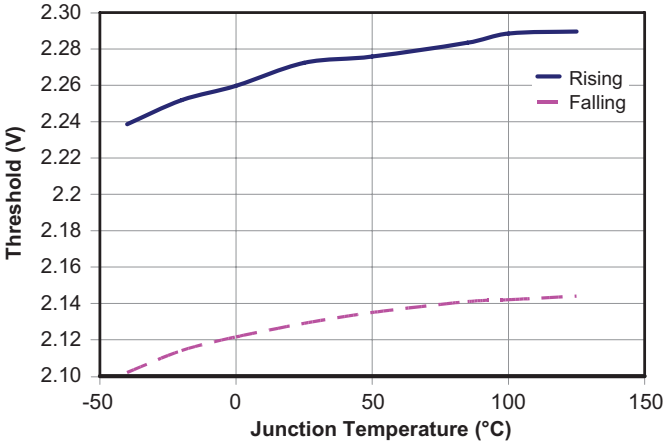


Figure 10. UVLO Threshold vs. Junction Temperature



Detailed Description

The AOZ1342 family of power-distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70 mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

Thermal Shut-down Protection

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OC) logic output low.

During current limit or short circuit conditions, the increasing power dissipation in the chip causes the die temperature to rise. When the die temperature reaches a certain level, the thermal shutdown circuitry will shutdown the device. The thermal shutdown will cycle repeatedly until the short circuit condition is resolved.

Applications Information

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on and to also limit input voltage drop. The input capacitor also prevents high-frequency noise on the power line from passing through the output of the power side. The choice of input capacitor is based on its ripple current and voltage ratings rather than its capacitor value. The input capacitor should be located as close as possible to the VIN pin. A 0.1 μF ceramic cap is recommended. However, a higher value capacitor will reduce the voltage drop at the input.

Output Capacitor Selection

The output capacitor acts in a similar way. A small 0.1 μF capacitor prevents high-frequency noise from going into the system. Also, the output capacitor has to supply enough current for the large load that it may encounter during system transients. This bulk capacitor must be large enough to supply a fast transient load in order to prevent the output from dropping.

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$P_D = R_{ON} \times (I_{OUT})^2$$

The worst case power dissipation occurs when the load current hits the current limit due to over-current or short circuit faults. The power dissipation under these conditions can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LIMIT}$$

Layout Guidelines

Good PCB layout is important for improving the thermal and overall performance of AOZ1342. To optimize the switch response time to output short-circuit conditions, keep all traces as short as possible to reduce the effect of unwanted parasitic inductance. Place the input and output bypass capacitors as close as possible to the IN and OUT pins. The input and output PCB traces should be as wide as possible for the given PCB space. Use a ground plane to enhance the power dissipation capability of the device.

USB Power Distribution Application

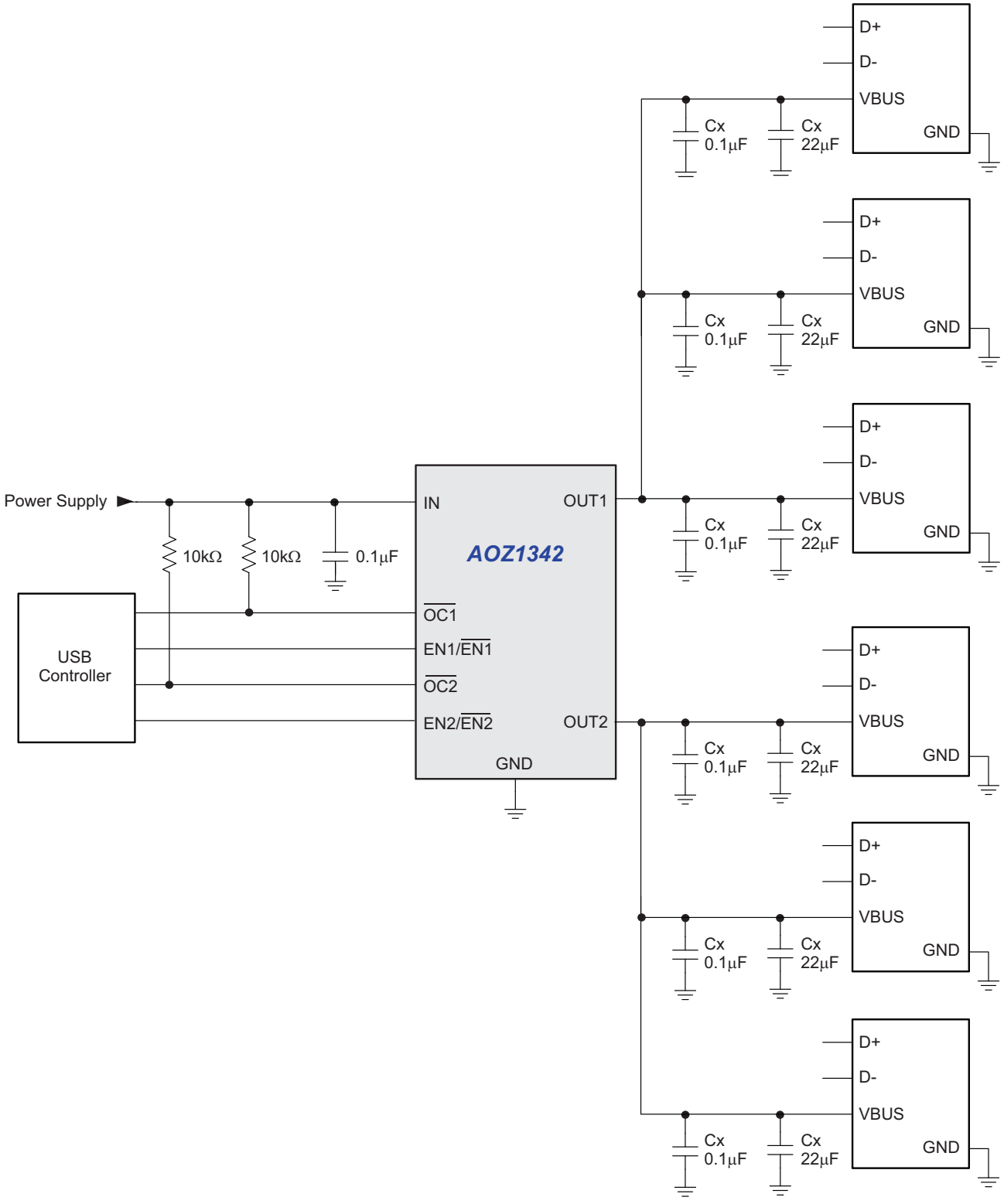
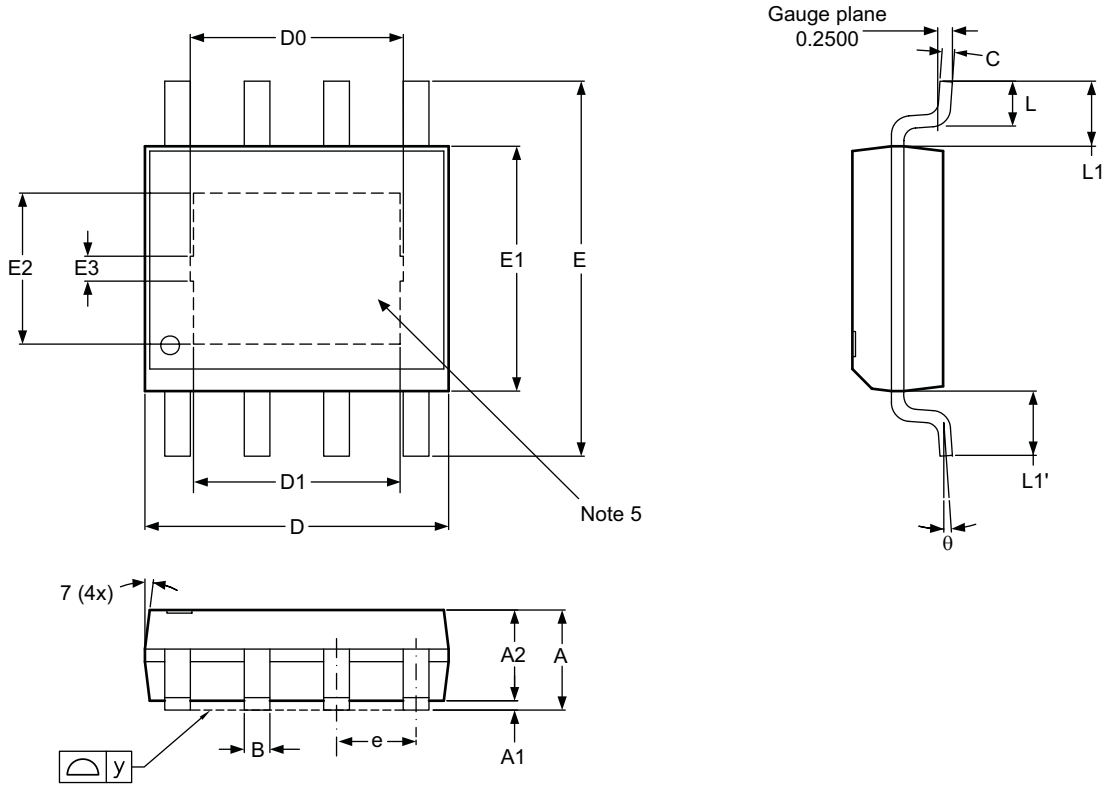
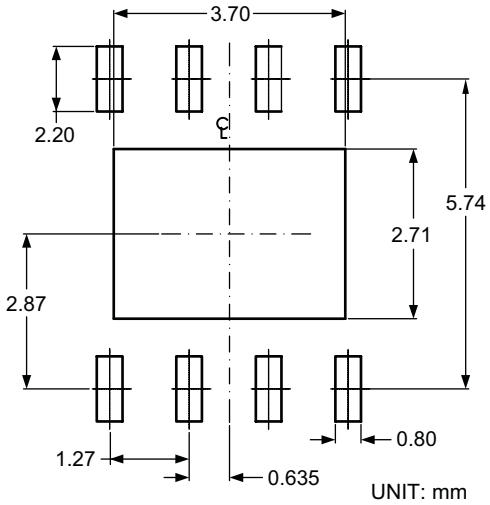


Figure 11. Typical Six-Port USB Host/Self-Powered Hub Applications Circuitry

Package Dimensions, Exposed Pad SO-8



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.40	1.55	1.70
A1	0.00	0.05	0.10
A2	1.40	1.50	1.60
B	0.31	0.406	0.51
C	0.17	—	0.25
D	4.80	4.96	5.00
D0	3.20	3.40	3.60
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
e	—	1.27	—
E1	3.80	3.90	4.00
E2	2.21	2.41	2.61
E3	0.40 REF		
L	0.40	0.95	1.27
y	—	—	0.10
θ	0°	3°	8°
| L1–L1' |	—	0.04	0.12
L1	1.04 REF		

Dimensions in inches

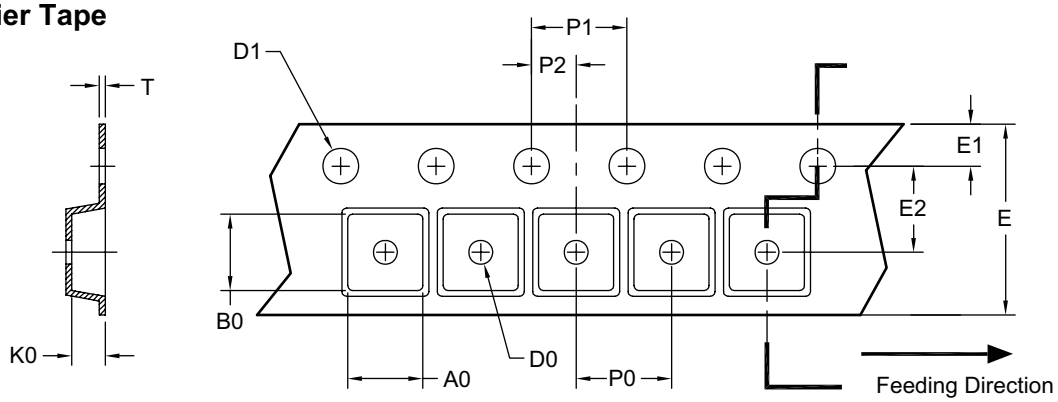
Symbols	Min.	Nom.	Max.
A	0.055	0.061	0.067
A1	0.000	0.002	0.004
A2	0.055	0.059	0.063
B	0.012	0.016	0.020
C	0.007	—	0.010
D	0.189	0.195	0.197
D0	0.126	0.134	0.142
D1	0.122	0.130	0.138
E	0.228	0.236	0.244
e	—	0.050	—
E1	0.150	0.153	0.157
E2	0.087	0.095	0.103
E3	0.016 REF		
L	0.016	0.037	0.050
y	—	—	0.004
θ	0°	3°	8°
| L1–L1' |	—	0.002	0.005
L1	0.041 REF		

Notes:

1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gauge plane.
3. Tolerance 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Followed from JEDEC MS-012

Tape and Reel Dimensions, Exposed Pad SO-8

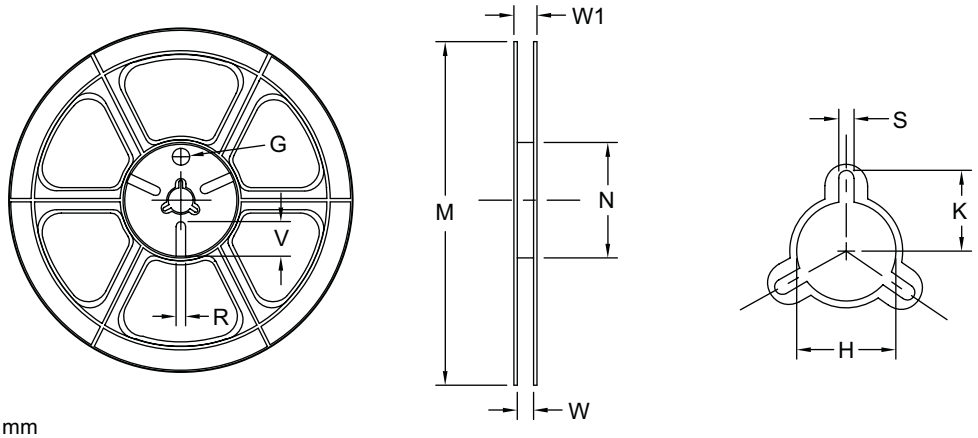
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

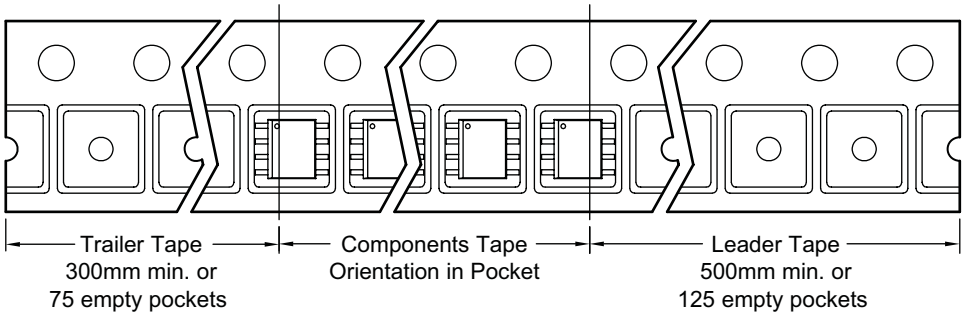
Reel



UNIT: mm

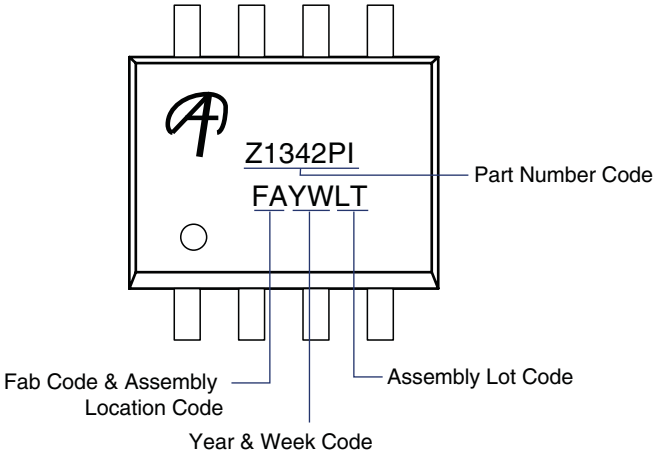
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation

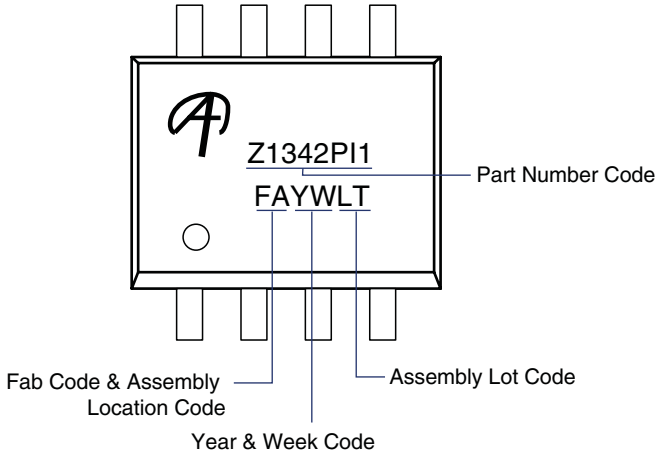


Part Marking

AOZ1342PI
(Exposed Pad SO-8)



AOZ1342PI-1
(Exposed Pad SO-8)



This datasheet contains preliminary data; supplementary data may be published at a later date.
Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.