

# S71WS-P based MCP Products

## 1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM



*Data Sheet (Advance Information)*

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## 1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash Memory with CellularRAM



*Data Sheet (Advance Information)*

### Features

- Power supply voltage of 1.7 to 1.95V
- Flash access time: 80 ns, 25 ns
- Flash burst frequencies: 66 MHz, 80 MHz, 108 MHz
- pSRAM Access time: 70 ns, 20 ns
- pSRAM burst frequency: 66 MHz, 80 MHz, 104 MHz
- Package:
  - 8.0 x 11.6 mm MCP
- Operating Temperature
  - -25°C to +85°C (wireless)

The S71WS series is a product line of stacked packages and consists of:

- One or two S29WS-P NOR flash memory die
- CellularRAM die

The products covered by this document are listed in the table below.

| Device    | CellularRAM Density (Mb) |             |
|-----------|--------------------------|-------------|
|           | 64 Mb                    | 128 Mb      |
| S29WS512P | S71WS512PC0              | S71WS512PD0 |

**Note:**

For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

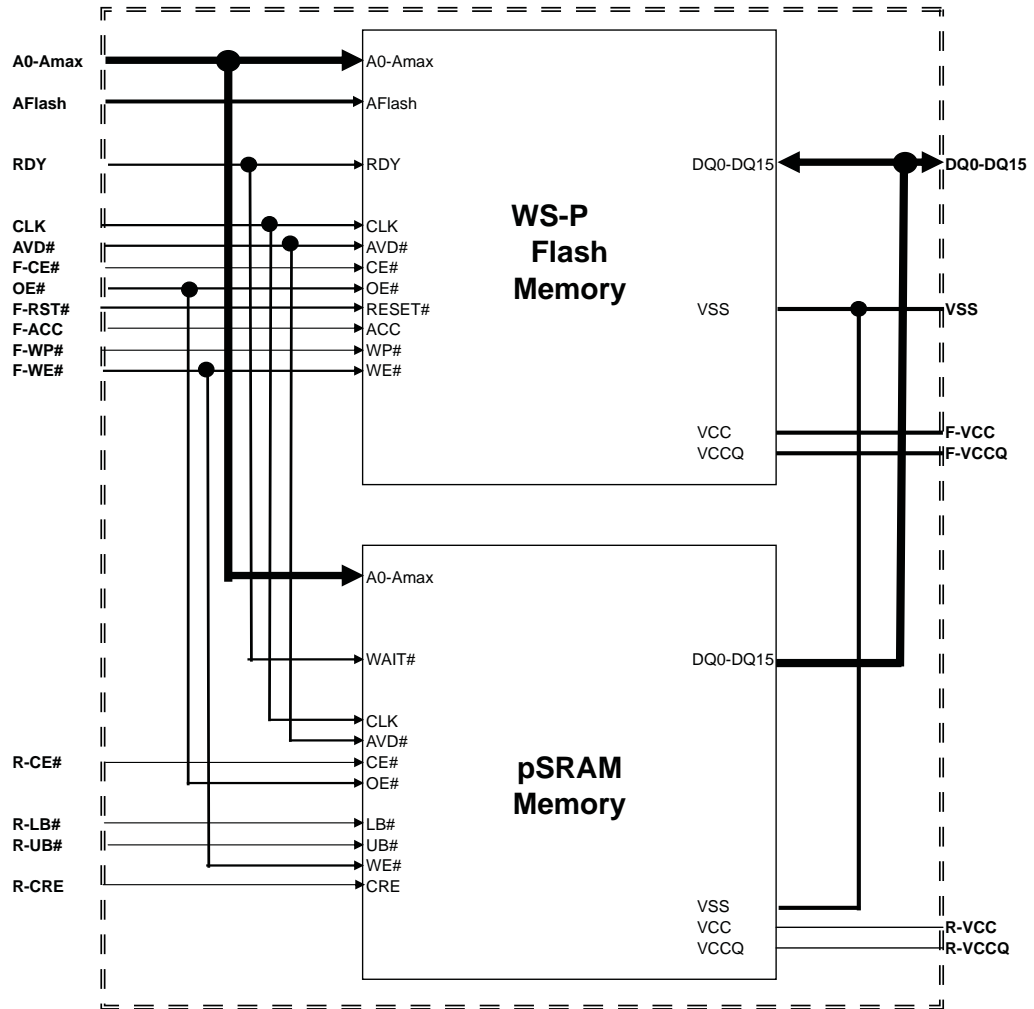
For detailed specifications, please refer to the individual data sheets.

| Document                 | Publication Identification Number (PID) |
|--------------------------|---|
| S29WS-P                  | S29WS-P_00                              |
| 128 M CellularRAM Type 2 | Cellram_04                              |
| 64 M CellularRAM Type 2  | Cellram_07                              |

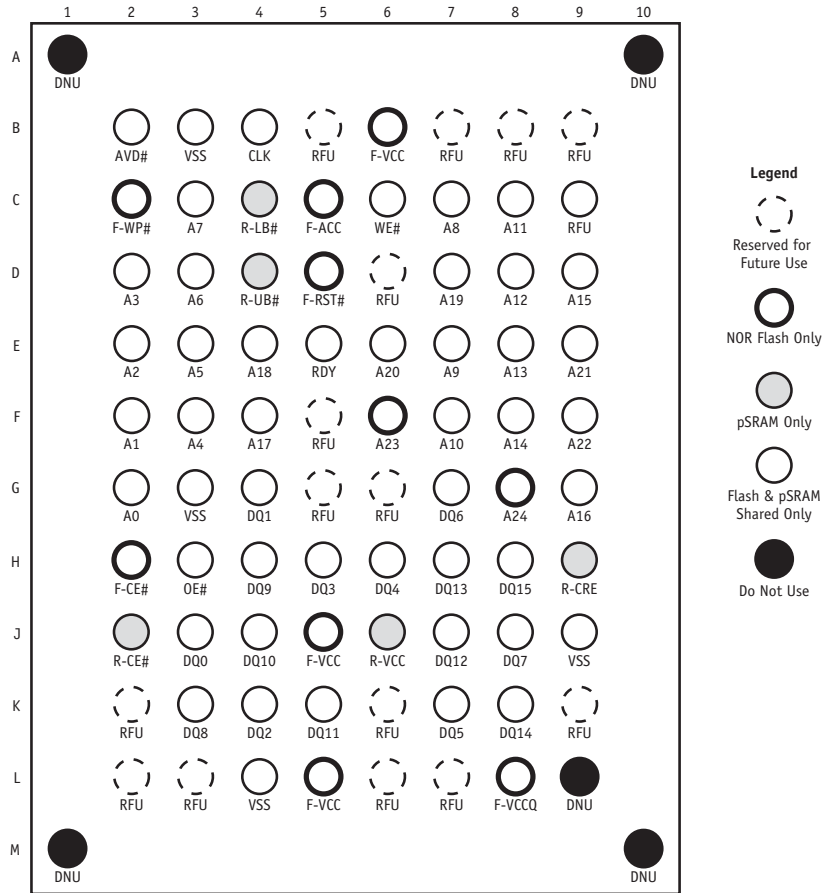
## 1. Product Selector Guide

| Device         | Model Number | Flash Density (Mb) | CellularRAM Density (Mb) | Flash Speed (MHz) | CellularRAM Speed (MHz) | CellularRAM Supplier | Package            |
|----------------|--------------|--------------------|--------------------------|-------------------|-------------------------|----------------------|--------------------|
| S71WS512PD0HF3 | HR           | 512                | 128                      | 80                | 104                     | Type 2               | MCP<br>8 x 11.6 mm |
| S71WS512PC0HF3 | SV           |                    | 64                       | 66                |                         |                      |                    |
| S71WS512PD0HF3 | HL           |                    | 128                      | 108               | 104                     |                      |                    |

## 2. MCP Block Diagram



### 3. Connection Diagrams



| MCP         | Flash-only Addresses | Shared Addresses |
|-------------|----------------------|------------------|
| S71WS512PD0 | A24-A23              | A22-A0           |
| S71WS512PC0 | A24-A22              | A21-A0           |

#### 3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

#### 3.2 Look-ahead Ballout for Future Designs

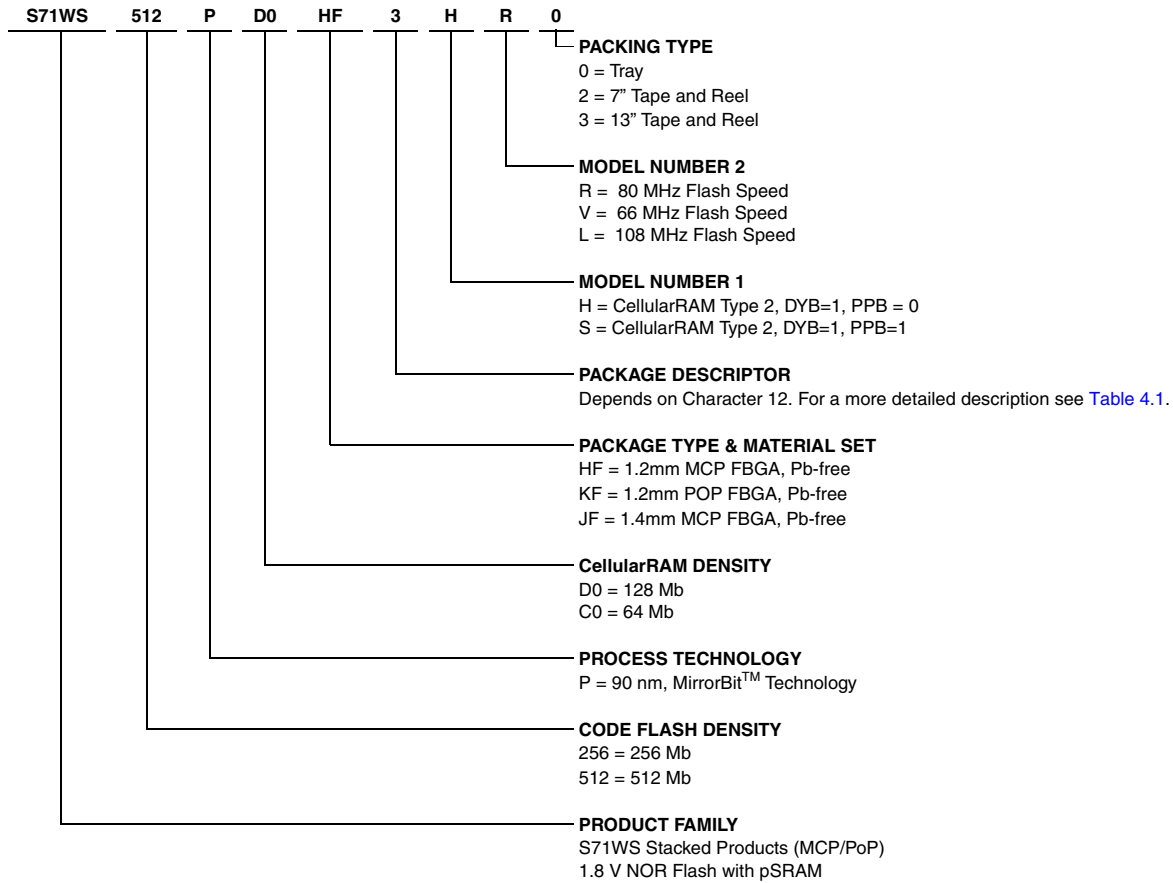
Please refer to the Design-in Scalable Wireless Solutions with Spansion Products application note (publication number: Design\_Scalable\_Wireless\_A0\_E). Contact your local Spansion sales representative for more details.

### 3.3 NOR Flash and pSRAM Input/Output Descriptions

|                    |   |   |
|--------------------|---|---|
| Amax-A0            | = | NOR Flash Address inputs  |
| DQ15-DQ0           | = | Flash Data input/output, shared between NOR and ORNAND Flash. DQ0-DQ7 shared for x8 ORNAND  |
| F-CE#              | = | NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.  |
| OE#                | = | Output Enable input. Asynchronous relative to CLK for Burst mode.   |
| WE#                | = | Write Enable input.   |
| F-V <sub>CC</sub>  | = | NOR Flash device power supply (1.7 V - 1.95V).  |
| F-V <sub>CCQ</sub> | = | Input/Output Buffer power supply.   |
| V <sub>SS</sub>    | = | Ground  |
| RFU                | = | Reserved for Future Use   |
| RDY                | = | Flash ready output. Indicates the status of the Burst read. VOL = data valid. The Flash RDY pin is shared with the WAIT pin of the pSRAM.   |
| CLK                | = | NOR Flash Clock, shared with CLK of burst-mode pSRAM.. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access. |
| AVD#               | = | NOR Flash Address Valid input. Shared with AVD# of burst-mode pSRAM. Indicates to device that the valid address is present on the address inputs.<br>VIL = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK.<br>VIH= device ignores address inputs             |
| F-RST#             | = | NOR Flash hardware reset input. VIL= device resets and returns to reading array data  |
| F-WP#              | = | NOR Flash hardware write protect input. VIL = disables program and erase functions in the four outermost sectors.   |
| F-ACC              | = | NOR Flash accelerated input. At VHH, accelerates programming; automatically places device in unlock bypass mode. At VIL, disables all program and erase functions. Should be at VIH for all other conditions.   |
| R-CE#              | = | Chip-enable input for pSRAM   |
| R-CRE              | = | Control Register Enable (pSRAM). For CellularRAM only.  |
| R-VCC              | = | pSRAM Power Supply  |
| R-UB#              | = | Upper Byte Control (pSRAM)  |
| R-LB#              | = | Lower Byte Control (pSRAM)  |
| DNU                | = | Do Not Use  |

## 4. Ordering Information

The order number is formed by a valid combinations of the following:



**Table 4.1** Character Position Descriptions (Sheet 1 of 2)

| Character 12 | Character 14 | Character 14 Description |                    |               |
|--------------|--------------|--------------------------|--------------------|---------------|
|              |              | Package Area             | Package Ball Count | Raw Ball Size |
| H, J, or G   | 0            | 7x9 mm                   | 56                 | 0.35 mm       |
|              | 1            | 7x9 mm                   | 80                 |               |
|              | 2            | 8x11.6 mm                | 64                 |               |
|              | 3            | 8x11.6 mm                | 84                 |               |
|              | 4            | 9x12 mm                  | 84                 |               |
|              | 5            | 9x12 mm                  | 115                |               |
|              | 6            | 9x12 mm                  | 137                |               |
|              | 7            | 11x13 mm                 | 84                 |               |
|              | 8            | 11x13 mm                 | 115                |               |
|              | 9            | 11x13 mm                 | 137                |               |

**Table 4.1** Character Position Descriptions (Sheet 2 of 2)

| Character 12 | Character 14 | Character 14 Description |                    |               |
|--------------|--------------|--------------------------|--------------------|---------------|
|              |              | Package Area             | Package Ball Count | Raw Ball Size |
| K            | A            | 11x11 mm                 | 112                | 0.45 mm       |
|              | B            | 11x11 mm                 | 112                | 0.50 mm       |
|              | D            | 12x12 mm                 | 128                | 0.45 mm       |
|              | F            | 12x12 mm                 | 128                | 0.50 mm       |
|              | G            | 14x14 mm                 | 152                | 0.45 mm       |
|              | H            | 14x14 mm                 | 152                | 0.50 mm       |
|              | J            | 15x15 mm                 | 160                | 0.45 mm       |
|              | K            | 15x15 mm                 | 160                | 0.50 mm       |
|              | L            | 17x17 mm                 | 192                | 0.45 mm       |
|              | M            | 17x17 mm                 | 192                | 0.50 mm       |

### 4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| S71WS-P Valid Combinations |                        |                    |              |                  | NOR Flash Speed (MHz) | CellularRAM Speed (MHz) | CellularRAM Supplier | Package Type | Package Markings |
|----------------------------|------------------------|--------------------|--------------|------------------|-----------------------|-------------------------|----------------------|--------------|------------------|
| Device                     | Package & Material Set | Package Descriptor | Model Number | Packing Type     |                       |                         |                      |              |                  |
| S71WS512PD0                | HF                     | 3                  | HL           | 0, 2, 3 (Note 1) | 108                   | 104                     | Type 2               | 8 x 11.6 mm  | (Note 2)         |
|                            |                        |                    | HR           |                  | 80                    |                         |                      |              |                  |
| S71WS512PC0                |                        |                    | SV           |                  | 66                    |                         |                      |              |                  |

**Notes:**

1. Packing Type 0 is standard. Specify other options as required.
2. BGA package marking omits leading S and packing type designator from ordering part number.



## 6. Revision History

### 6.1 Revision A (February 21, 2006)

Initial release.

### 6.2 Revision A1 (April 12, 2006)

Added the S71WS512PC0

### 6.3 Revision A2 (August 21, 2006)

Added the S71WS512PD0 108MHz OPN

#### ***Colophon***

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