Integrated Device Technology, Inc.

HIGH-SPEED 36K (4K x 9-BIT) DUAL-PORT RAM

IDT7014S

FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 20/25/35ns (max.)
  - — Commercial: 12/15/20/25ns (max.)
- Low-power operation
  - — IDT7014S
    Active: 900mW (typ.)
- IDT'S BiCMOS process
- Fully asynchronous operation from either port
- TTL-compatible; single 5V (±10%) power supply
- Available in 52-pin PLCC, 68-pin LCC, and a 64-pin TQFP
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7014 is an extremely high-speed 4K x 9 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to high-speed applications which do not rely on BUSY signals to manage simultaneous access.

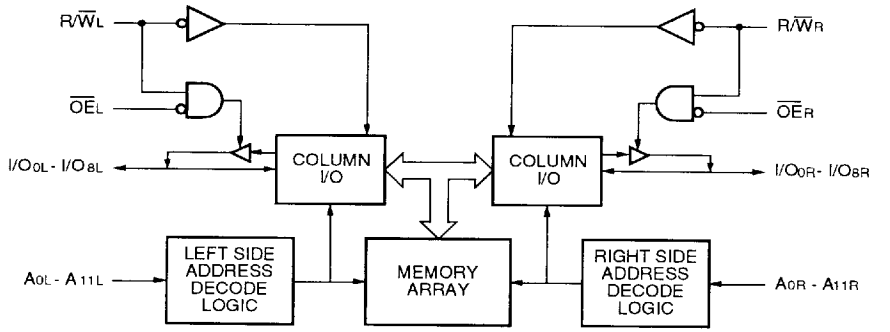
The IDT7014 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. See functional description.

The IDT7014 utilitizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's BiCMOS high-performance technology, these Dual-Ports typically operate on only 900mW of power at maximum access times as fast as 12ns.

The IDT7014 is packaged in a 52-pin PLCC and 68-pin fine pitch LCC, and a 64-pin thin plastic quad flatpack, (TQFP). Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

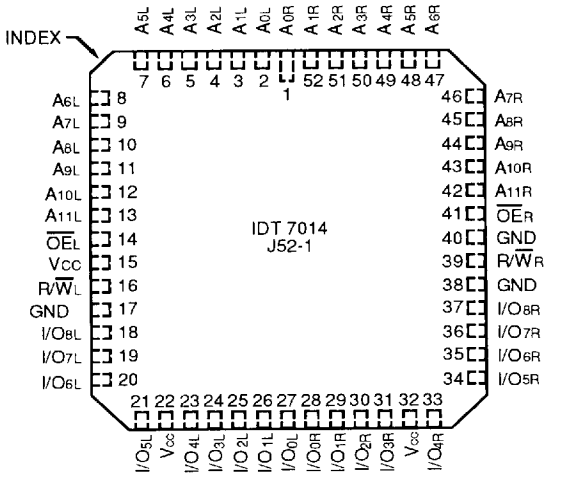
FUNCTIONAL BLOCK DIAGRAM



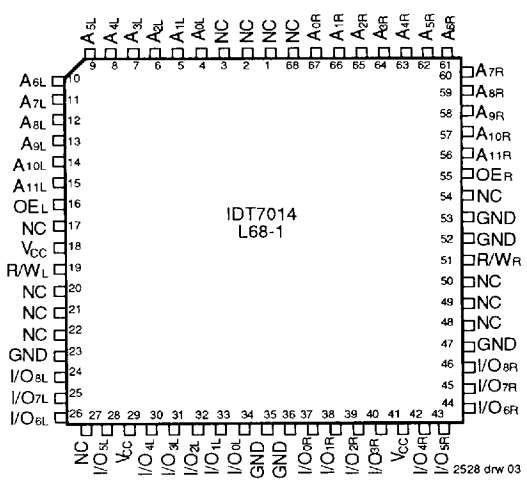
2528 drw 01

PIN CONFIGURATION

INTEGRATED DEVICE

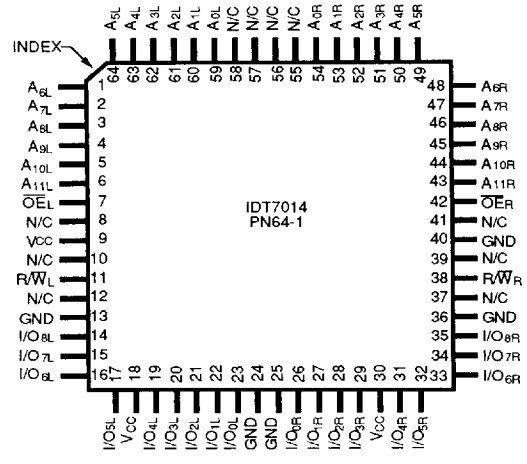


PLCC
Top View



LCC
Top View

NOTES:
1 All Vcc pins must be connected to power supply
2 All ground pins must be connected to ground supply



TQFP
Top View

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0 5 to +7 0	–0 5 to +7 0	V
VTERM(3)	Terminal Voltage	–0 5 to Vcc	–0 5 to Vcc	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2528 tbl 01

NOTES:
1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliability
2 Inputs and Vcc terminals only
3 I/O terminals only

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5 0V ± 10%
Commercial	0°C to +70°C	0V	5 0V ± 10%

2528 tbl 02

RECOMMENDED DC OPERATING CONDTIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4 5	5 0	5 5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2 2	—	6 0	V
VIL	Input Low Voltage	–0 5(1)	—	0 8	V

NOTE:
1 VIL = –3 0V for pulse width less than 20ns

2528 tbl 03

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7014S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	V

2528 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	IDT7014S12[1]		IDT7014S15[1]		IDT7014S20		IDT7014S25		IDT7014S35[2]		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	Outputs Open f = f_{MAX}[3]	Mil.	—	—	—	260	—	260	—	255	—	250	mA
			Com'l.	—	250	—	250	—	245	—	240	—	—	

2528 tbl 05

NOTES:
1. 0°C to +70°C temperature range only
2. –55°C to +125°C temperature range only
3. At f = fMAX, address inputs are cycling at the maximum read cycle of 1/tRC using the "AC Test Conditions" input levels of GND to 3V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2528 tbl 06

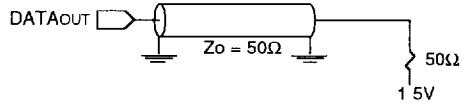


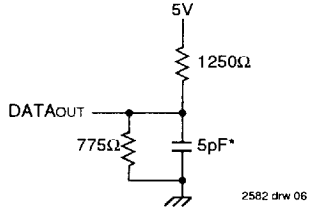
Figure 1. Output load.

2528 drw 05

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

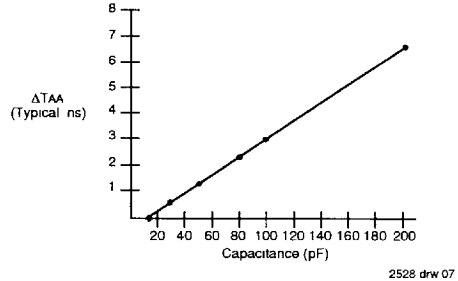
Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

2528 tbl 07



* Including scope and jig.

Figure 2. Output Load (for tHZ, tWZ, and tOW)



2528 drw 07

Figure 3. Lumped Capacitive Load, Typical Derating.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

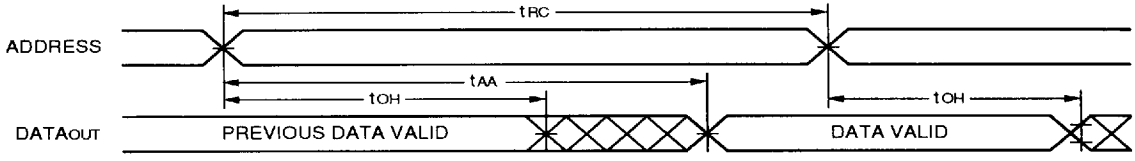
INTEGRATED DEVICE

Symbol	Parameter	7014Sx12[3] Min.	7014Sx12[3] Max.	7014Sx15[3] Min.	7014Sx15[3] Max.	7014Sx20 Min.	7014Sx20 Max.	7014Sx25 Min.	7014Sx25 Max.	7014Sx35[4] Min.	7014Sx35[4] Max.	Unit
READ CYCLE												
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	8	—	8	—	10	—	12	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	0	—	0	—	0	—	0	—	3	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	7	—	7	—	9	—	11	—	15	ns

2528 tbl 08

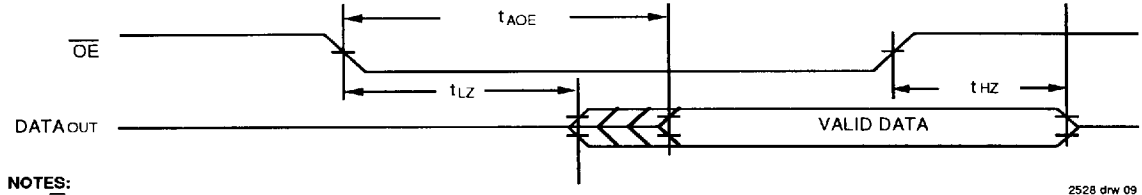
NOTES:
1 Transition is measured ±500mV from low or high-impedance voltage with load (Figure 2)
2 This parameter is guaranteed but not tested
3 0°C to +70°C temperature range only
4 –55°C to +125°C temperature range only

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2]



2528 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2528 drw 09

NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2 $\overline{OE}$ = V_{IL}
3 Addresses valid prior to $\overline{OE}$ transition LOW

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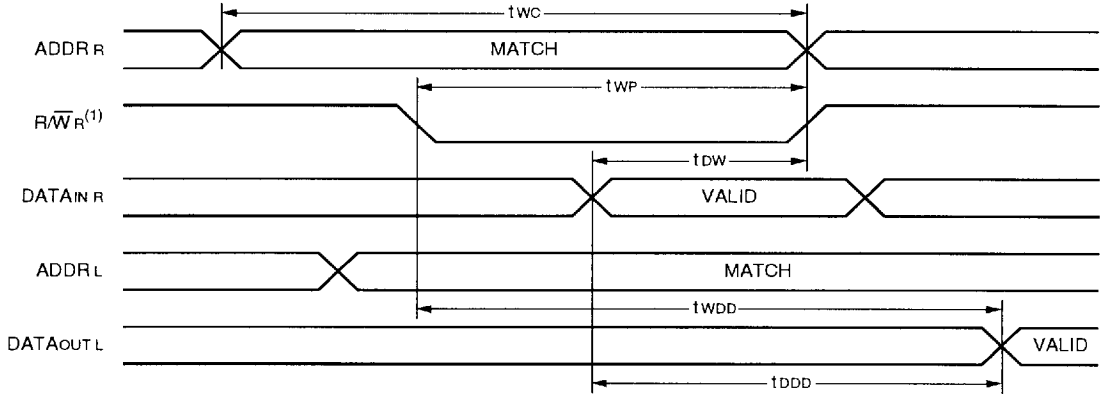
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	7014S12[5]		7014S15[5]		7014S20		7014S25		7014S35[6]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE												
tWC	Write Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
tAW	Address Valid to End-of-Write	10	—	14	—	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	15	—	20	—	30	—	ns
tWR	Write Recovery Time	1	—	1	—	2	—	2	—	2	—	ns
tDW	Data Valid to End-of-Write	8	—	10	—	12	—	15	—	25	—	ns
tHZ	Output High-Z Time[1, 2]	—	7	—	7	—	9	—	11	—	15	ns
tDH	Data Hold Time[3]	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High-Z[1, 2]	—	7	—	7	—	9	—	11	—	15	ns
tOW	Output Active from End-of-Write[1, 2, 3]	0	—	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay[4]	—	25	—	30	—	40	—	45	—	55	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	22	—	25	—	30	—	35	—	45	ns

2528 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high-impedance voltage with load (Figure 2)
2. This parameter is guaranteed but not tested
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay"
5. 0°C to +70°C temperature range only
6. –55°C to +125°C temperature range only

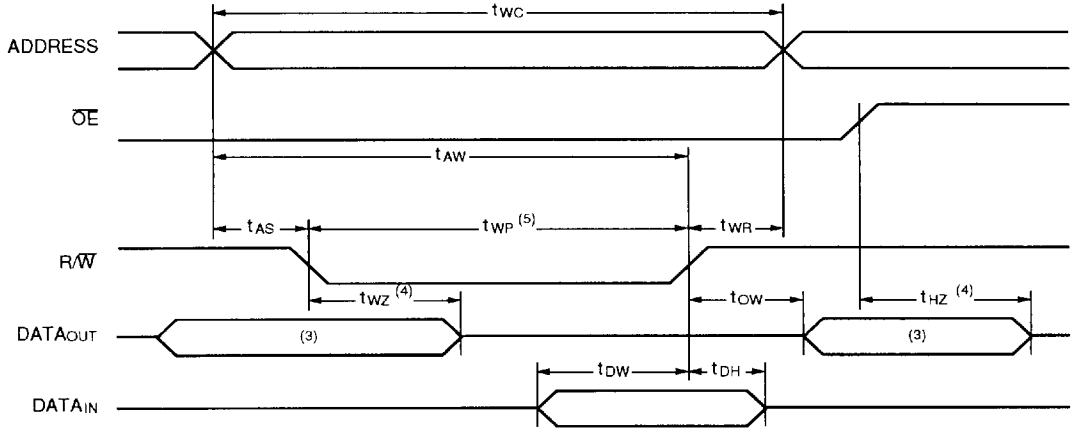
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY



2528 drw 10

TIMING WAVEFORM OF WRITE CYCLE[1, 2, 3, 4, 5]

INTEGRATED DEVICE



2528 drw 11

NOTES:
1 Either R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions
2 tWR is measured from R/$\overline{W}$ going HIGH to the end of write cycle
3 During this period, the I/O pins are in the output state, and input signals must not be applied
4 Transition is measured ±500mV from steady state with a 5pF load (including scope and jig) This parameter is sampled and not 100% tested
5 If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP

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FUNCTIONAL DESCRIPTION

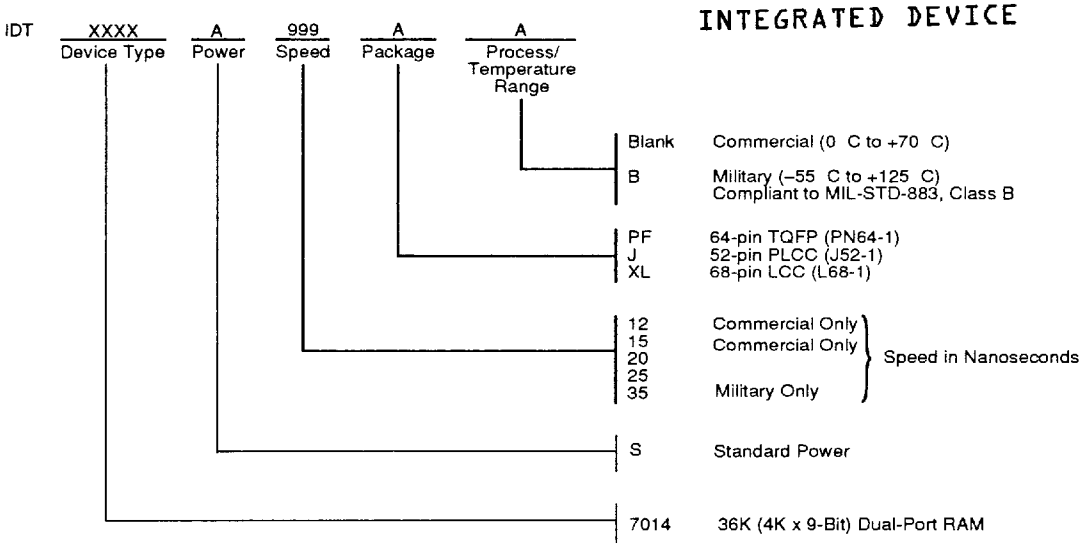
The IDT7014 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. It lacks the chip enable feature of CMOS Dual Ports, thus it operates in active mode as soon as power is applied. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. The user application should avoid simultaneous write operations to the same memory location. There is no on-chip arbitration circuitry to resolve write priority and partial data from both ports may be written. READ/WRITE conditions are illustrated in table 1.

TABLE I – READ/WRITE CONTROL

Left or Right Port[1]			
R/$\overline{W}$	$\overline{OE}$	D0-8	Function
L	X	DATAIN	Data on port written into memory
H	L	DATAOUT	Data in memory output on port
X	H	Z	High-impedance outputs

NOTE: 2528 tbl 10
1 AOL - A11L ≠ AOR - A11R
H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ORDERING INFORMATION



2528 drw 12