REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24									

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
92-09-11

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 64 - MACROCELL ELECTRICALLY PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-92158
A	67268	

SHEET 1 OF 24

DESC FORM 193
JUL 91

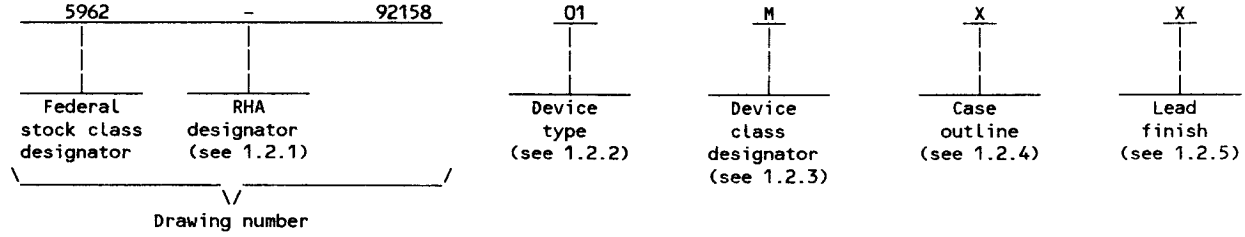
5962-E607-92

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		64-Macrocell EPLD	40 ns
02		64-Macrocell EPLD	30 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GQCC1-J44 or CQCC2-J44	44	"J" lead chip carrier 2/

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings. 3/

Supply voltage range to ground potential (V_{CC})	-2.0 V dc to +7.0 V dc
DC input voltage range	-2.0 V dc to +7.0 V dc
Maximum power dissipation	1.5 W 4/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C
Endurance	25 erase/write cycles (minimum)
Data Retention	10 years (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	5/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Must withstand the added P_D due to short circuit test (e.g., I_{SC})
5/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Goverment standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a full military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein) or qualification conformance inspection, groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA V_{IH} = 2.2 V, V_{IL} = 0.8 V				0.45	
Input high voltage 1/ 2/	V_{IH}				2.2		
Input low voltage 1/ 2/	V_{IL}					0.8	
Input leakage current	I_{IX}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND			-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND			-40	+40	
Output short circuit current 3/ 4/	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V			-30	-90	mA
Power supply current 4/ 5/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} to GND $f = f_{MAX1}$				275	
Power supply current (standby) 2/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} to GND,				200	
Input capacitance 2/	C_{IN}	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.4.1e)	4			10	pF
Output capacitance 2/	C_{OUT}	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.4.1e)	4			10	
Functional testing		See 4.4.1c	7,8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Dedicated input to combinatorial output delay 7/	t_{PD1}	See figures 3 (circuit A) and 4 6/	9,10,11	01		40	ns
				02		30	
I/O input to combinatorial output delay 8/	t_{PD2}			01		62	
				02		44	
Dedicated input to combinatorial output delay with expander delay 9/	t_{PD3}			01		65	
				02		44	
I/O input to combinatorial output delay with expander delay 2/ 4/ 10/	t_{PD4}			01		87	
				02		58	
Input to output enable delay 4/ 7/	t_{EA}			01		40	
				02		30	
Input to output disable delay 4/ 7/	t_{ER}	See figures 3 (circuit B) and 4 6/		01		40	
				02		30	
Synchronous clock input to output delay	t_{CO1}	See figures 3 (circuit A) and 4 6/		01		23	
				02		16	
Synchronous clock to local feedback to combinatorial output 4/ 11/	t_{CO2}			01		48	
				02		35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Dedicated input or feedback setup time to synchronous clock input 7/ 12/	t_{S1}	See figures 3 (circuit A) and 4 6/	9,10,11	01	28		ns
				02	20		
I/O input setup time to synchronous clock input 7/ 12/	t_{S2}			01	45		
				02	35		
Input hold time from synchronous clock input 7/	t_H			All	0		
Synchronous clock input high time 2/	t_{WH}			01	15		
				02	10		
Synchronous clock input low time 2/	t_{WL}			01	15		
				02	10		
Asynchronous clear width 2/ 4/ 7/	t_{RW}			01	40		
				02	30		
Asynchronous clear recovery time 2/ 4/ 7/	t_{RR}			01	40		
				02	30		
Asynchronous clear to registered output delay 2/ 7/	t_{RO}			01		40	
				02		30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Asynchronous preset width 2/ 4/ 7/	t_{PW}	See figures 3 (circuit A) and 4 6/	9,10,11	01	40		ns
				02	30		
Asynchronous preset recovery time 2/ 4/ 7/	t_{PR}			01	40		
				02	30		
Asynchronous reset to registered output delay 2/ 7/	t_{PO}			01		40	
				02		30	
Synchronous clock to local feedback input 4/ 13/	t_{CF}			01		7	
				02		3	
External synchronous clock period ($1/f_{MAX3}$) 4/	t_P			01	30		
				02	20		
External maximum frequency ($1/(t_{CO} + t_{S1})$) 4/ 14/	f_{MAX1}			01	19.6		MHz
				02	27		
Internal local feedback maximum frequency, lesser of ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$) 4/ 15/	f_{MAX2}			01	28.5		
				02	43		
Data path maximum frequency, least of $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$ or ($1/t_{CO1}$) 4/ 16/	f_{MAX3}			01	33		
				02	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Maximum register toggle frequency $(1/(t_{WL} + t_{WH}))$ 4/ 17/	f_{MAX4}	See figures 3 (circuit A) and 4 6/	9,10,11	01	33		MHz
				02	40	50	
Output data stable time from synchronous clock input 4/ 18/	t_{OH}			All	3		ns
External asynchronous switching characteristics							
Asynchronous clock input to output delay 6/	t_{ACO1}	See figures 3 (circuit A) and 4 6/	9,10,11	01		45	ns
				02		30	
Asynchronous clock input to local feedback to combinatorial output 2/ 19/	t_{ACO2}			01		64	
				02		46	
Dedicated input or feedback setup time to asynchronous clock input 6/	t_{AS1}			01	10		
				02	6		
I/O input setup time to asynchronous clock input 4/ 6/	t_{AS2}			01	34		
				02	25		
Input hold time from asynchronous clock input 6/	t_{AH}			01	15		
				02	8		
Asynchronous clock input high time 2/ 6/	t_{AWH}			01	17.5		
				02	14		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Asynchronous clock input low time 2/ 7/ 20/	t_{AWL}	See figures 3 (circuit A) and 4 6/	9,10,11	01	17.5		ns
				02	11		
Asynchronous clock to local feedback input 4/ 21/	t_{ACF}			01		26	
				02		18	
External asynchronous clock period ($1/f_{MAXA4}$) 4/	t_{AP}			01	35		
				02	25		
External maximum frequency in asynchronous mode $1/(t_{ACO1} + t_{AS1})$ 4/ 22/	f_{MAXA1}			01	18		MHz
				02	27		
Maximum internal asynchronous frequency ($1/(t_{S1} + t_{CF})$) or ($1/t_{CO1}$) 4/ 23/	f_{MAXA2}			01	27		
				02	40		
Data path maximum frequency in asynchronous mode $1/(t_{WL} + t_{WH})$, $1/(t_{S1} + t_H)$ or ($1/t_{CO1}$) 4/ 24/	f_{MAXA3}			01	22		
				02	33		
Maximum asynchronous register toggle frequency $1/(t_{AWH} + t_{AWL})$ 4/ 25/	f_{MAXA4}			01	28.5		
				02	40		
Output data stable time from asynchronous clock input 4/ 26/	t_{AOH}			All	15		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second.
4/ May not be tested but shall be guaranteed to the limits specified in table I.
5/ Measured with device programmed as a 16-bit counter in each LAB.
6/ AC tests are performed with input rise and fall times of 6 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output loads on figure 3.
7/ This specification is a measure of the delay from input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.

When this note is appled to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.

If an input signal is applied to an I/O pin, an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used, add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
8/ This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
9/ This specification is a measure of the delay from an input signal applied to a dedicated input to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

TABLE I. Electrical performance characteristics - Continued.

10/ This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
11/ This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB.
12/ If data is applied to an I/O input for capture by a macrocell register, the I/O pin set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
13/ This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB.
14/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs.
15/ This specification indicates the guaranteed maximum frequency at which a state machine, with internal-only feedback, can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$. All feedback is assumed to be local, originating within the same LAB.
16/ This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used.
17/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled.
18/ This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.
19/ This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB.
20/ This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped. If a given input is used to clock multiple registers with both positive and negative polarity, t_{AWH} should be used for both t_{AWH} and t_{AWL}.
21/ This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array in put. This delay plus the asynchronous register set-up time, t_{AS1}, is the minimum internal period for an internal asynchronous clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path, and assumes that the clock input signal is applied to a dedicated input pin.
22/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs, and that no expander logic is employed in the clock signal path or data path.
23/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal-only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + 1/t_{AS1}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
24/ This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
25/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
26/ This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 Processing EPLDs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Erasure of EPLDs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.6.

3.12.2 Programmability of EPLDs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7.

3.12.3 Verification of erasure or programmed EPLDs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors, this reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

(1) All devices selected for testing shall be programmed in accordance with 3.2.3.1 herein.

(2) Verify pattern (see 3.12.3).

(3) Erase (see 3.12.1).

(4) Verify pattern erasure (see 3.12.3)

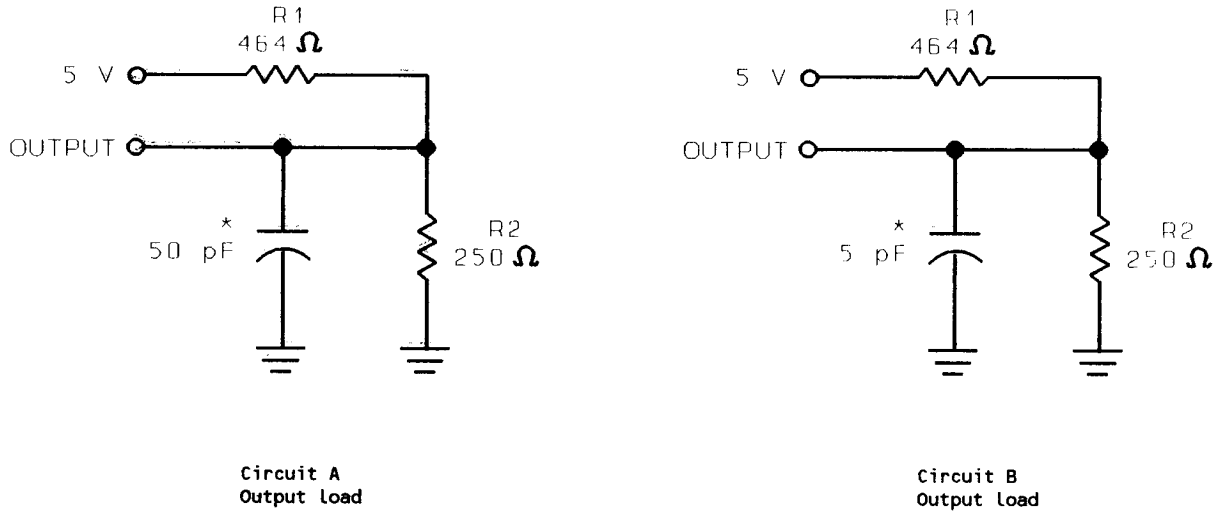
Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	I/O
2	I/O
3	V_{CC}
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	INPUT
10	GND
11	INPUT
12	INPUT
13	INPUT
14	V_{CC}
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND
22	I/O
23	I/O
24	I/O
25	V_{CC}
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	INPUT
32	GND
33	INPUT
34	INPUT/CLK
35	INPUT
36	V_{CC}
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	GND
44	I/O

FIGURE 1. Terminal connections.

Truth table		
Input pins		Output pins
I/CLK	I	I/O
X	X	Z

NOTES:
1. X = Don't care.
2. Z = High impedance.

FIGURE 2. Truth table (unprogrammed).



Circuit A
Output load

Circuit B
Output load

*Including scope and jig (minimum values).

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 6 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

Input pulses

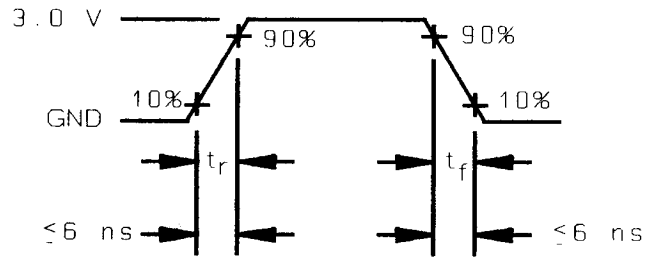
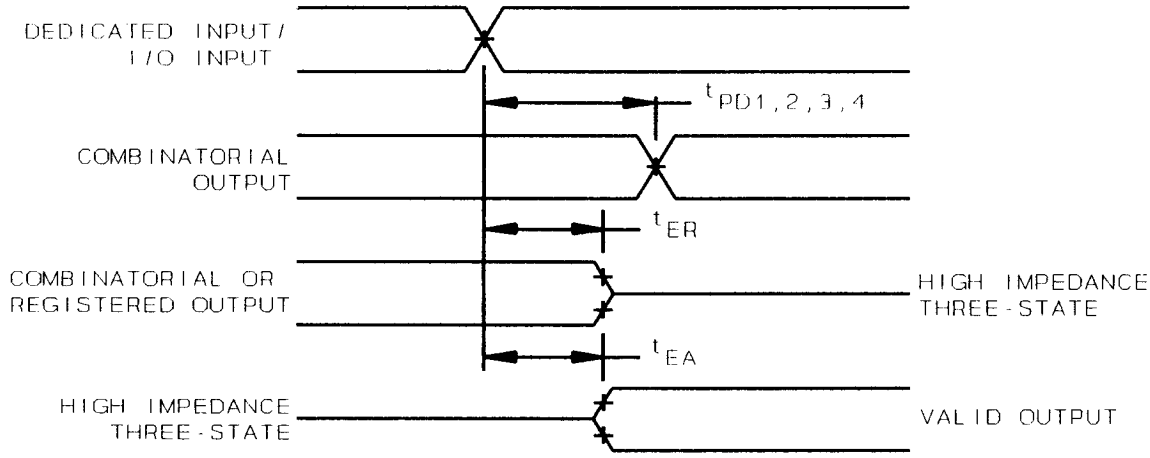


FIGURE 3. Output load circuits and test conditions.

External combinatorial



External synchronous

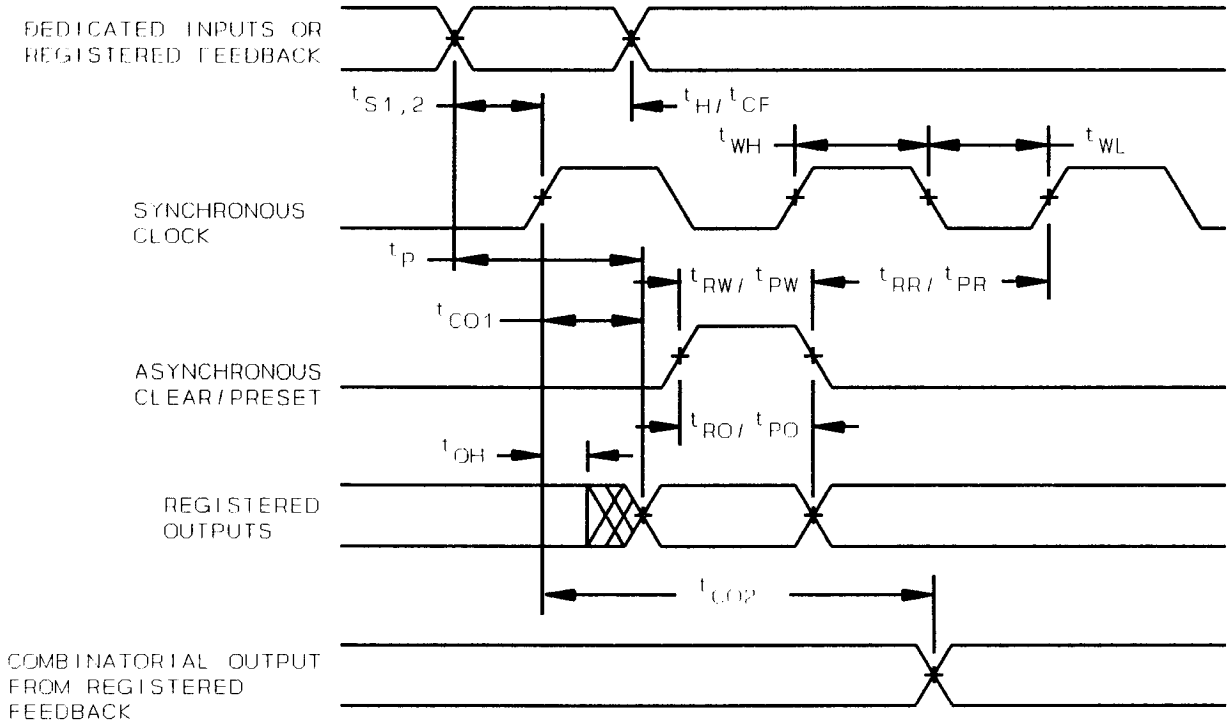


FIGURE 4. Switching waveforms.

External asynchronous

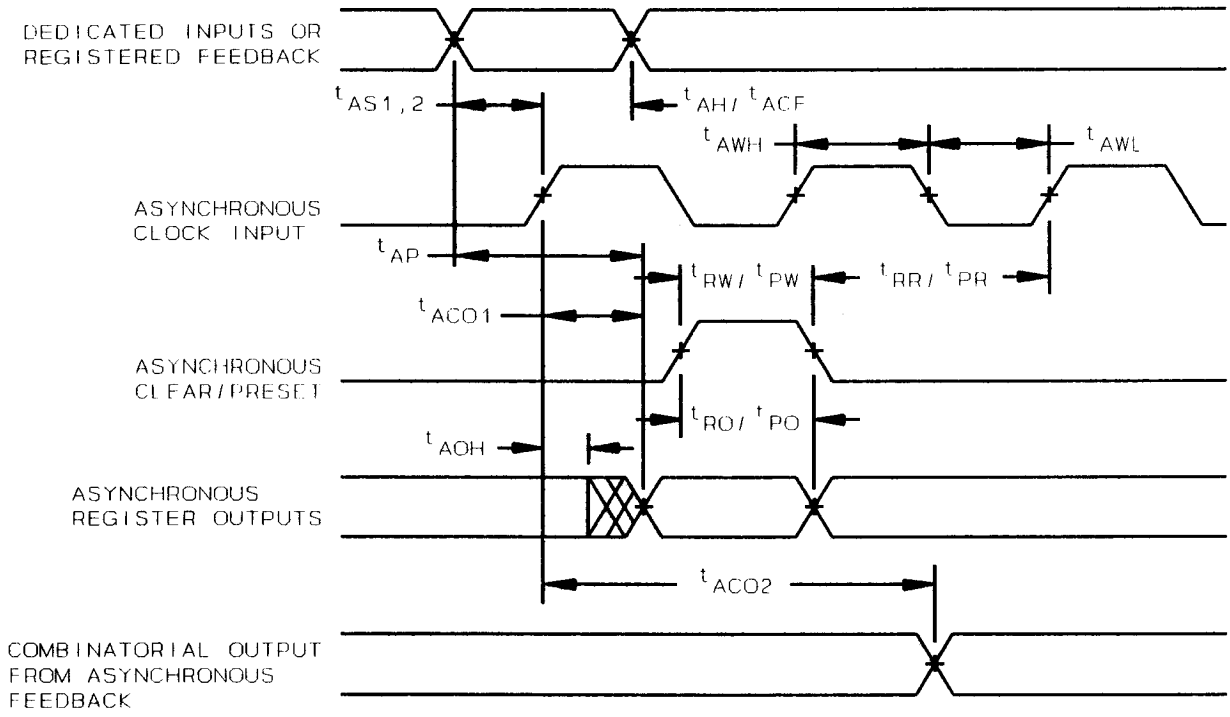


FIGURE 4. Switching waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the burn-in test circuit shall be submitted to DESC-EC for review with the certificate of compliance. For device classes B and S, the burn-in test circuit shall be submitted to the qualifying activity.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48-hour burn-in shall be broken into two sequences of 24 hours each (Static I and Static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassmbled devices.)

Margin test method. *Steps 1 through 3 may be performed at wafer level.

(1) Program a minimum or 95 percent of the total number of cells, including the slowest programming cell (see 3.12.2).

(2) Bake, unbiased, for 72 hours at +140°C or for 32 hours at +150°C or for 8 hours at +200°C or for 2 hours at +300°C for unassembled devices only.

(3) Perform electrical test (see 4.2.b) at +25°C including a margin test at Vm = +5.7 V and loose timing (i.e., 1 µs).

(4) Erase (see 3.12.1).

(5) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell (see 3.12.2).

(6) Perform electrical test (see 4.2.b) at +25°C including a margin test at Vm = +5.7 V and loose timing (i.e., 1 µs).

(7) Perform burn-in (see 4.2.1a).

(8) Perform electrical test (see 4.2.1b) at +25°C including a margin test at Vm = +5.7 V and loose timing (i.e., 1 μs).

(9) Perform electrical tests at T_C = +125°C.

(10) Perform electrical tests at T_C = -55°C.

(11) Erase (see 3.12.1). Devices may be submitted for groups A, B, C, and D testing.

(12) Verify erasure (see 3.12.3).

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-EC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

d. Additional requirements beyond MIL-I-38535 for classes Q and V are specified in table IIA herein.

4.2.3 Percent Defective Allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specifed PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extension for device class B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.3 Electrostatic Discharge Sensitivity (ESDS) inspection. ESDS testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9		1,7,9
2	Static burn-in (method 1015)	Not required	Not required	Required	Not required	Required
3	Same as line 1			1 Δ		1 Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7* Δ		1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11 Δ		
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ		1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1b.
6/ Δ indicates delta limit (see table IIC) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIC).
7/ The device manufacturer may at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100 percent
Internal visual	2010, condition A or approved alternate	100 percent
Nondestructive bond pull	2023 or approved alternate	100 percent
Reverse bias burn-in	1015	100 percent
Burn-in	1015, total of 240 hours at +125°C	100 percent
Radiographic	2012	100 percent

TABLE IIC. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{IX} standby	±1 μA value in table I
I_{OZ}	±4 μA value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revison level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S, the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the qualifying activity upon request. For device classes Q and V, the procedures and circuits shall be shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIC herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIC herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be submitted to DESC-EC for review with the certificate of compliance. For device class B the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-EC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, or H and for device class M, shall be M or D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisiton document. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein. RHA samples need not be tested at -55°C or +125°C prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein. Additionally classes Q and V, for quality conformance inspection may be at wafer level.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510 (device classes M, B, and S) and MIL-I-38535 (device classes Q and V) for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure.

e. Prior to and during total dose irradiation, the devices shall be biased to the worst case conditions established during characterization.

f. Single event phenomena (SEP) testing shall be performed on all class S and V devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics of the device. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. For device class V, the device parametrics that influence single event upset immunity shall be monitored at the wafer level as part of a TRB approved wafer level hardness plan. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

(2) The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

(3) The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} =5.5 V dc for the latch-up measurements.

g. For device classes M, B, and S, subgroups 1 and 2 of table V method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

i. Transient dose rate survivability testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence latch-up and device burn-out shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

j. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels.

(3) Test conditions (SEP).

(4) Number of upsets (SEP).

(5) Number of transients.

(6) Occurence of latch-up.

4.5 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIC. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Erasing procedure. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2,537 Angstroms (Å). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 15 ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7,258 ws/cm^2 (1 week at 12,000 μW/cm^2). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.7 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

C_{IN}	Input terminal capacitance.
C_{OUT}	Output terminal capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IX}	Input current.
I_{OZ}	Output current.
T_C	Case temperature.
V_{CC}	Positive supply voltage.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique part numbers. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique part number. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-92XXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-92XXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-92XXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-92XXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.