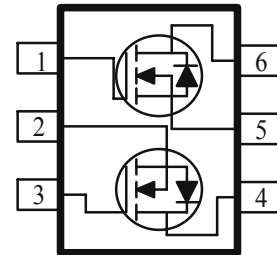
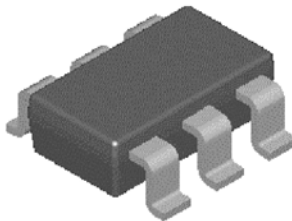


N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TSOP-6 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	58 @ $V_{GS} = 10V$	3.5
	82 @ $V_{GS} = 4.5V$	3.0

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	A
	$T_A = 70^\circ C$		
Pulsed Drain Current ^b	I_{DM}	16	
Continuous Source Current (Diode Conduction) ^a	I_S	1.25	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	W
	$T_A = 70^\circ C$		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	$R_{\theta JA}$	$^\circ C/W$
	Steady-State		100
			166

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

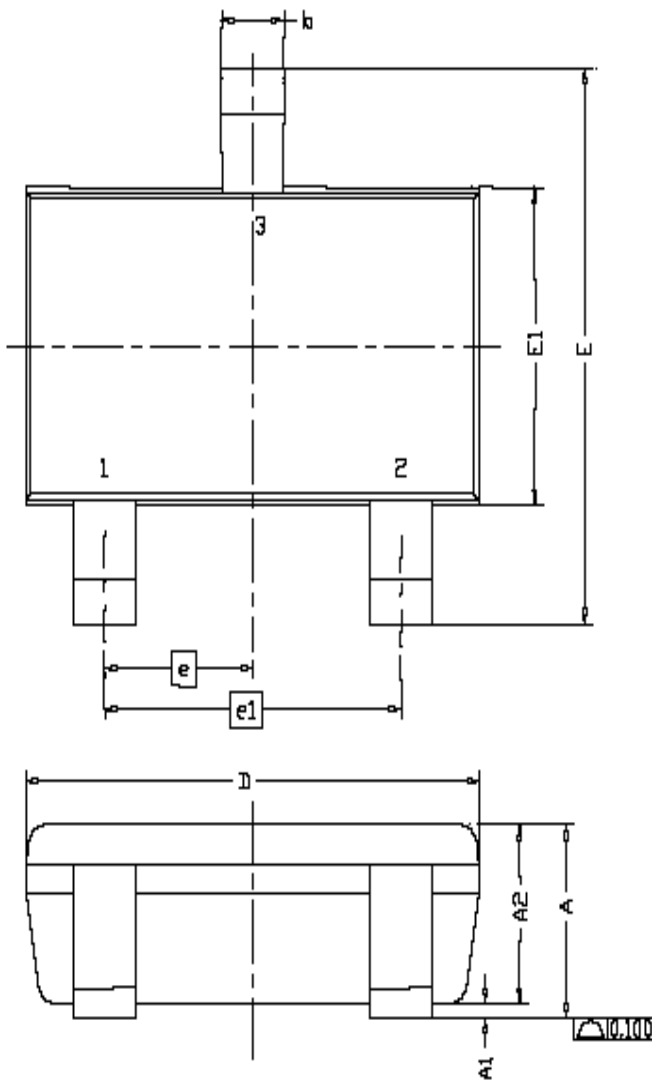
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = 20 V$			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 V, V_{GS} = 0 V$			1	uA
		$V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55^\circ C$			25	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 10 V$	6			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 V, I_D = 3.5 A$			58	mΩ
		$V_{GS} = 4.5 V, I_D = 3 A$			82	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 15 V, I_D = 3.5 A$		6.9		S
Diode Forward Voltage	V_{SD}	$I_S = 2.3 A, V_{GS} = 0 V$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15 V, V_{GS} = 4.5 V,$ $I_D = 3.5 A$		2.2		nC
Gate-Source Charge	Q_{gs}			0.5		
Gate-Drain Charge	Q_{gd}			0.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 V, R_L = 25 \Omega, I_D = 1 A,$ $V_{GEN} = 10 V$		16		nS
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall-Time	t_f			3		

Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM		

