

## AD7228A

### FEATURES

- Eight 8-Bit DACs with Output Amplifiers
- Operates with Single +5 V, +12 V or +15 V or Dual Supplies
- μP Compatible (95 ns  $\overline{WR}$  Pulse)
- No User Trims Required
- Skinny 24-Pin DIPs, SOIC, and 28-Terminal Surface Mount Packages

### GENERAL DESCRIPTION

The AD7228A contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5 V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when  $\overline{WR}$  goes low. The control logic is speed compatible with most 8-bit microprocessors.

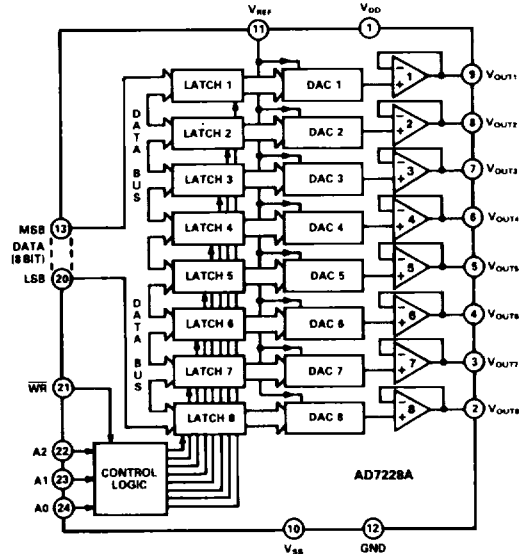
Specified performance is guaranteed for input reference voltages from +2 to +10 V when using dual supplies. The part is also specified for single supply +15 V operation using a reference of +10 V and single supply +5 V operation using a reference of +1.23 V. Each output buffer amplifier is capable of developing +10 V across a 2 kΩ load.

The AD7228A is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC<sup>2</sup>MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

### PRODUCT HIGHLIGHTS

1. Eight DACs and Amplifiers in Small Package  
The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. Single or Dual Supply Operation  
The voltage-mode configuration of the DACs allows single supply operation of the AD7228A. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Microprocessor Compatibility  
The AD7228A has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high performance 8-bit microprocessors.

### FUNCTIONAL BLOCK DIAGRAM



### ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Total Unadjusted Error (LSB)	Package Option <sup>2</sup>
AD7228ABN	-40°C to +85°C	±2 max	N-24
AD7228ACN	-40°C to +85°C	±1 max	N-24
AD7228ABP	-40°C to +85°C	±2 max	P-28A
AD7228ACP	-40°C to +85°C	±1 max	P-28A
AD7228ABR	-40°C to +85°C	±2 max	R-24
AD7228ACR	-40°C to +85°C	±1 max	R-24
AD7228ABQ	-40°C to +85°C	±2 max	Q-24
AD7228ACQ	-40°C to +85°C	±1 max	Q-24
AD7228ATQ <sup>3</sup>	-55°C to +125°C	±2 max	Q-24
AD7228AUQ <sup>3</sup>	-55°C to +125°C	±1 max	Q-24

#### NOTES

<sup>1</sup>To order MIL-STD-883, Class B processed parts, add /883B to part number.

Contact your local sales office for military data sheet and availability.

<sup>2</sup>N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

<sup>3</sup>These grades will be available to /883B processing only.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at <http://www.analog.com>.

# AD7228A—SPECIFICATIONS

**DUAL SUPPLY** ( $V_{DD} = 10.8\text{ V to }16.5\text{ V}$ ;  $V_{SS} = -5\text{ V} \pm 10\%$ ;  $GND = 0\text{ V}$ ;  $V_{REF} = +2\text{ V to }+10\text{ V}$ <sup>1</sup>;  $R_L = 2\text{ k}\Omega$ ,  $C_L = 100\text{ pF}$  unless otherwise noted.) All specifications  $T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.

Parameter	B Version <sup>2</sup>	C Version	T Version	U Version	Units	Conditions/Comments
<b>STATIC PERFORMANCE</b>						
Resolution	8	8	8	8	Bits	$V_{DD} = +15\text{ V} \pm 10\%$ , $V_{REF} = +10\text{ V}$ <b>Guaranteed Monotonic</b> Typical tempco is 5 ppm/°C with $V_{REF} = +10\text{ V}$
Total Unadjusted Error <sup>1</sup>	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	
Full-Scale Error <sup>1</sup>	±1	±1/2	±1	±1/2	LSB max	
Zero Code Error $\alpha$ 25°C	±25	±15	±25	±15	mV max	Typical tempco is 30 $\mu\text{V}/^\circ\text{C}$
$T_{MIN}$ to $T_{MAX}$	±30	±20	±30	±20	mV max	
Minimum Load Resistance	2	2	2	2	k $\Omega$ min	$V_{OUT} = +10\text{ V}$
<b>REFERENCE INPUT</b>						
Voltage Range <sup>1</sup>	2 to 10	2 to 10	2 to 10	2 to 10	V min/V max	Occurs when each DAC is loaded with all 1s. $V_{REF} = 8\text{ V}$ p-p Sine Wave $\alpha$ 10 kHz
Input Resistance	2	2	2	2	k $\Omega$ min	
Input Capacitance <sup>5</sup>	500	500	500	500	pF max	
AC Feedthrough	70	70	70	70	dB typ	
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$	2.4	2.4	2.4	2.4	V min	$V_{IN} = 0\text{ V or }V_{DD}$
Input Low Voltage, $V_{ISL}$	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	$\mu\text{A}$ max	
Input Capacitance <sup>4</sup>	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
<b>DYNAMIC PERFORMANCE</b> <sup>3</sup>						
Voltage Output Slew Rate	2	2	2	2	V/ $\mu\text{s}$ min	$V_{REF} = +10\text{ V}$ ; Settling Time to $\pm 1/2$ LSB $V_{REF} = +10\text{ V}$ ; Settling Time to $\pm 1/2$ LSB Code transition all 0s to all 1s. $V_{REF} = 0\text{ V}$ ; $\overline{WR} = V_{DD}$ Code transition all 0s to all 1s. $V_{REF} = +10\text{ V}$ ; $\overline{WR} = 0\text{ V}$
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	$\mu\text{s}$ max	
Negative Full-Scale Change	5	5	5	5	$\mu\text{s}$ max	
Digital Feedthrough	50	50	50	50	nV secs typ	
Digital Crosstalk <sup>6</sup>	50	50	50	50	nV secs typ	
<b>POWER SUPPLIES</b>						
$V_{DD}$ Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	For Specified Performance
$V_{SS}$ Range	4.5/ 5.5	4.5/ 5.5	4.5/ 5.5	4.5/ 5.5	V min/V max	
$I_{DD}$ $\alpha$ 25°C	16	16	16	16	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or $V_{INH}$
$T_{MIN}$ to $T_{MAX}$	20	20	22	22	mA max	
$I_{SS}$ $\alpha$ 25°C	14	14	14	14	mA max	
$T_{MIN}$ to $T_{MAX}$	18	18	20	20	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or $V_{INH}$

**SINGLE SUPPLY** ( $V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = GND = 0\text{ V}$ ;  $V_{REF} = +10\text{ V}$ ;  $R_L = 2\text{ k}\Omega$ ,  $C_L = 100\text{ pF}$  unless otherwise noted.) All specifications  $T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.

Parameter	B Version <sup>2</sup>	C Version	T Version	U Version	Units	Conditions/Comments	
<b>STATIC PERFORMANCE</b>							
Resolution	8	8	8	8	Bits	<b>Guaranteed Monotonic</b> $V_{OUT} = +10\text{ V}$	
Total Unadjusted Error <sup>1</sup>	±2	±1	±2	±1	LSB max		
Differential Nonlinearity	±1	±1	±1	±1	LSB max		
Minimum Load Resistance	2	2	2	2	k $\Omega$ min		
<b>REFERENCE INPUT</b>							
Input Resistance	2	2	2	2	k $\Omega$ min	Occurs when each DAC is loaded with all 1s.	
Input Capacitance <sup>5</sup>	500	500	500	500	pF max		
<b>DIGITAL INPUTS</b>							
	As per Dual Supply Specifications						
<b>DYNAMIC PERFORMANCE</b> <sup>3</sup>							
Voltage Output Slew Rate	2	2	2	2	V/ $\mu\text{s}$ min	Settling Time to $\pm 1/2$ LSB Settling Time to $\pm 1/2$ LSB Code transition all 0s to all 1s. $V_{REF} = 0\text{ V}$ ; $\overline{WR} = V_{DD}$ Code transition all 0s to all 1s. $V_{REF} = +10\text{ V}$ ; $\overline{WR} = 0\text{ V}$	
Voltage Output Settling Time							
Positive Full-Scale Change	5	5	5	5	$\mu\text{s}$ max		
Negative Full-Scale Change	7	7	7	7	$\mu\text{s}$ max		
Digital Feedthrough	50	50	50	50	nV secs typ		
Digital Crosstalk <sup>6</sup>	50	50	50	50	nV secs typ		
<b>POWER SUPPLIES</b>							
$V_{DD}$ Range	13.5/16.5	13.5/16.5	13.5/16.5	13.5/16.5	V min/V max	For Specified Performance	
$I_{DD}$ $\alpha$ 25°C	16	16	16	16	mA max		
$T_{MIN}$ to $T_{MAX}$	20	20	22	22	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or $V_{INH}$	

## NOTES

<sup>1</sup> $V_{OUT}$  must be less than  $V_{DD}$  by 3.5 V to ensure correct operation.

<sup>2</sup>Temperature ranges are as follows:

B, C Versions: -40°C to +85°C

T, U Versions: 55°C to +125°C

<sup>3</sup>Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.

<sup>4</sup>Calculated after zero code error has been adjusted out.

<sup>5</sup>Sample tested at 25°C to ensure compliance.

<sup>6</sup>The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.

Specifications subject to change without notice.