PARADIGM®

PDM4M6124
PDM4M6125
PDM4M6126

128KB/256KB/512KB Second Level Cache Modules for the Intel i486 CPU/82420TX PCI Set

Features:

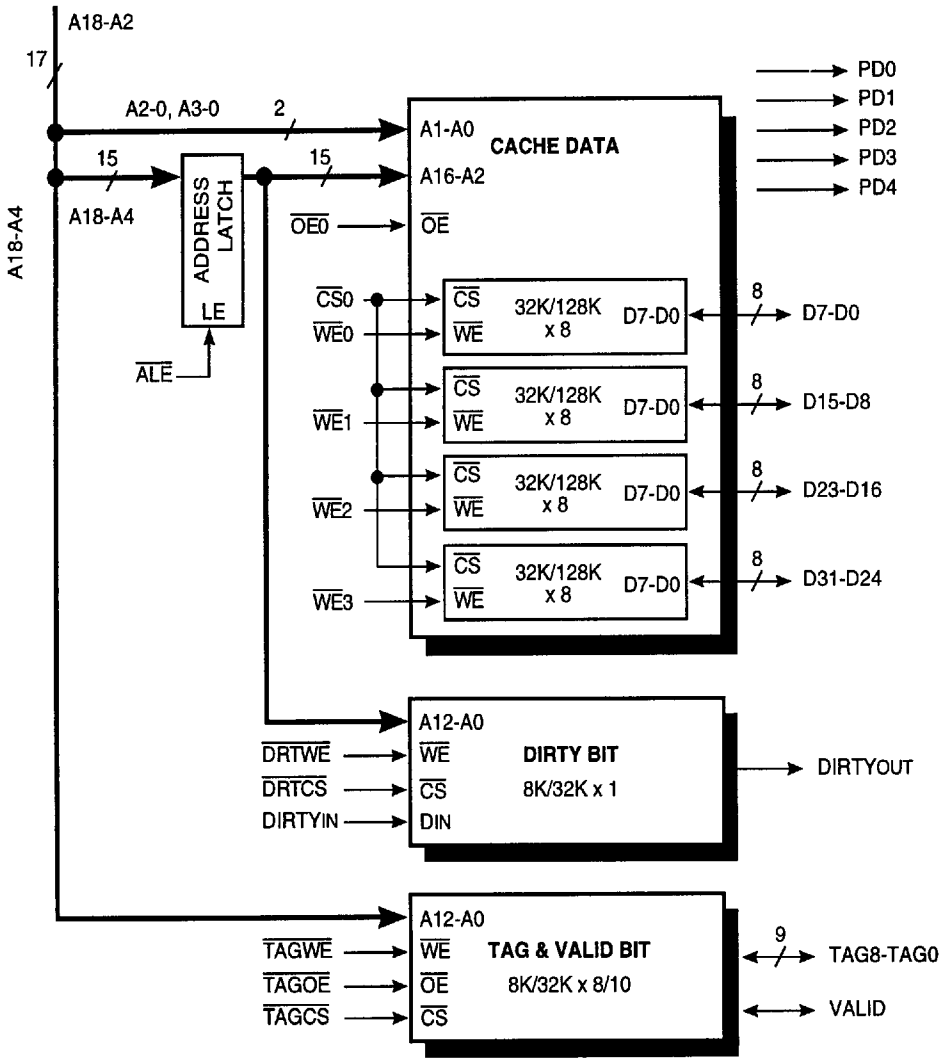
- Available in 128KB/256KB/512KB configurations
- Ideal for use with Intel i486™ based systems, especially those using Intel's 82420TX (Saturn) chipset
- Operates with a wide range of system speeds including 33 MHz
- Presence detect pins map directly into 82424TX CDC
- Single 5V (±5%) power supply
- Low cost, low profile card-edge 112-pin module
- Uses Burndy Computerbus™ Connector part number CELP2X56SC3Z48
- Multiple GND pins and decoupling capacitors for maximum noise immunity

Description:

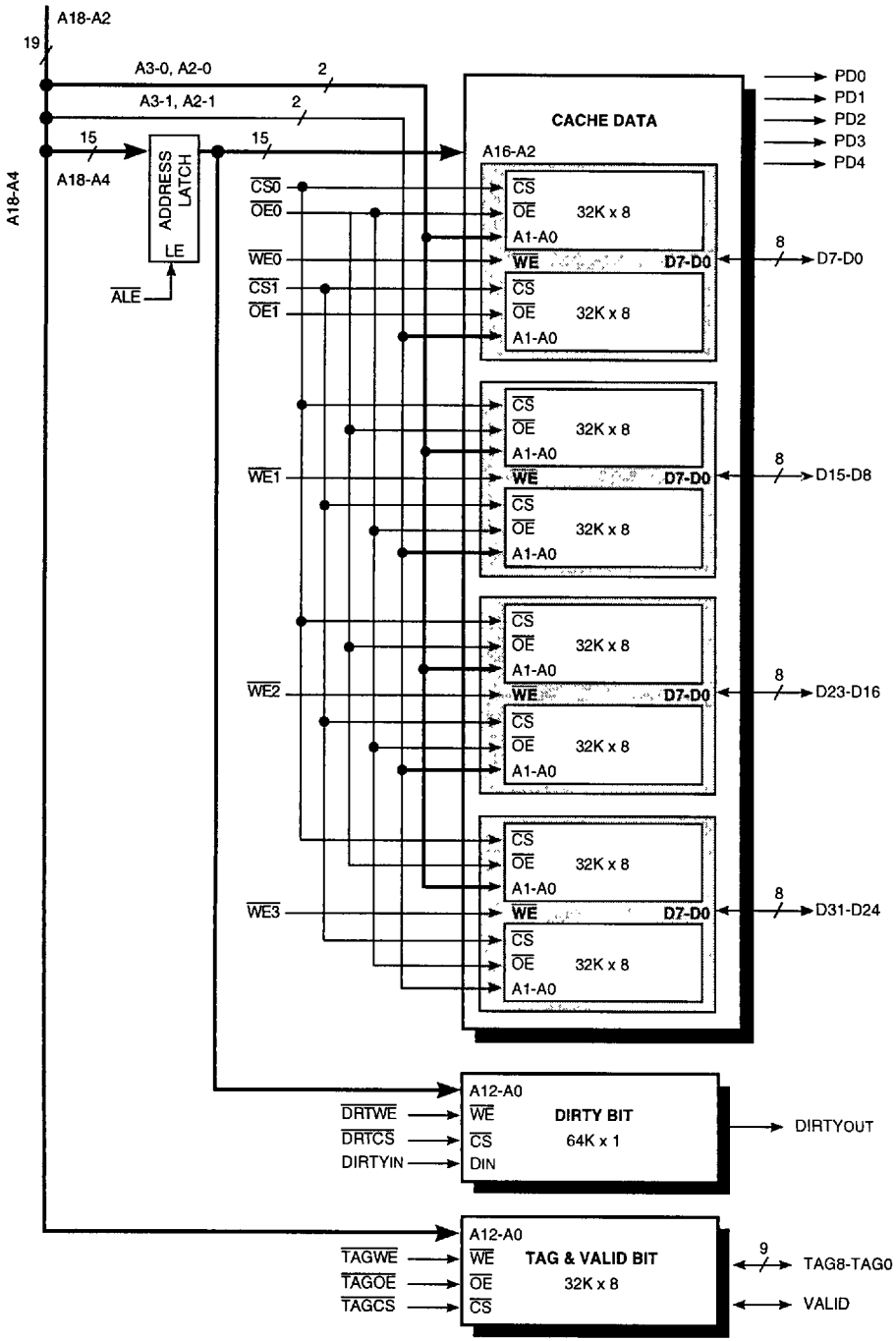
The PDM4M6124, PDM4M6125, and PDM4M6126 are high-performance CMOS static RAM modules. They are designed for use as second level cache in systems using Intel i486 class CPUs and the Intel 82420TX (Saturn) chipset. The PDM4M6124/6125 are based on asynchronous 32K x 8 static RAMs and provide 128KB and 256KB of second level cache, respectively. The PDM4M6126 provides 512KB of second level cache by using 128K x 8 asynchronous static RAMs. The design of the modules includes on-board logic, data and tag SRAM and an additional SRAM used as a dirty bit as specified in the Intel Saturn chipset specification. The on-board presence detect pins, which map directly into the 82424TX chip, allow a system to determine the cache configuration.

The PDM4M6124, PDM4M6125, and PDM4M6126 are available in a 112-pin DIMM package. This low profile package allows for modules with a maximum height of 1.210", a maximum length of 3.150" and a maximum thickness of 0.365". Equal clock line trace lengths ensure minimum clock skew. Multiple GND pins and decoupling capacitors ensure maximum protections from noise.

Functional Block Diagram
PDM4M6124 and PDM4M6126
128KB/512KB Pipelined
Burst Version



Functional Block Diagram
PDM4M6125–256KB
Asynchronous Version



Pin Configuration

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	39	TAG5	77	GND
2	D1	40	GND	78	D28
3	D3	41	TAG7	79	D30
4	D5	42	TAG8	80	A2-0
5	D7	43	$\overline{ALE}$	81	A3-0
6	VCC	44	$\overline{WE0}$	82	VCC
7	NC(2)	45	VCC	83	A4
8	D9	46	GND	84	A6
9	D11	47	$\overline{WE1}$	85	A8
10	D13	48	$\overline{WE2}$	86	A10
11	GND	49	$\overline{WE3}$	87	A12
12	D15	50	VCC	88	A14
13	D17	51	$\overline{OE1}$(1)	89	A16
14	D19	52	$\overline{CS1}$(1)	90	A18
15	D21	53	PD1	91	GND
16	VCC	54	PD3	92	DIRTYIN
17	D23	55	NC	93	TAG0
18	NC(2)	56	GND	94	TAG2
19	D25	57	GND	95	TAG4
20	D27	58	D0	96	GND
21	GND	59	D2	97	TAG6
22	D29	60	D4	98	VALID
23	D31	61	D6	99	$\overline{TAGCS}$
24	A2-1(1)	62	VCC	100	$\overline{TAGWE}$
25	A3-1(1)	63	NC(2)	101	VCC
26	VCC	64	D8	102	GND
27	A5	65	D10	103	$\overline{TAGOE}$
28	A7	66	D12	104	$\overline{DIRTYWE}$
29	A9	67	GND	105	$\overline{DIRTYCS}$
30	A11	68	D14	106	VCC
31	A13	69	D16	107	$\overline{OE0}$
32	A15	70	D18	108	CS0
33	A17	71	D20	109	PD0
34	NC	72	VCC	110	PD2
35	GND	73	D22	111	PD4
36	DIRTYOUT	74	NC(2)	112	GND
37	TAG1	75	D24		
38	TAG3	76	D26		

Pin Assignment

Pin	Signal
A18-A4	Address Inputs
A2-0, A3-0	Lower Order Bank 0 Address Inputs
A2-1, A3-1	Lower Order Bank 1 Address Inputs
D31-D0	Cache Data Inputs/Outputs
$\overline{CS0}$	Bank 0 Chip Select Input
$\overline{CS1}$	Bank 1 Chip Select Input (6125 Only)
$\overline{WE3}$-$\overline{WE0}$	Byte Write Enable Inputs
$\overline{OE0}$	Bank 0 Output Enable Input
$\overline{OE1}$	Bank 1 Output Enable Input (6125 Only)
ALE	Address Latch Enable Input
TAG8-TAG0	Tag Data Inputs/Outputs
VALID	Valid Bit Input/Output
$\overline{TAGWE}$	Tag and Valid Bit Write Enable Input
$\overline{TAGOE}$	Tag and Valid Bit Output Enable Input
$\overline{TAGCS}$	Tag and Valid Bit Chip Select Input
DIRTYIN	Dirty Bit Input
DIRTYOUT	Dirty Bit Output
$\overline{DRTCS}$	Dirty Bit Chip Select Input
$\overline{DRYWE}$	Dirty Bit Write Enable Input
PD4-PD0	Presence Detect Pins
NC	No Connect
GND	Ground
VCC	Power Supply

Notes:

1. These pins are NC (No Connect on the PDM4M6124 and PDM4M6126.
2. Please consult the factory regarding module versions that support parity.

Presence Detect Table[1]

PD4	PD3	PD2	PD1	PD0	Size	Max[2]	Module
NC	NC	NC	NC	NC	—	—	No Cache Present
VCC	VCC	NC	NC	NC	64KB	8MB	—
VCC	VCC	NC	NC	VCC	128KB	16MB	—
VCC	VCC	NC	VCC	NC	256KB	32MB	—
VCC	VCC	NC	VCC	VCC	512K	64MB	—
VCC	NC	VCC	NC	NC	64KB	32MB	—
VCC	NC	VCC	NC	VCC	128KB	64MB	PDM4M6124
VCC	NC	VCC	VCC	NC	256KB	128KB	PDM4M6125
VCC	NC	VCC	VCC	VCC	512KB	128MB[3]	PDM4M6126

Notes:

1. Pins PD4-PD0 map directly to the 82424TX CDC Secondary Cache Control Register bits:
   PD4 – CP (Cache Present)
   PD3, PD2 – TAW (Tag Address Width)
   PD1, PD0 – SCS (Secondary Cache Size)
2. Maximum cacheable address space based on a 7- or 9-bit tag field
3. The maximum cacheable address space allowed by the core logic is 128MB.

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to Vcc +0.5	V
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
TA	Operating Temperature	0 to +70	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V

Capacitance[1,2] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Module[3]	Unit
CIN1	Input Capacitance, ($\overline{ALE}$, DIRTYIN, Dirty Control) VIN = 0V	12	pF
CIN2	Input Capacitance, ($\overline{WE}$) VIN = 0V	12/22/12	pF
CIN3	Input Capacitance, (A18-A4, Tag Control) VIN = 0V	22	pF
CIN4	Input Capacitance, ($\overline{CS}$, $\overline{OE}$, A2-x, A3-x) VIN = 0V	50	pF
CI/O1	Data I/O Capacitance, VOUT = 0V	14/25/14	pF
CI/O2	Tag I/O Capacitance, VOUT = 0V	12	pF
COUT	OutputCapacitance, VOUT = 0V	12	pF

NOTE: 1. This parameter is determined by device characteristics but is not production tested.
2. These parameters are maximum values.
3. The module specifications are for either 128KB/256KB/512KB versions respectively or all versions if the specification is a single number.

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage Current	VCC = Max.,VIN = GND to VCC	—	20	µA
ILI	Input Leakage Current ($\overline{CS}$, $\overline{OE}$, A2-x, A3-x)	VCC = Max., VIN = GND to VCC	—	40	µA
ILO	Output Leakage Current	VOUT = 0V to VCC, VCC = Max., $\overline{CS}$ ≥ VIH	—	20	µA
VOL	Output Low Voltage	IOL = 8 mA, VCC = Min.	—	0.4	V
VOH	Output High Voltage	IOH = –4 mA, VCC = Min.	2.4	—	V
VIH	Input High Voltage		2.2	6.0	V
VIL	Input Low Voltage		–0.5[1]	0.8	V

NOTE: 1. V_{IL} = –1.0V for pulse widths less than 5 ns, once per cycle.

Power Supply Characteristic

Symbol	Parameter	Max.	Unit
ICC	Operating Power Supply Current, Vcc = Max, $\overline{CS}$ ≤ VIL, f = fMAX, Outputs Open	1140	mA
ISB	Standby Supply Current Vcc = Max, $\overline{CS}$ ≥ VIH, f = fMAX, Outputs Open	445	mA
ISB1	Full Standby Supply Current $\overline{CS}$ ≥ Vcc – 0.2V, f = 0, Vin > Vcc – 0.2V or < 0.2V	205	mA

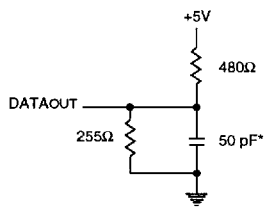
AC Electrical Characteristics (Vcc = 5V ± 5%, T_A = 0°C to +70°C)

Symbol	Parameter	PDM4M6124/6125/6126						Unit
		Data		Tag		Dirty		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	30	—	30	—	30	—	ns
t_{AA} A2-A3	Address Access Time	—	18	—	—	—	—	ns
t_{AA} A16-A4(3)	Address Access Time	—	30	—	12(2)	—	28	ns
t_{ACS}	Chip Select Access Time	—	18	—	12	—	30	ns
t_{OE}	Output Enable to Output Valid	—	15	—	10	—	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	15	—	10	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	15	—	10	—	—	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	30	—	30	—	30	—	ns
t_{WP}	Write Pulse Width	13	—	13	—	13	—	ns
t_{CW}	Chip Select to End of Write	20	—	20	—	20	—	ns
t_{AW} A16-A4	Address Valid to End of Write	23	—	20	—	23	—	ns
t_{AS} A16-A4	Address Setup Time	10	-	2	—	10	—	ns
t_{AS} A2-A3	Address Setup Time	2	-	—	—	—	—	ns
t_{DS}	Data Setup to Write Time	11	—	13	—	13	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns

NOTES 1. This parameter is determined by device characteristics but is not production tested.
2. Preliminary specifications only.

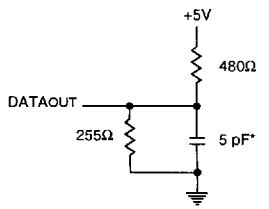
AC Test Conditions - 5V Power Supply

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



* Including scope and jig capacitances

Figure 1. Output Load

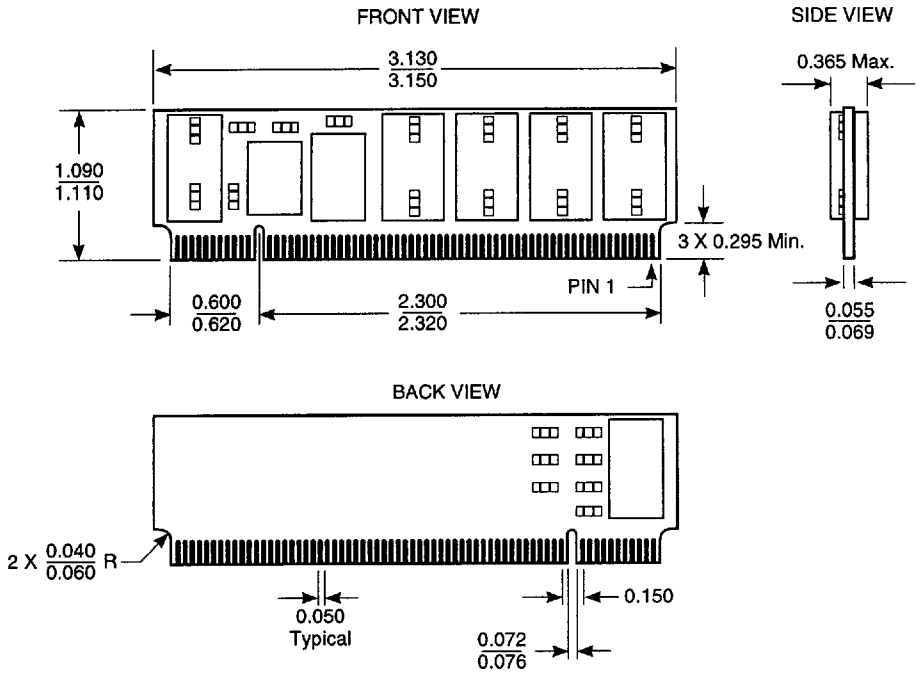


* Including scope and jig capacitances

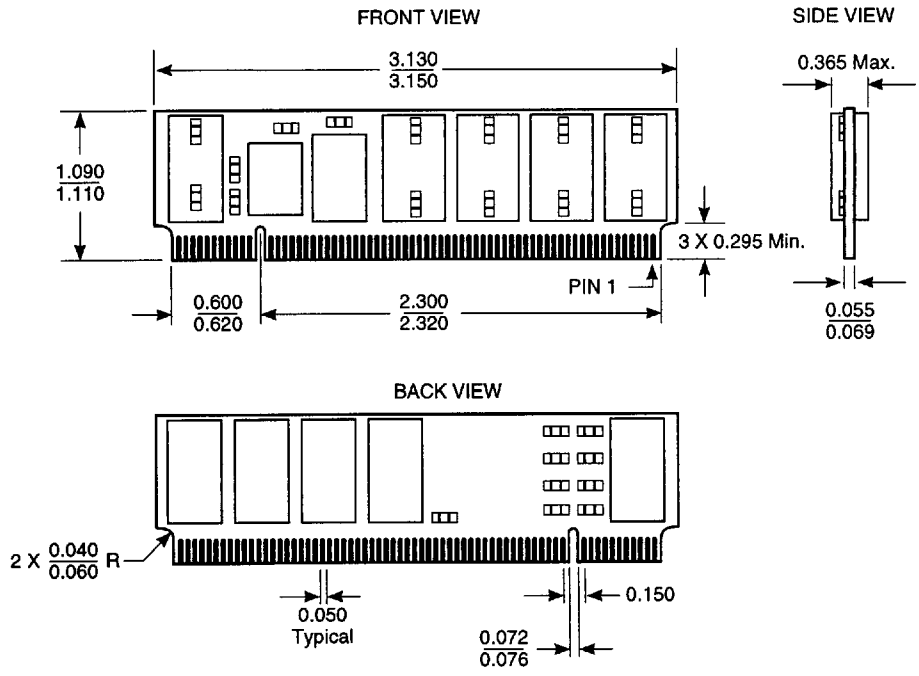
Figure 2. Output Load
(for tOHZ, tCHZ, tOLZ, and tCLZ)

Package Dimensions

PDM4M6124

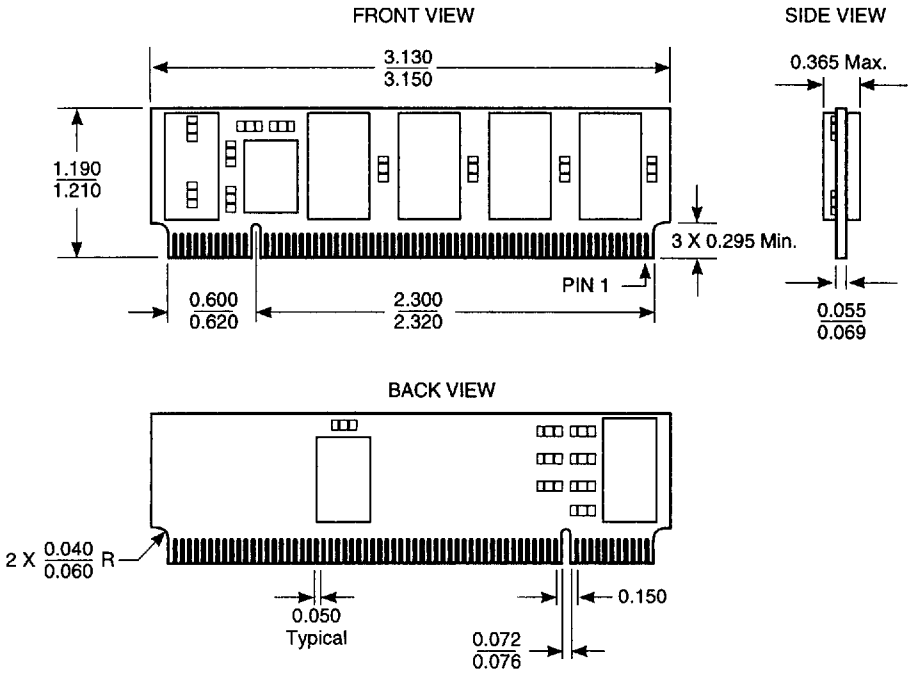


PDM4M6125



Package Dimensions

PDM4M6126



Ordering Information

PDM4M XXXX S XX X X

Device	Power	Speed	Package	Temp	
				Blank	Commercial (0 to 70°C)
			M		112 lead Module, Card Edge Low Profile (CELP)
		33			Speed in Megahertz
	S				Standard Power
6124					128KB Secondary Cache Module – 9-bit Tag
6125					256KB Secondary Cache Module – 9-bit Tag
6126					512KB Secondary Cache Module – 9-bit Tag

Advanced Packaging

Advances in packaging techniques permit a wide variety of solutions to board space problems.

Modules are comprised of individual semiconductor devises with other support devises, such as decoders and capacitors as required, mounted on a multilayer substrate. The substrate is custom designed to provide appropriate circuitry for the components in a package configuration that meets thermal and mechanical design objectives in a minimal amount of board real estate. The final module may have a through-hole pin configuration or may be surface mountable device.

Commercial modules are generally developed using components encapsulated in plastic, surface mounted on FR4 epoxy laminate substrates. The surface mountable component packages may be SOJ, SOIC, VSOP, TSOP, or QFP styles.

Ceramic packaging may be used for devices that need to be hermetic or require extended temperature range performance, such as military applications. Ceramic modules may use LCC or CSOJ component packaging on ceramic substrates with sidebrazed lead attach, or may use multiple die bonded in an MCM-C package.

Module Package Styles

Many module package styles are available from Paradigm. Features and relative board space are described here.

SIP

Vertically mounted, the SIP (Single In-line Package) contains a single row of pins along on edge for through-hole assembly. Pins are on a 100-mil pitch. Components may be mounted on both sides of the substrate. The device is most commonly constructed using plastic encapsulated components on an FR4 substrate, but it may be constructed of ceramic, as well. The vertical orientation and the ability to mount components on both sides of the substrate adds up to exceptional density.

ZIP

ZIP (Zig-zag In-line Package) is similar in space savings to the SIP, since both feature vertical substrate configurations. They also feature the additional advantages of larger pin counts with the structural stability of two rows of pins. Pins are placed on a 100-mil pitch, with 100-mil spacing between the rows.

SIMM

The SIMM (Single In-line Memory Module) package is similar to the SIP. The major difference is, rather than a single row of pins, the bottom edge has a row of connector contacts that are designed to plug into a socket mounted on the motherboard. Spacing between contacts is either 50- or 100-mil pitch. Since socket mounted SIMMs may be changed easily, they offer greater system flexibility by allowing multiple densities and speed grades.

CELP/DIMM

Like the SIMM, the DIMM (Dual readout In-line Memory Module) is socket mounted, but its dual readout contains larger pinouts for extremely high density in a compact component.

DIP

DIP (Dual In-line Package) modules offer a low profile with excellent mechanical ruggedness. Historically, DIP modules have provided the same form, fit, and function as future generation memory devices. Ceramic DIP modules have also been the preferred package for military applications.

PGA

The PGA (Pin Grid Array) has an array of pins arranged in a matrix on a 100-mil grid. This ceramic package style provides a large pin count in a smaller area than possible in package styles with pins only on the package edge or perimeter. With its large number of through-hole contract points, it offers exceptional structural integrity. This package style is also commonly used for multichip arrays bonded within a single cavity.