54AC/74AC568 • 54AC/74AC569
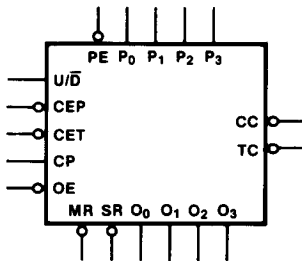## 4-Bit Bidirectional Counters With 3-State Outputs

Description

The 'AC568 and 'AC569 are fully synchronous, bidirectional counters with 3-state outputs. The 'AC568 is a BCD decade counter; the 'AC569 is a modulo 16 binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high-impedance state but does not prevent counting, resetting or parallel loading.

- **Synchronous Counting and Loading**
- **Lookahead Carry Capability for Easy Cascading**
- **Preset Capability for Programmable Operation**
- **3-State Outputs for Bus Organized Systems**
- **Outputs Source/Sink 24 mA**
- **Synchronous and Asynchronous Resets**

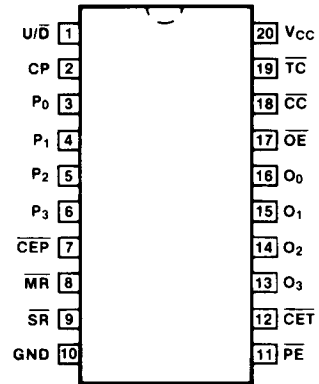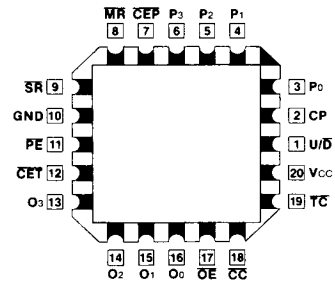**Ordering Code:** See Section 6

Logic Symbol

Connection Diagrams

**Pin Assignment
for DIP, Flatpak and SOIC**

**Pin Assignment
for LCC and PCC**

Pin Names

|			
P_0 - P_3	Parallel Data Inputs	$\overline{OE}$	Output Enable Input
$\overline{CEP}$	Count Enable Parallel Input	$\overline{MR}$	Master Reset Input
$\overline{CET}$	Count Enable Trickle Input	$\overline{SR}$	Synchronous Reset Input
CP	Clock Pulse Input	O_0 - O_3	3-State Parallel Data Outputs
$\overline{PE}$	Parallel Enable Input	$\overline{TC}$	Terminal Count Output
U/$\overline{D}$	Up/Down Count Control Input	$\overline{CC}$	Clocked Carry Output

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Logic Diagram ('AC568)
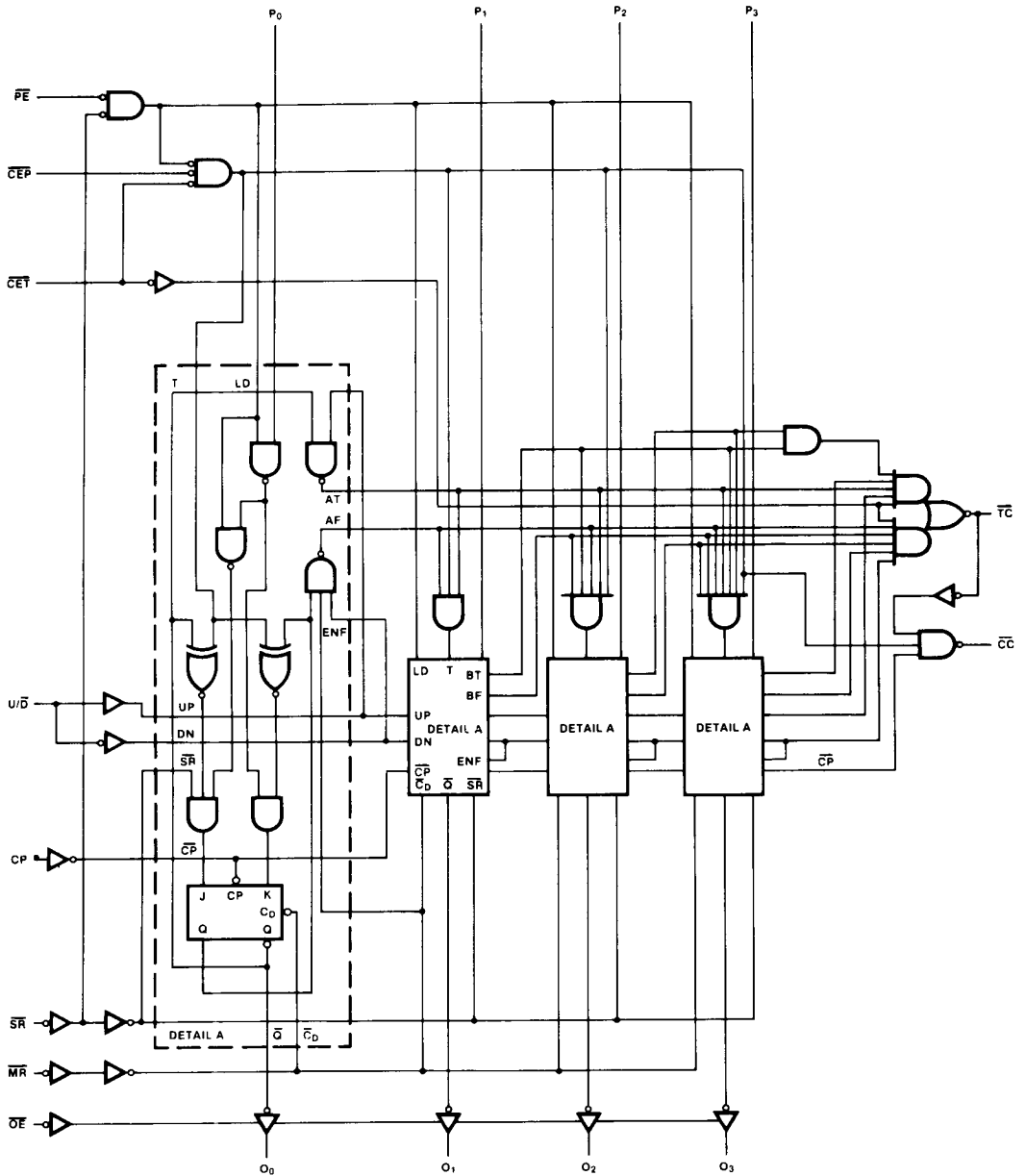
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.
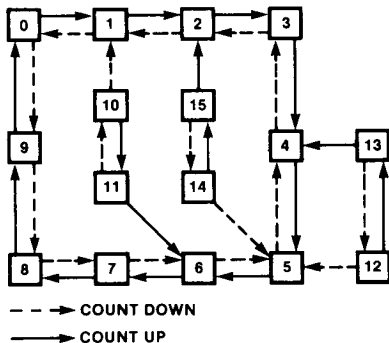
Logic Diagram ('AC569)
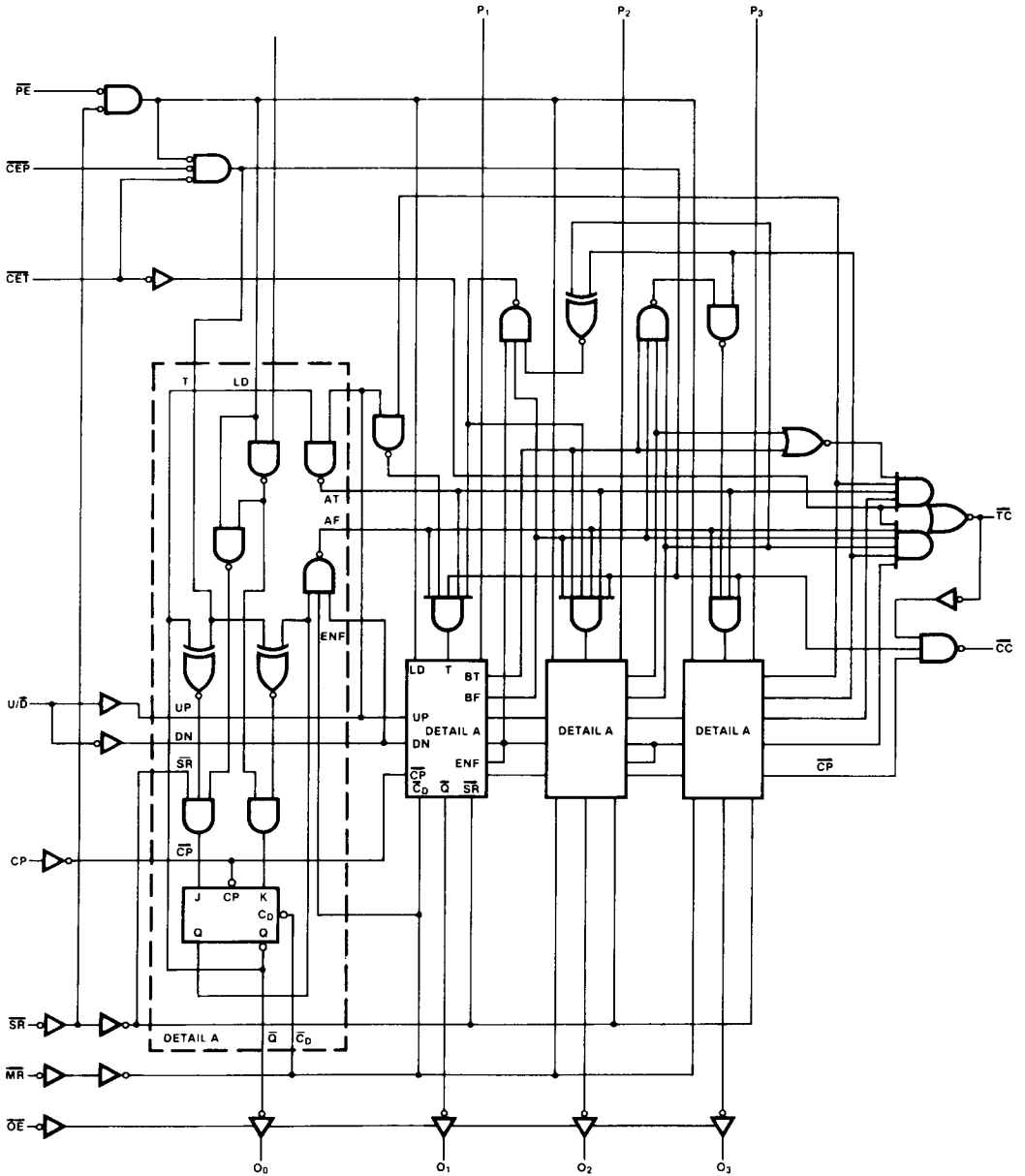
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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State Diagrams

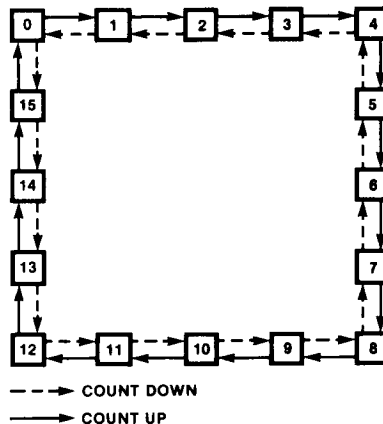### 'AC568


```
- - -▶ COUNT DOWN
———▶ COUNT UP
```

'AC569


```
- - -▶ COUNT DOWN
———▶ COUNT UP
```

Logic Equations:

Count Enable $= \overline{CEP} \bullet \overline{CET} \bullet PE$

Up ('AC568): $\overline{TC} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

('AC569): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

Down (Both): $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

Functional Description

The 'AC568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The 'AC569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs—Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle ($\overline{CET}$)—plus the Up/Down (U/$\overline{D}$) input determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (Pn) inputs

to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The 'AC568 and 'AC569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the 'AC568, 15 for the 'AC569) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure a shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative

CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure b are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 ('AC568) or 16 ('AC569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry (CC) output is provided. The CC output is normally HIGH. When SR and PE are HIGH, and CEP, CET and TC are LOW, the CC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the CC Truth Table. When the Output Enable (OE) is LOW, the parallel data outputs $O_0 - O_3$ are active and follow the flip-flop Q outputs. A HIGH signal on OE forces $O_0 - O_3$ to the high-Z state but does not prevent counting, loading or resetting.

Mode Select Table

Inputs						Operating Mode
MR	SR	PE	CEP	CET	U/D	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

CC Truth Table

Inputs						Output
SR	PE	CEP	CET	TC*	CP	CC
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊔	⊔

* = TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
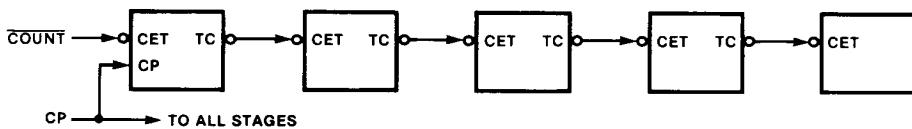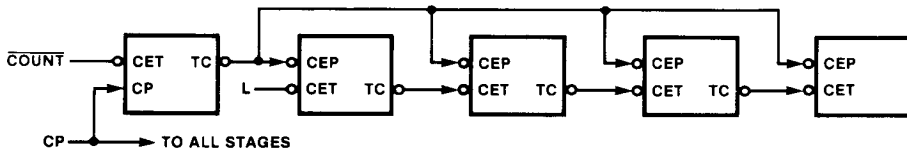X = Immaterial

Figure a: Multistage Counter with Ripple Carry

Figure b: Multistage Counter with Lookahead Carry

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
Icc	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A =$ Worst Case
Icc	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF Min	Typ	Max	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF Min	Max	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	Max	Units	Fig. No.
fmax	Maximum Clock Frequency	3.3 5.0		87 117						MHz	3-3
tPLH	Propagation Delay CP to On (PE HIGH or LOW)	3.3 5.0		10.0 7.5						ns	3-6
tPHL	Propagation Delay CP to On (PE HIGH or LOW)	3.3 5.0		11.0 8.0						ns	3-6
tPLH	Propagation Delay CP to TC	3.3 5.0		16.5 12.0						ns	3-6
tPHL	Propagation Delay CP to TC	3.3 5.0		16.5 12.0						ns	3-6
tPLH	Propagation Delay CET to TC	3.3 5.0		10.5 7.5						ns	3-6
tPHL	Propagation Delay CET to TC	3.3 5.0		10.0 7.0						ns	3-6
tPLH	Propagation Delay U/D to TC ('568)	3.3 5.0		10.5 7.5						ns	3-6
tPHL	Propagation Delay U/D to TC ('568)	3.3 5.0		9.0 6.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
 Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics (cont'd)

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay U/D to TC ('569)	3.3 5.0		10.5 7.5						ns	3-6
tPHL	Propagation Delay U/D to TC ('569)	3.3 5.0		9.0 6.5						ns	3-6
tPLH	Propagation Delay CP to CC	3.3 5.0		11.0 8.0						ns	3-6
tPHL	Propagation Delay CP to CC	3.3 5.0		9.5 7.0						ns	3-6
tPLH	Propagation Delay CEP or CET to CC	3.3 5.0		9.5 7.0						ns	3-6
tPHL	Propagation Delay CEP or CET to CC	3.3 5.0		9.5 7.0						ns	3-6
tPHL	Propagation Delay MR to On	3.3 5.0		12.5 9.0						ns	3-6
tPZH	Output Enable Time OE to On	3.3 5.0		7.5 5.5						ns	3-7
tPZL	Output Enable Time OE to On	3.3 5.0		7.5 5.5						ns	3-8
tPHZ	Output Disable Time OE to On	3.3 5.0		9.5 7.0						ns	3-7
tPZL	Output Disable Time OE to On	3.3 5.0		11.0 8.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
 Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
ts	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	8.0 6.0			ns	3-9
th	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	0 0			ns	3-9
ts	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	3.3 5.0	8.0 12.5			ns	3-9
th	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	3.3 5.0	0 0			ns	3-9
ts	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	12.5 9.0			ns	3-9
th	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	0 0			ns	3-9
ts	Setup Time, HIGH or LOW $U/\overline{D}$ to CP ('568)	3.3 5.0	12.5 9.0			ns	3-9
ts	Setup Time, HIGH or LOW $U/\overline{D}$ to CP ('569)	3.3 5.0	12.5 9.0			ns	3-9
th	Hold Time, HIGH or LOW $U/\overline{D}$ to CP	3.3 5.0	0 0			ns	3-9
ts	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	4.0 3.0			ns	3-9
th	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	-1.5 -1.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
 Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements (cont'd)

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
tw	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 3.0			ns	3-6
tw	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.0 3.0			ns	3-6
trec	$\overline{MR}$ Recovery Time	3.3 5.0	4.0 3.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
 Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V