

74LCX162841 Low-Voltage 20-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX162841 contains twenty non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state. The 30Ω-series resistor helps reducing output overshoot and undershoot.

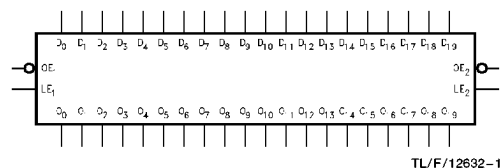
The LCX162841 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX162841 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- 30Ω-series resistor on outputs
- Support live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±12 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 162841
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

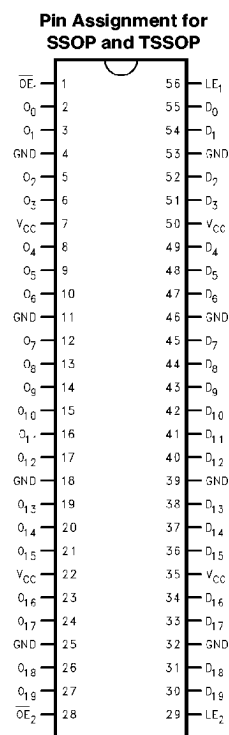
Logic Symbol



Pin Names	Description
\overline{OE}_n	Output Enable Input (Active Low)
LE_n	Latch Enable Input
D_0-D_{19}	Inputs
O_0-O_{19}	Outputs

	SSOP	TSSOP
Order Number	74LCX162841MEA 74LCX162841MEAX	74LCX162841MTD 74LCX162841MTDX
See NS Package Number	MS56A	MTD56

Connection Diagram



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Functional Description

The LCX162841 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LE_n is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE_n . The TRI-STATE standard outputs are controlled by the Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the standard outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

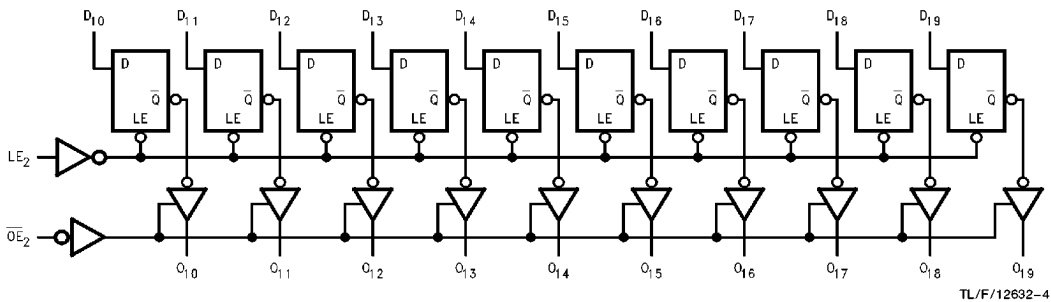
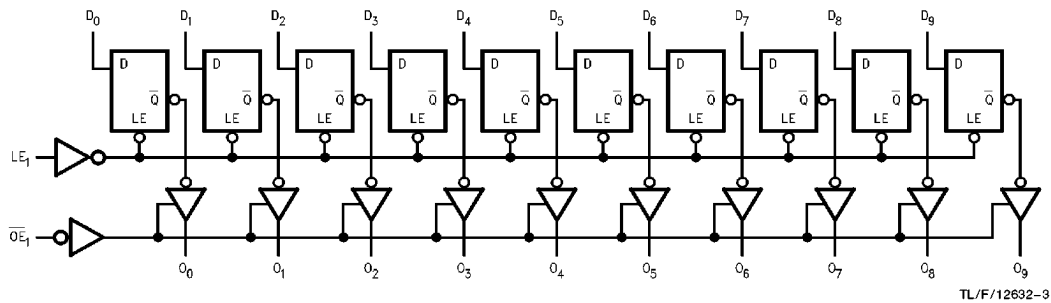
Truth Tables

Inputs			Outputs
LE_1	\overline{OE}_1	D_0-D_9	O_0-O_9
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
LE_2	\overline{OE}_2	$D_{10}-D_{19}$	$O_{10}-O_{19}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
 L = Low Voltage Level
 X = Immaterial
 Z = High Impedance
 O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	-0.5 to +7.0		V
V _I	DC Input Voltage	-0.5 to +7.0		V
V _O	DC Output Voltage	-0.5 to +7.0	Output in TRI-STATE	V
		-0.5 to V _{CC} + 0.5	Output in High or Low State (Note 2)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	-65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

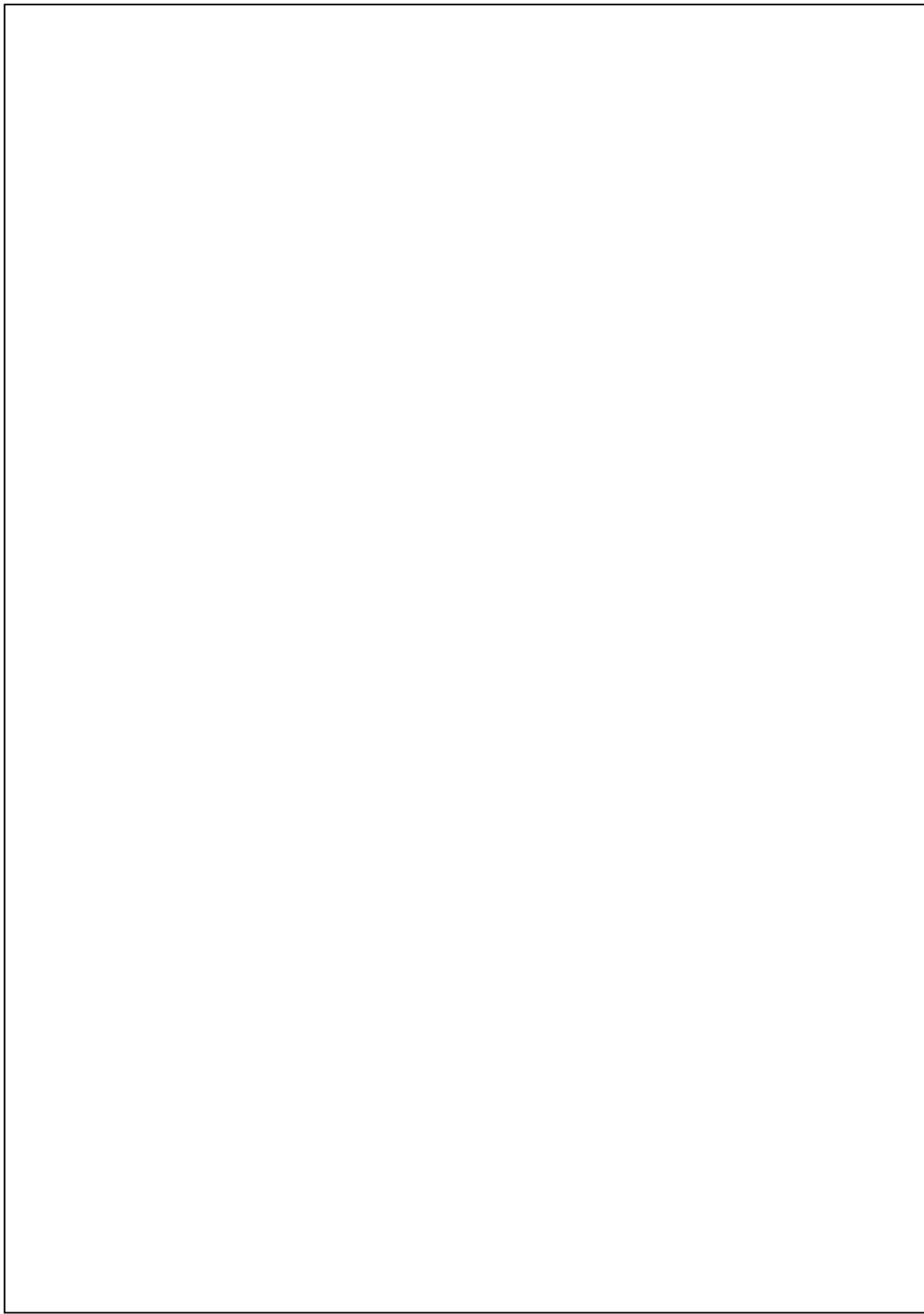
Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

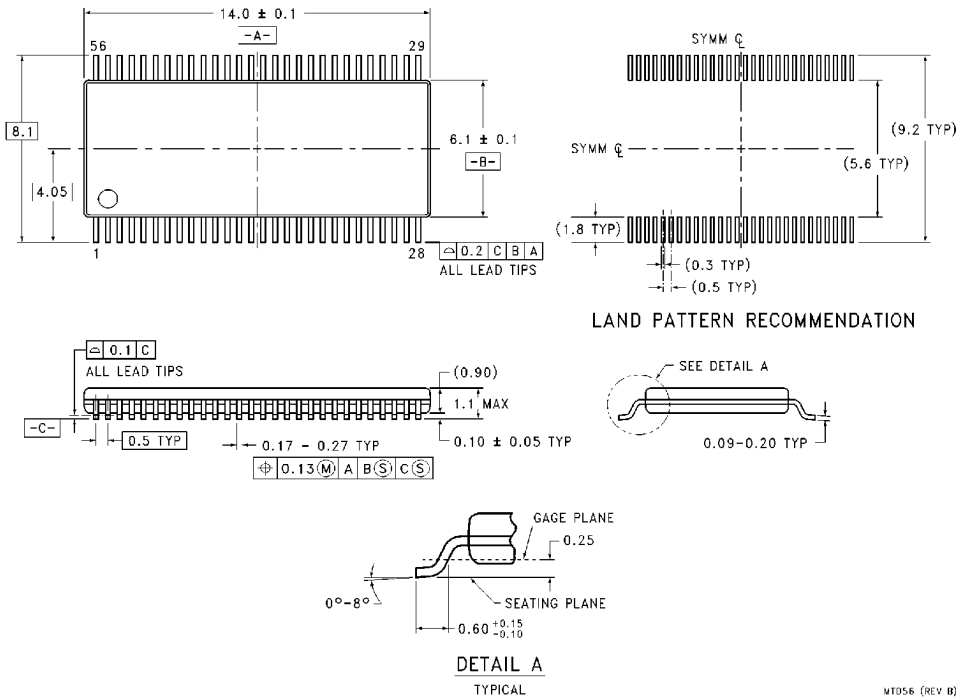
Symbol	Parameter	Min	Max	Units	
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V _I	Input Voltage	0	5.5	V	
V _O	Output Voltage	HIGH or LOW State	0	V _{CC}	V
		TRI-STATE	0	5.5	
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V-3.6V V _{CC} = 2.7V		±12 ±6	mA
T _A	Free-Air Operating Temperature	-40	85	°C	
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V-2.0V, V _{CC} = 3.0V	0	10	ns/V	

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.7-3.6	2.0		V
V _{IL}	LOW Level Input Voltage		2.7-3.6		0.8	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = -12 mA	3.0	2.0		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 12 mA	3.0		0.8	V
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.7-3.6		±5.0	μA
I _{OZ}	TRI-STATE Output Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.7-3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.7-3.6		20	μA
		3.6V ≤ V _I , V _O ≤ 5.5V	2.7-3.6		±20	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7-3.6		500	μA



Physical Dimensions All dimensions are in millimeters (Continued)



**Order Number 74LCX162841MTD or 74LCX162841MTDX
NS Package Number MTD56**

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