Integrated Device Technology, Inc.

CMOS MICROCYCLE LENGTH CONTROLLER

IDT49C25
IDT49C25A

FEATURES:

- Similar function to AMD's Am2925 bipolar controller with improved speeds and output drive over full temperature and voltage supply extremes
- Four microcode-controlled clock outputs allow clock cycle length control for 15 to 30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- System controls for $\overline{RUN}/\overline{HALT}$ and Single Step
  — Switch-debounced inputs provide flexible halt controls
- Low input/output capacitance
  — 6pF inputs (typ.)
  — 8pF outputs (typ.)
- CMOS power levels (1mW typ. static)
- Available in 300 mil 24-pin plastic and ceramic THINDIP, 28-pin LCC and PLCC packages and CERPACK
- Both CMOS and TTL output compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

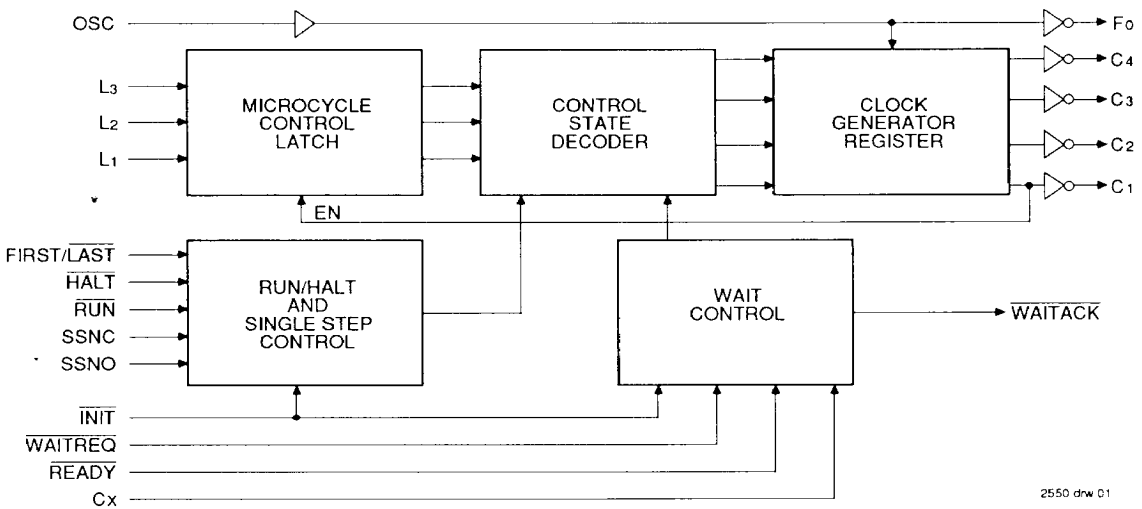
The IDT49C25/A are single-chip general purpose clock generator/drivers built using IDT's advanced CEMOS™, a dual metal CMOS technology. It has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meets a variety of system speed requirements.

The IDT49C25/A generate four different simultaneous clock out-put waveforms tailored to meet the needs of the IDT3900 CMOS family and other MOS and bipolar microprocessor-based systems. One of eight cycle lengths may be generated under microprogram control using the cycle length inputs, L_1, L_2 and L_3.

A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs, C_1, C_2, C_3 and C_4.

System control functions include $\overline{RUN}$, $\overline{HALT}$, Single-Step, Initialize and Ready/Wait controls. In addition, the $\overline{FIRST}/\overline{LAST}$ input determines where a halt occurs and the C_x input determines the end point timing of wait cycles. $\overline{WAITACK}$ indicates that the IDT49C25/A are in a wait state.

FUNCTIONAL BLOCK DIAGRAM



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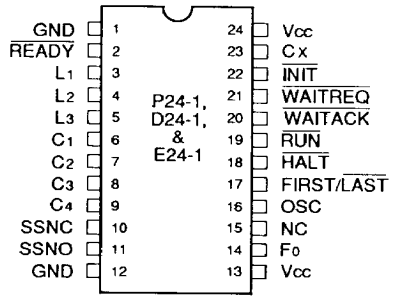
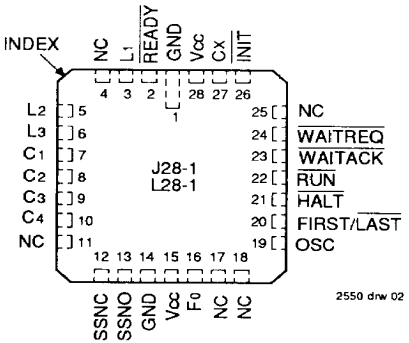
PIN CONFIGURATIONS



DIP/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

Pin Names	I/O	Description
C_1, C_2, C_3, C_4	O	System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls: L_1, L_2 and L_3.
L_1, L_2, L_3	I	Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.
F_0	O	The buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{WAITACK}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.
$\overline{HALT}$ and $\overline{RUN}$	I	Debounced inputs to provide $\overline{HALT}$ control. These inputs determine whether the output clocks run or not. A LOW input on $\overline{HALT}$ ($\overline{RUN}$ = HIGH) will stop all clock outputs.
FIRST/$\overline{LAST}$	I	$\overline{HALT}$ time control input. A HIGH input in conjunction with a $\overline{HALT}$ command will cause a halt to occur when C_4 = LOW and C_1 = C_2 = C_3 = HIGH (see clock waveforms). A LOW input causes a $\overline{HALT}$ to occur when C_1 = C_2 = C_3 = LOW and C_4 = HIGH.
SSNO and SSNC	I	Single Step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{HALT}$ is activated LOW.
$\overline{WAITREQ}$	I	The Wait Request active LOW input. When LOW, this input will cause the outputs to halt during the next oscillator cycle after the Cx input goes LOW.
Cx	I	Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after Cx goes LOW. Cx is normally tied to any one of C_1, C_2, C_3 or C_4.
$\overline{WAITACK}$	O	The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state.
$\overline{READY}$	I	The $\overline{READY}$ active LOW input is used to continue normal clock output patterns after a wait state.
$\overline{INIT}$	I	The Initialize active LOW input. This input is intended for use during power-up initialization of the system. When LOW, all clock outputs run free regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.
OSC	I	External oscillator input (TTL level input).

2550 tbl 01

6

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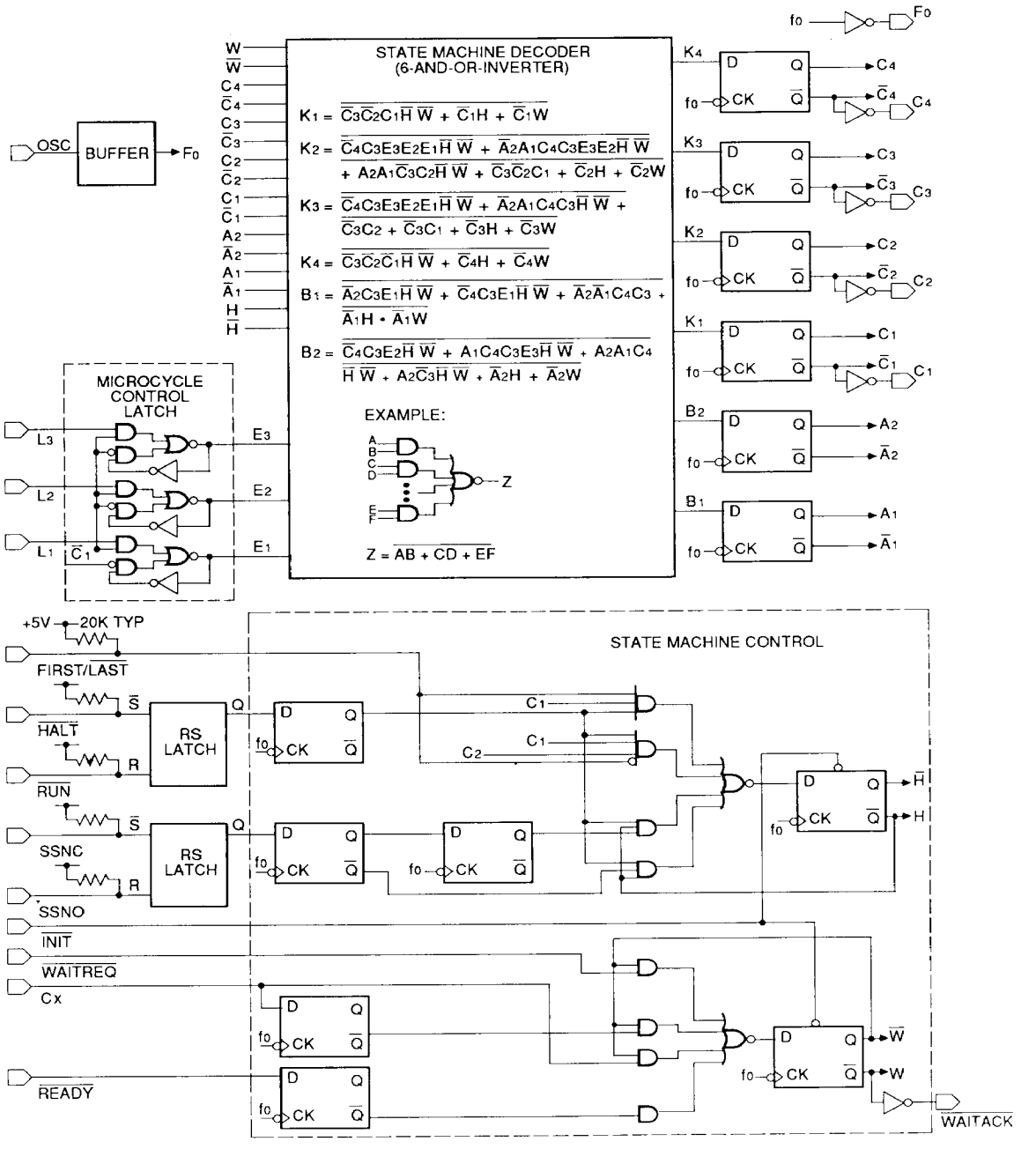
LOGIC DIAGRAM



2550 drw 03

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2550 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2550 tbl 03

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc - 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max., V_{IN} = Vcc		—	—	25	µA
I_{IL}	Input LOW Current	Vcc = Max.	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$	—	—	-1.0	mA
		V_{IN} = GND	FIRST/$\overline{LAST}$	—	—	-1.5	
			Other Inputs	—	—	-5	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = -18mA		—	-0.7	-1.2	mA
I_{SC}	Short Circuit Current	Vcc = Max.[3], V_O = GND		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH}= -300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA MIL.	2.4	4.0	—	
			I_{OH}= -5.0mA COM'L	2.4	4.0	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL.	—	—	0.5	
			I_{OL} = 24mA COM'L	—	—	0.5	

NOTES: 2550 tbl 04

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circiut test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{IN} \geq V_{HC}$, $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.24	0.4	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max., Outputs Open, f_{CP} = OSC = 5MHz (50% duty cycle) $\overline{READY}$, SSNO, $\overline{WAITREQ}$, $\overline{HALT}$, $\overline{INIT}$ = V_{CC} L_1, L_2, L_3, SSNC, FIRST/$\overline{LAST}$, $\overline{RUN}$, Cx = GND		—	6.5	9.7	mA
		V_{CC} = Max. Outputs Open f_{CP} = OSC = 5MHz (50% duty cycle) SSNO, $\overline{HALT}$ = V_{CC} $\overline{READY}$, $\overline{WAITREQ}$, $\overline{INIT}$ = 3.4V (98% duty cycle) L_1, L_2, L_3, SSNC, FIRST/$\overline{LAST}$, $\overline{RUN}$, Cx = GND		—	8.5	16.6	

2550 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_0 N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_0 = Output Frequency
   N_O = Number of Outputs at f_0
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

				IDT49C25				IDT49C25A				
				Com'l.		Mil.		Com'l.		Mil.		
	Symbol	Parameter	Condition	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
1	f_{MAX1}	F_O Frequency (C_x Connected)[1, 6]	C_L = 50pF R_L = 500Ω	31	—	31	—	40	—	40	—	MHz
2	f_{MAX2}	F_O Frequency (C_x = HIGH)[6]		—	—	—	—	—	—	—	—	MHz
3	t_{OFFSET}	F_O (↗) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↗)		—	8.5	—	8.5	—	6.0	—	6.0	ns
4	t_{OFFSET}	F_O (↗) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↘)		—	17	—	18	—	11.5	—	12	ns
5	t_{SKEW}	C_1 (↗) to C_2 (↗)		—	2	—	2	—	1.5	—	1.5	ns
6	t_{SKEW}	C_1 (↗) to C_3 (↗)		—	2	—	2	—	1.5	—	1.5	ns
7	t_{SKEW}	C_1 (↗) to C_4 (↘) Opposite Transition		—	11	—	11	—	8.0	—	8.0	ns
8	t_{SU}	L_1, L_2, L_3, to C_1 (↗)		6	—	6	—	5	—	5	—	ns
9	t_H	L_1, L_2, L_3, to C_1 (↗)		8	—	8	—	6	—	6	—	ns
10	t_{SU}	Cx to F_O (↗)[2]		18	—	18	—	12	—	12	—	ns
11	t_H	Cx to F_O (↗)[2]		0	—	0	—	0	—	0	—	ns
12	t_{SU}	$\overline{WAITREQ}$ to F_O (↗)[3]		18	—	18	—	12	—	12	—	ns
13	t_H	$\overline{WAITREQ}$ to F_O (↗)[3]		0	—	0	—	0	—	0	—	ns
14	t_{SU}	$\overline{READY}$ to F_O (↗)[3]		18	—	18	—	12	—	12	—	ns
15	t_H	$\overline{READY}$ to F_O (↗)[3]		0	—	0	—	0	—	0	—	ns
16	t_{SU}	$\overline{RUN}$, $\overline{HALT}$ (↗) to F_O (↗)[3,4]		18	—	18	—	12	—	12	—	ns
17	t_{SU}	SSNC, SSNO to F_O (↗)[3,4]		18	—	18	—	12	—	12	—	ns
18	t_{SU}	FIRST/$\overline{LAST}$ to F_O (↗)[5]		18	—	18	—	12	—	12	—	ns
19	t_{SU}	$\overline{INIT}$ (↗) to F_O (↗)[3]		18	—	18	—	12	—	12	—	ns
20	t_W	$\overline{INIT}$ LOW Pulse Width		20	—	25	—	18	—	23	—	ns
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$		—	25	—	27	—	16	—	18	ns
22	t_{PLH}	OSC to F_O		—	13	—	16	—	8.5	—	10.5	ns
23	t_{PHL}			—	13	—	16	—	8.5	—	10.5	ns

2550 tbl 06

NOTES:
1. The frequency guarantees apply with C_x connected to C_1, C_2, C_3, C_4 or HIGH. The Cx input load must be considered part of the 50pf/500Ω clock output loading.
2. These set-up and hold times apply to the F_O LOW-to-HIGH transition of the period in which Cx goes LOW.
3. These inputs are synchronized internally. Failure to meet ts may cause a 1/F_O delay but will not cause incorrect operation.
4. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
5. FIRST/$\overline{LAST}$ normally wired HIGH or LOW.
6. This parameter is guaranteed but not tested.

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SWITCHING WAVEFORMS

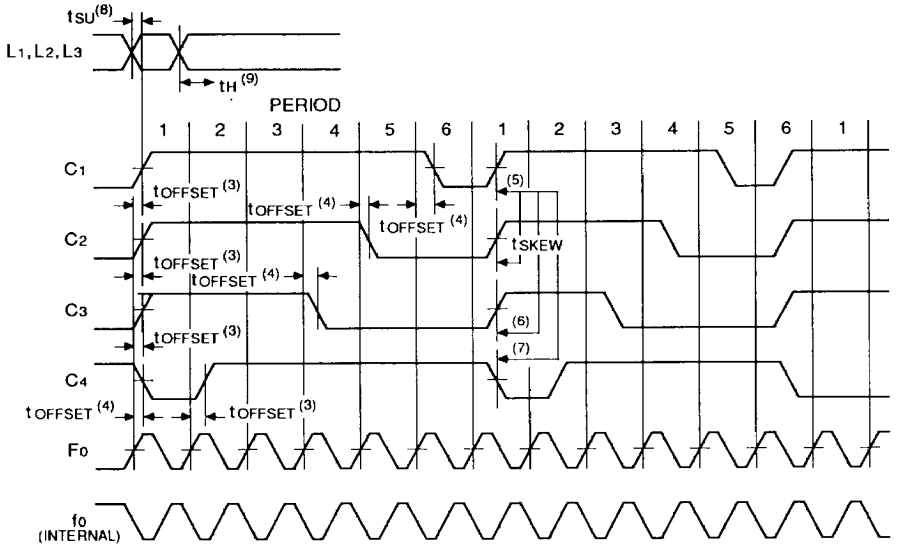

Figure 2. Normal Cycle Without Wait States (Pattern F6 Shown)

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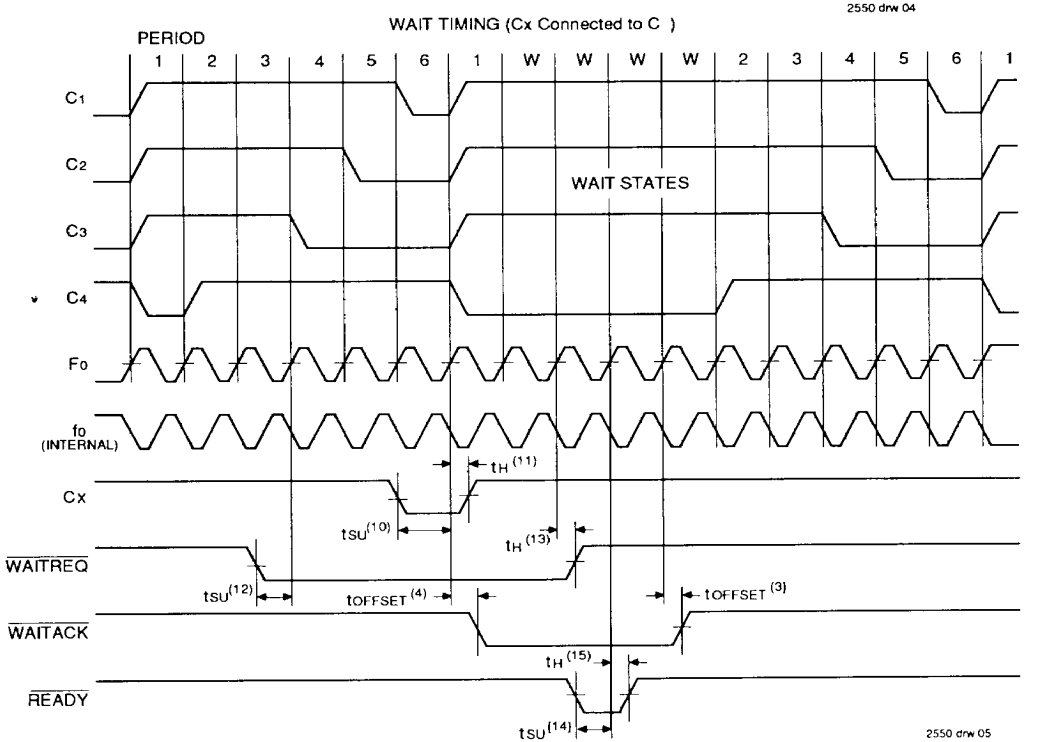

Figure 3. Wait Timing (CX Connected to C1)

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DETAILED DESCRIPTION

The IDT49C25/A are dynamically programmable general-purpose clock controllers. They can be logically separated into two parts — a state machine decoder and a state machine control section.

The state machine takes microcode information from the Microcycle Length (L) inputs L_1, L_2 and L_3 and counts the fundamental frequency of the oscillator (OSC) to create the clock outputs F_0, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape

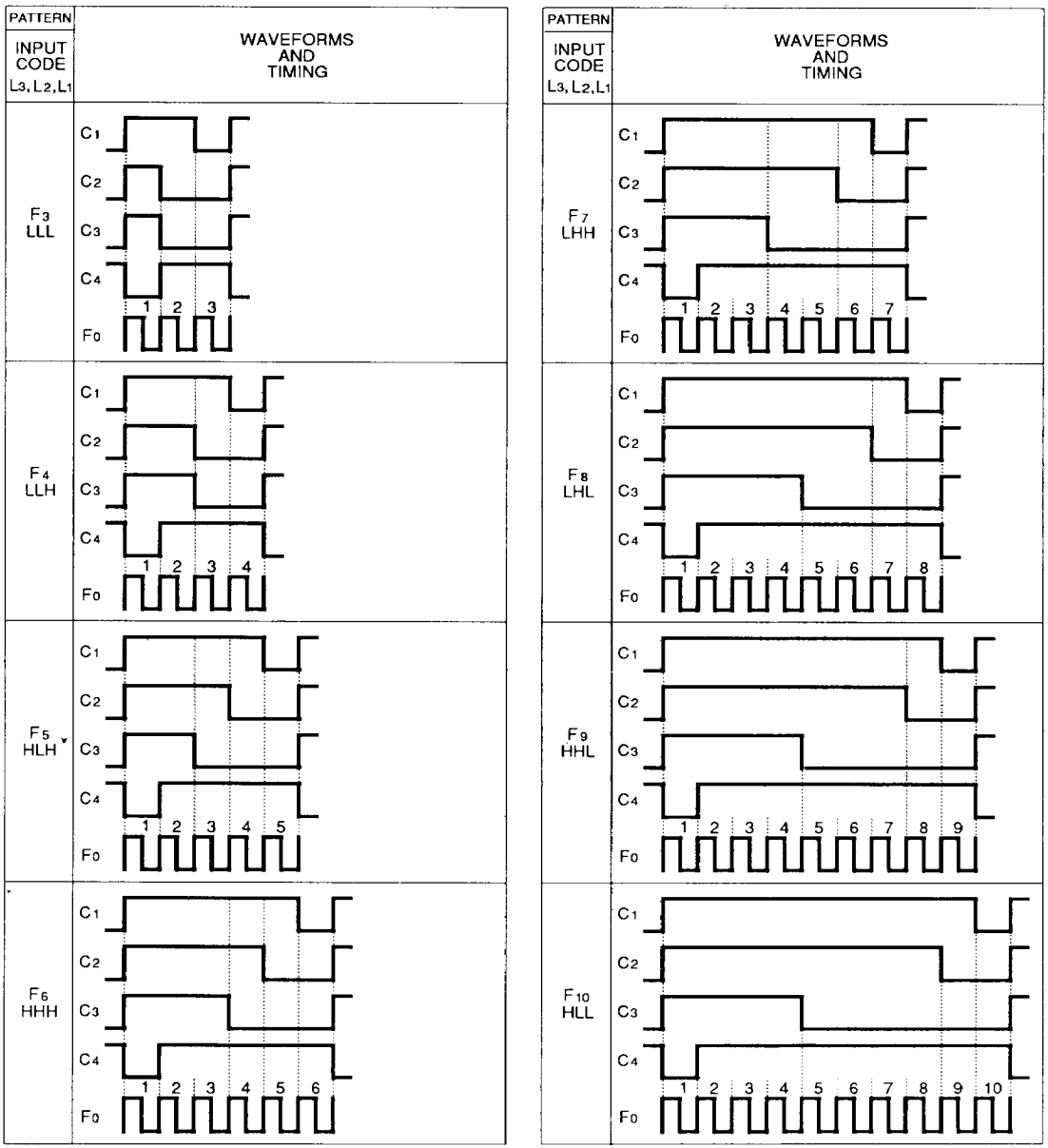

Figure 4. IDT49C25/A Clock Waveforms

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relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle and C_4 is always LOW on the first. C_3 has an approximate duty cycle of 50% and C_2 is HIGH for all but the last two periods (see Figure 4).

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into combinatorial logic to generate the next state. On each falling edge of the internal clock, the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle ($C_1 = C_2 = C_3$ = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the IDT49C25/A comprised of $\overline{RUN}$, $\overline{HALT}$, $\overline{WAIT}$ and SINGLE STEP.

SYSTEM TIMING

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The IDT49C25/A allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

IDT49C25/A CONTROL INPUTS

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which are intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch which performs the function of a pipeline register for the microcycle length microcode bits.

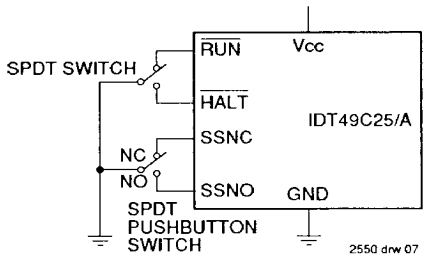

Figure 5. Switch Connection for $\overline{RUN}$/$\overline{HALT}$ and Single Step

Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{RUN}$, $\overline{HALT}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 5). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{LAST}$ input is used to determine at what point of the microcycle the IDT49C25/A will halt when $\overline{HALT}$ or a SINGLE STEP is initiated. In most applications, the user wires this input HIGH or LOW, depending on the design.

When $\overline{HALT}$ is held low ($\overline{RUN}$ = HIGH), the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/$\overline{LAST}$ input. When $\overline{RUN}$ goes low ($\overline{HALT}$ = HIGH), the state machine will resume the run mode.

The $\overline{WAITREQ}$, Cx, $\overline{READY}$ and $\overline{WAITACK}$ signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the date bus for several microseconds. In this case, the peripheral pulls the $\overline{WAITREQ}$ line LOW. The Cx input lets the design specify when the $\overline{WAITREQ}$ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to

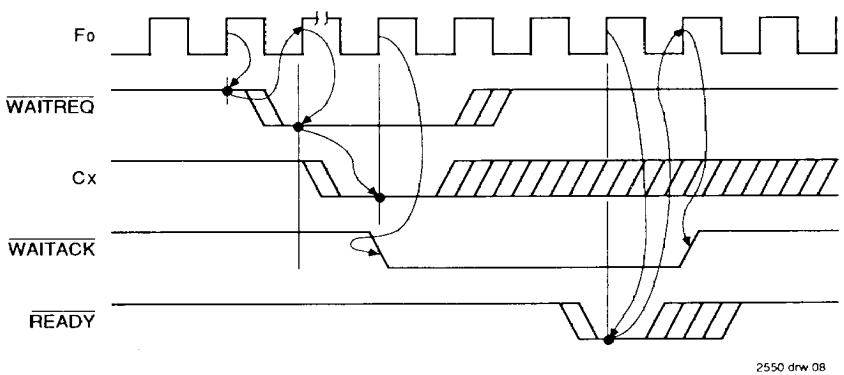

Figure 6. $\overline{WAIT}$/$\overline{READY}$ Timing

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respond in order to request a wait cycle (see Figure 6). The $\overline{READY}$ line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The $\overline{WAITACK}$ line goes LOW on the next oscillator cycle after the Cx input goes LOW and remains LOW until the second oscillator cycle after $\overline{READY}$ goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been high for one clock edge, the state machine will change to the next run mode. The microcycle will end on the first or last state of the microcycle, depending on the state of the FIRST/$\overline{LAST}$.

AC TIMING SIGNAL REFERENCES

Set-up and hold times in registers and latches are measured relative to the clock signals that drive them. In the IDT49C25/A, the external oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference of set-up, hold and clock-to-output times. However, for the Microcycle Control Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcycle Control Latch because, in a typical application, this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.

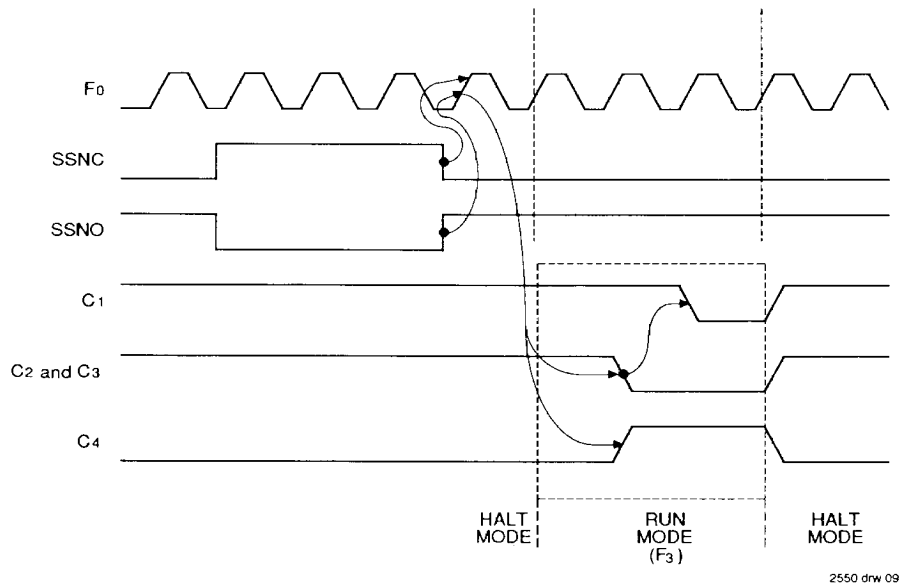

Figure 7. Single Step Timing Sequence

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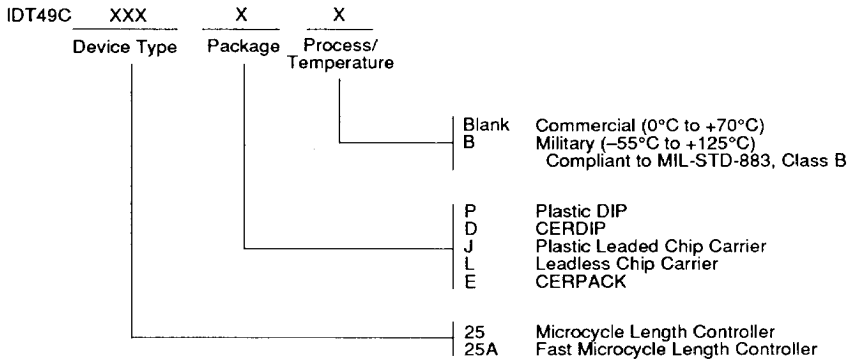
ORDERING INFORMATION



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