ICSSSTUAF32868B

Description

This 28-bit 1:2 configurable registered buffer is designed for 1.7V to 1.9V VDD operation. All inputs are compatible with the JEDEC standard for SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset ($\overline{\text{RESET}}$) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{\text{QERR}}$) output.

The ICSSSTUAF32868B operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high and $\overline{\text{CLK}}$ going low. The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (Vref) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low except $\overline{\text{QERR}}$. The LVCMOS $\overline{\text{RESET}}$ and C inputs must always be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up. In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the ICSSSTUAF32868B must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The ICSSSTUAF32868B includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. The corresponding $\overline{\text{QERR}}$ output signal for the data inputs is generated two clock cycles after the data, to which the $\overline{\text{QERR}}$ signal applies, is registered. The ICSSSTUAF32868B accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D1-D5, D7, D9-D12, D17-D28 when C = 0; or D1-D12, D17-D20, D22, D24-D28 when C = 1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. If a parity error occurs on the clock cycle before the device enters the low-power (LPM) and the $\overline{\text{QERR}}$ output is driven low, then it stays lateched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) are not included in the parity check computation.

The C input controls the pinout configuration from register-A configuration (when low) to register-B configuration (when high). The C input should not be switched during normal operation. It should be hardwired to a valid low or high level to configure the register in the desired mode. The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN, $\overline{\text{DCS0}}$, and $\overline{\text{DCS1}}$ inputs are high. If CSGEN, $\overline{\text{DCS0}}$ or$\overline{\text{DCS1}}$ input is low, the Qn outputs will function normally. Also, if both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs are high, the device will gate the $\overline{\text{QERR}}$ output from changing states. If either $\overline{\text{DCS0}}$ or$\overline{\text{DCS1}}$ is low, the $\overline{\text{QERR}}$ output will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and when driven low will force the Qn outputs low, and the $\overline{\text{QERR}}$ output high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ only, then the CSGEN input should be pulled up to Vdd through a pullup resistor. The two VREF pins (A1 and V1) are connected together internally by approximately 150. However, it is necessary to connect only one of the two VREF pins to the external VREF power supply. An unused VREF pin should be terminated with a VREF coupling capacitor.

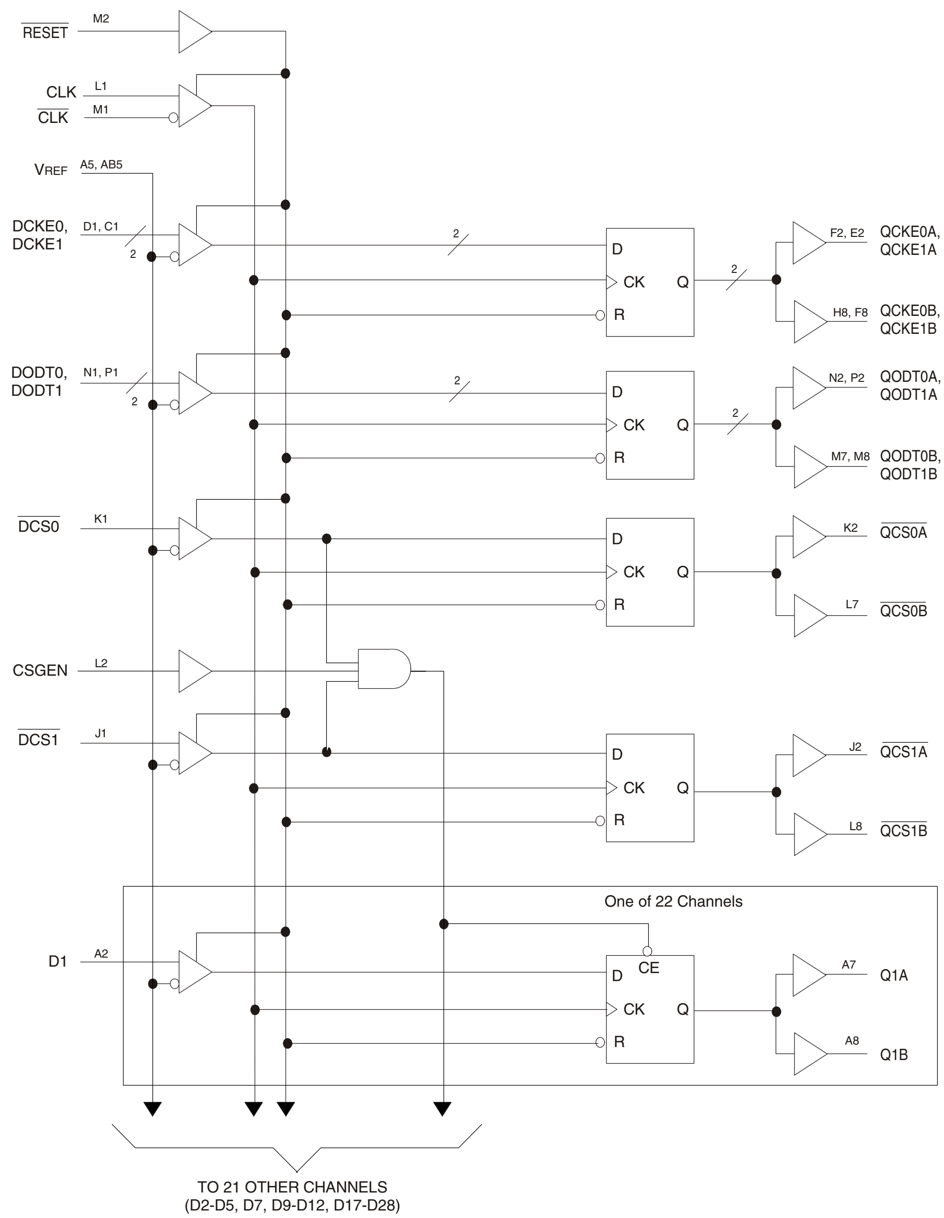
Features

- 28-bit 1:2 registered buffer with parity check functionality
- Supports SSTL_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on CSGEN and RESET inputs
- Low voltage operation: VDD = 1.7V to 1.9V
- Available in 176-ball LFBGA package

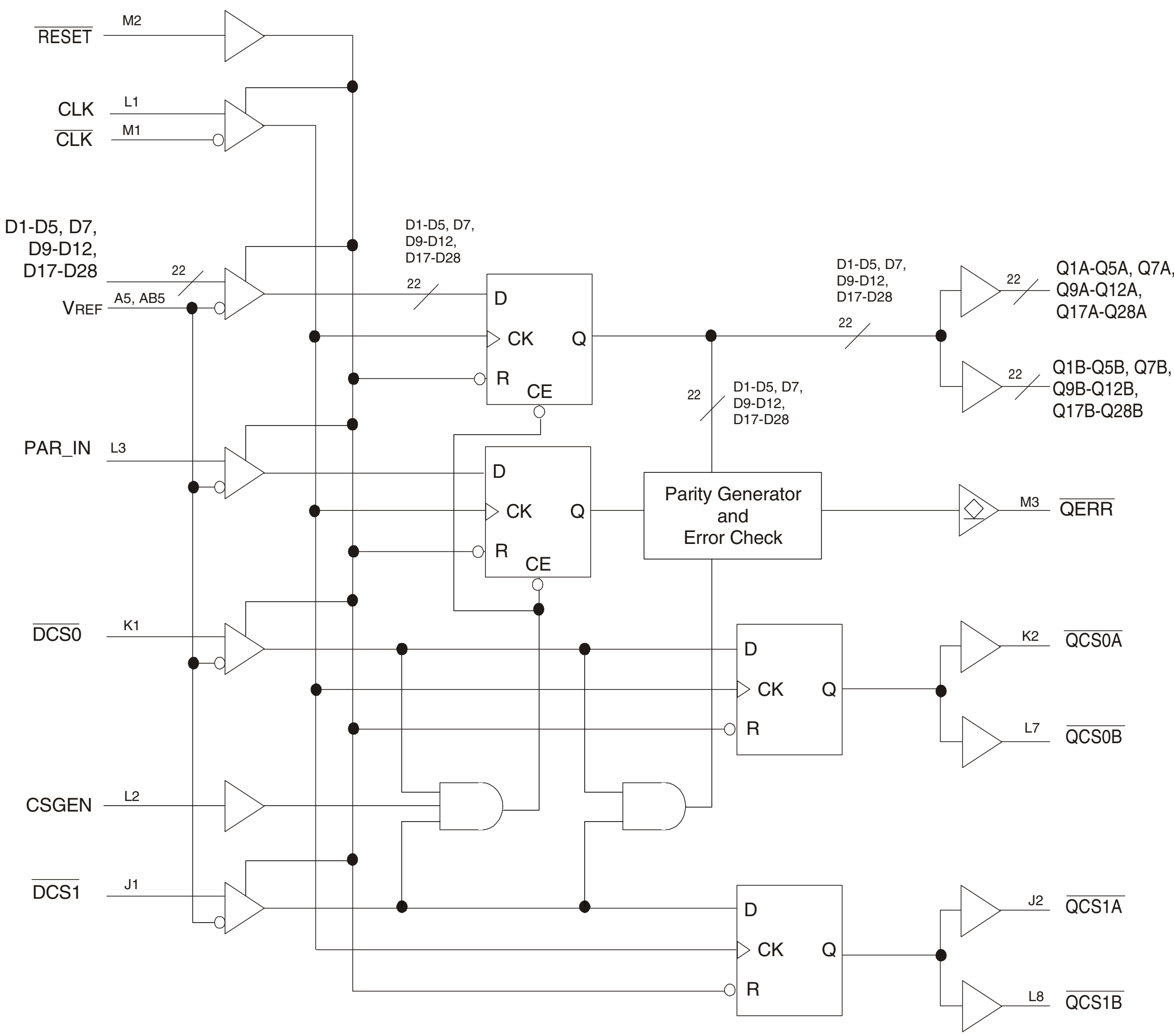
Applications

- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS98ULPA877A or IDTCSPUA877A
- Ideal for DDR2 400, 533, and 667

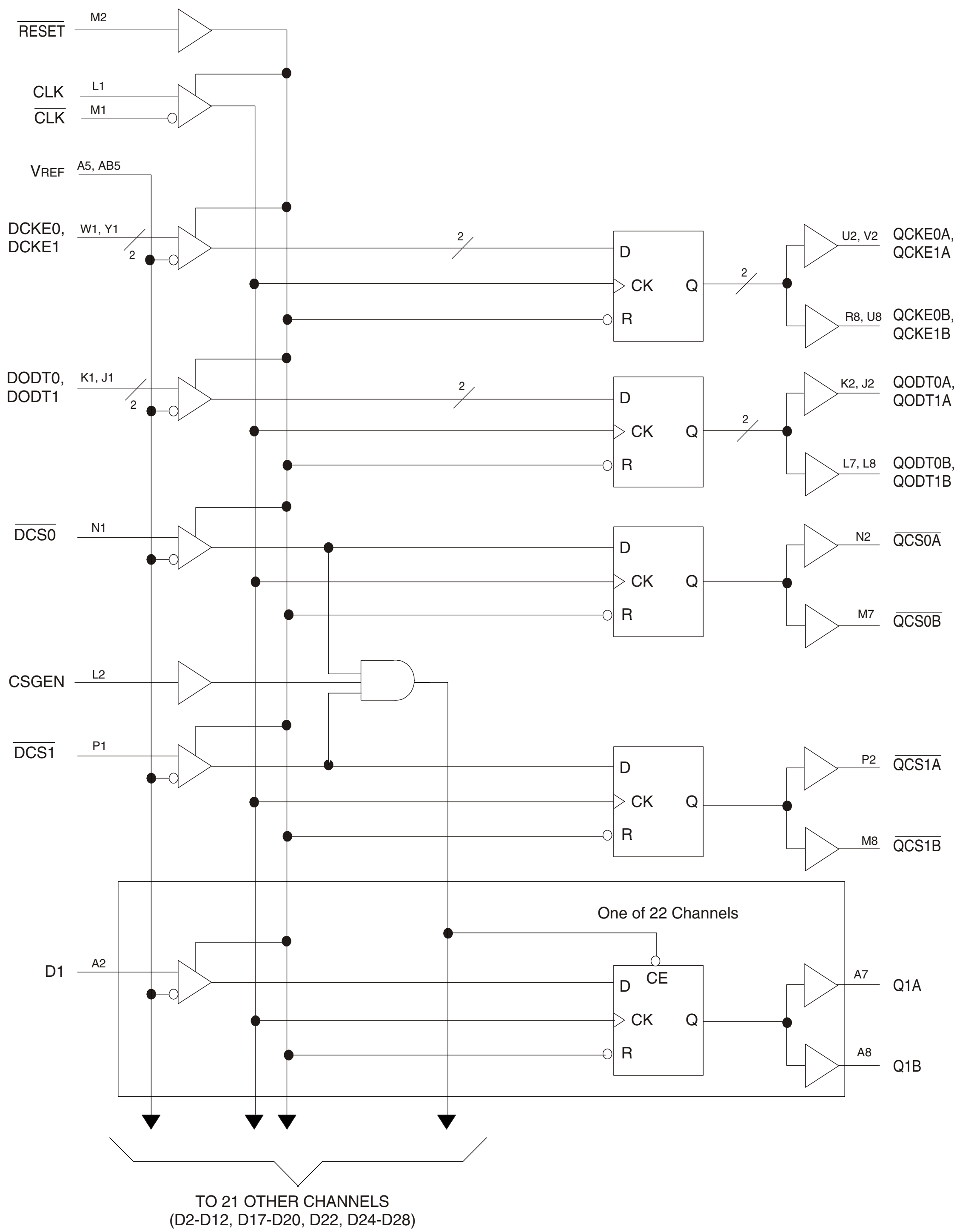
Block Diagram



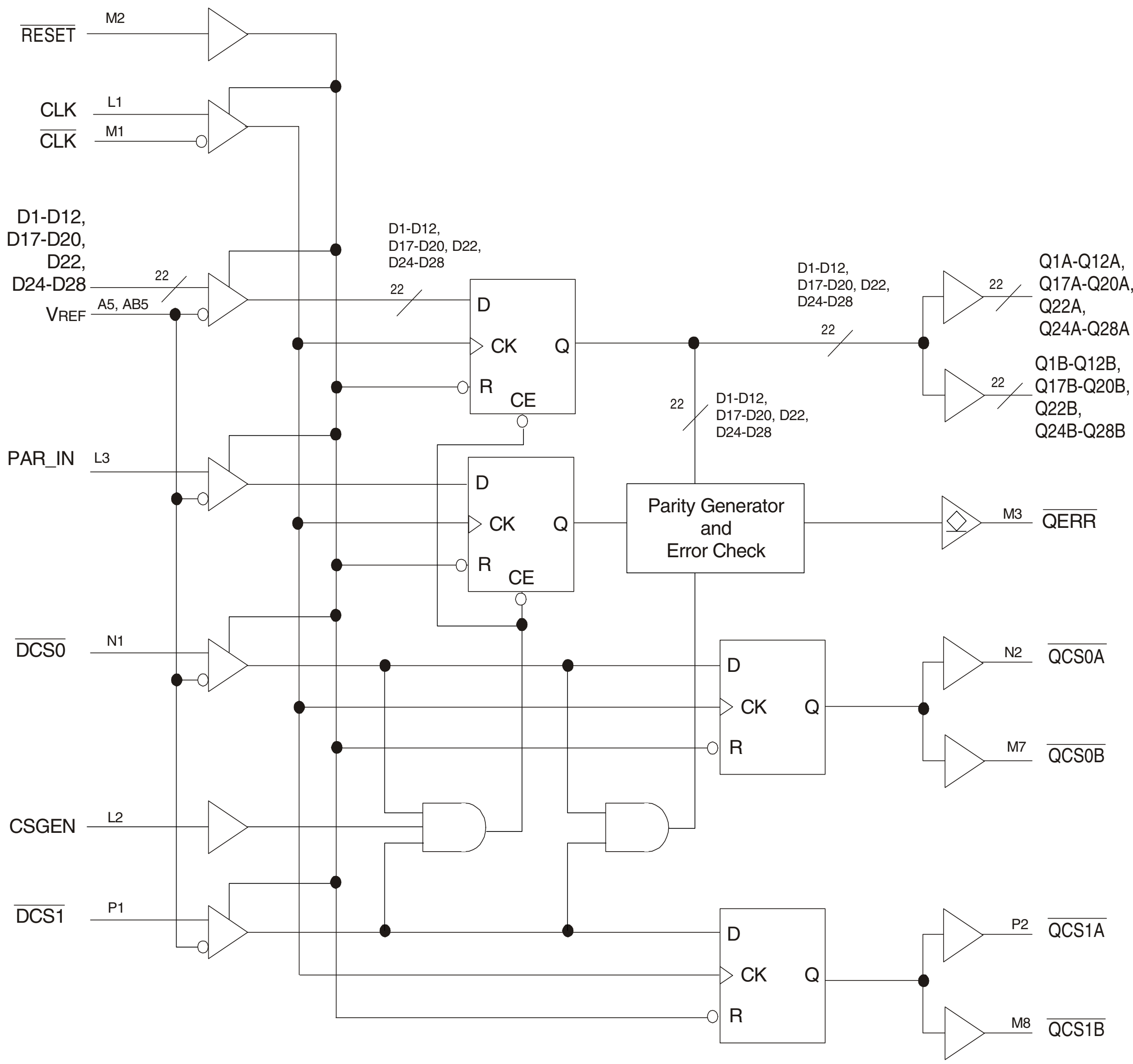
Parity Logic Diagram



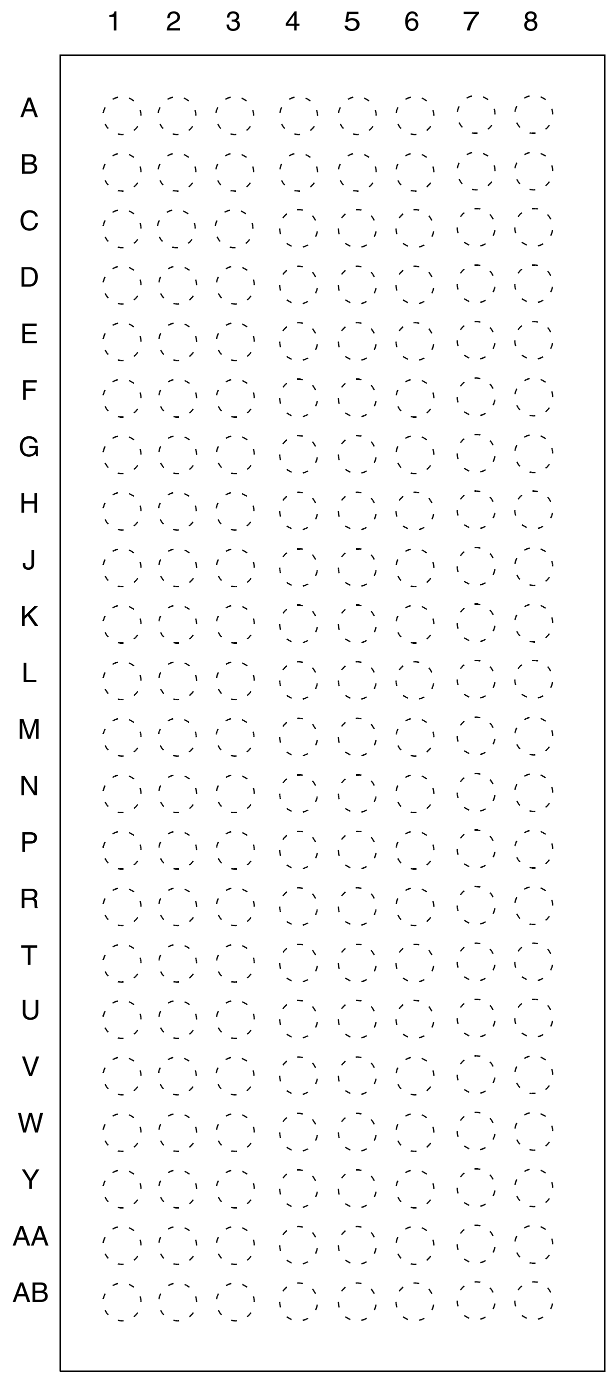
Block Diagram



Parity Logic Diagram



Pin Configuration



176 BALL BGA
TOP VIEW

Pin Configuration

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	VREF	GND	Q1A	Q1B
B	D4	D3	VDD	VDD	VDD	VDD	Q2A	Q2B
C	D6 (DCKE1)	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8 (DCKE0)	D7	VDD	VDD	VDD	VDD	Q4A	Q4B
E	D9	Q6A (QCKE1A)	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A (QCKE0A)	VDD	VDD	VDD	VDD	Q7A	Q6B (QCKE0B)
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	VDD	VDD	VDD	VDD	Q11A	Q8B (QCKE0B)
J	$\overline{\text{DCS1}}$	$\overline{\text{QCS1}}$	GND	GND	GND	GND	Q10B	Q9B
K	$\overline{\text{DCS0}}$	$\overline{\text{QCS0}}$	VDD	VDD	VDD	VDD	Q12B	Q11B
L	CLK	CSGEN	PAR_IN	GND	GND	GND	Q14B ($\overline{\text{QCS0B}}$)	Q13B ($\overline{\text{QCS1B}}$)
M	$\overline{\text{CLK}}$	$\overline{\text{RESET}}$	$\overline{\text{QERR}}$	VDD	VDD	VDD	Q15B (QODT0B)	Q16B (QODT1B)
N	D15 (DODT0)	Q15A (QODT0A)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DODT1)	Q16A (QODT1A)	VDD	VDD	VDD	VDD	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B
T	D18	Q19A	VDD	VDD	VDD	VDD	Q20A	Q22B
U	D19	Q21A	GND	GND	GND	GND	Q22A	Q23B
V	D20	Q23A	VDD	VDD	VDD	VDD	Q24A	Q24B
W	D21	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23	D24	VDD	VDD	VDD	VDD	Q26A	Q26B
AA	D24	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	VDD	VREF	VDD	Q28A	Q28B

1:2 REGISTER A (C = 0)

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	VREF	GND	Q1A	Q1B
B	D4	D3	VDD	VDD	VDD	VDD	Q2A	Q2B
C	D6	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8	D7	VDD	VDD	VDD	VDD	Q4A	Q4B
E	D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A	VDD	VDD	VDD	VDD	Q7A	Q6B
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	VDD	VDD	VDD	VDD	Q11A	Q8B
J	D13 (DODT1)	Q13A (QODT1A)	GND	GND	GND	GND	Q10B	Q9B
K	D14 (DODT0)	Q14A (QODT0A)	VDD	VDD	VDD	VDD	Q12B	Q11B
L	CLK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
M	$\overline{\text{CLK}}$	$\overline{\text{RESET}}$	$\overline{\text{QERR}}$	VDD	VDD	VDD	Q15B (QCS0B)	Q16B ($\overline{\text{QCS1B}}$)
N	D15 ($\overline{\text{DCS0}}$)	Q15A ($\overline{\text{QCS0A}}$)	GND	GND	GND	GND	Q17B	Q18B
P	D16 ($\overline{\text{DCS1}}$)	Q16A ($\overline{\text{QCS1A}}$)	VDD	VDD	VDD	VDD	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
T	D18	Q19A	VDD	VDD	VDD	VDD	Q20A	Q22B
U	D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
V	D20	Q23A (QCKE1A)	VDD	VDD	VDD	VDD	Q24A	Q24B
W	D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23 (DCKE1)	D24	VDD	VDD	VDD	VDD	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	VDD	VREF	VDD	Q28A	Q28B

1:2 REGISTER B (C = 1)

NOTE: NC denotes a no-connect (ball present but not connected to the die).

Function Table

Inputs[1]							Outputs			
$\overline{RESET}$	$\overline{DCS0}$	$\overline{DCS1}$	CSGEN	CLK	$\overline{CLK}$	Dx, DODT, DCKE	Qn	$\overline{QCS0}$	$\overline{QCS1}$	QODT, QCKE
H	L	L	X	↑	↓	L	L			
H	L	L	X	↑	↓	H	H			
H	L	L	X	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]	Q_0[2]
H	L	H	X	↑	↓	L	L			
H	L	H	X	↑	↓	H	H			
H	L	H	X	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]	Q_0[2]
H	L	L	X	↑	↓	L	L			
H	L	L	X	↑	↓	H	H			
H	L	L	X	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]	Q_0[2]
H	H	H	L	↑	↓	L	L			
H	H	H	L	↑	↓	H	H			
H	H	H	L	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]	Q_0[2]
H	H	H	H	↑	↓	L	Q_0[2]			
H	H	H	H	↑	↓	H	Q_0[2]			
H	H	H	H	L or H	L or H	X	Q_0[2]	Q_0[2]	Q_0[2]	Q_0[2]
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L	L

1 H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW to HIGH
↓ = HIGH to LOW

2 Output Level before the indicated steady-state conditions were established.

Parity and Standby Function Table

Inputs[1]							Outputs
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CLK	$\overline{\text{CLK}}$	Σ of Inputs = H (D1 - D28)	PAR_IN[2]	$\overline{\text{QERR}}$[3]
H	L	X	↑	↓	Even	L	H
H	L	X	↑	↓	Odd	L	L
H	L	X	↑	↓	Even	H	L
H	L	X	↑	↓	Odd	H	H
H	X	L	↑	↓	Even	L	H
H	X	L	↑	↓	Odd	L	L
H	X	L	↑	↓	Even	H	L
H	X	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$\overline{\text{QERR}}_0$[4]
H	X	X	↑	↓	X	X	$\overline{\text{QERR}}_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	H

1 H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW to HIGH
↓ = HIGH to LOW

2 PAR_IN arrives one clock cycle after the data to which it applies.

3 This transition assumes $\overline{\text{QERR}}$ is HIGH at the crossing of CLK going HIGH and $\overline{\text{CLK}}$ going LOW. If $\overline{\text{QERR}}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{\text{RESET}}$ is driven LOW.

4 If $\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$, and CSGEN are driven HIGH, the device is placed in low-power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the $\overline{\text{QERR}}$ output is driven LOW, it stays latched LOW for the LPM plus two clock cycles or until $\overline{\text{RESET}}$ is driven LOW.

Absolute Maximum Ratings

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Item		Rating
Supply Voltage, V_{DD}		-0.5V to 2.5V
Input Voltage Range, V_I[1]		-0.5V to V_{DD} + 2.5V
Output Voltage Range, V_O[1,2]		-0.5V to V_{DDQ} + 0.5V
Input Clamp Current, I_{IK}		±50mA
Output Clamp Current, I_{OK}		±50mA
Continuous Output Clamp Current, I_O		±50mA
Continuous Current through each V_{DD} or GND		±100mA
Package Thermal Impedance (θja)[3]	0m/s Airflow	40.4°C/W
	1m/s Airflow	29.1°C/W
Storage Temperature		-65 to +150°C

1 The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
2 This current will flow only when the output is in the high state level $V_O > V_{DDQ}$.
3 The package thermal impedance is calculated in accordance with JESD 51.

Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range

Parameter	V_{DD} = 1.8V ± 0.1V		Units
	Min.	Max.	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ[1]		1	V/ns

1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

Terminal Functions

Terminal Name	Electrical Characteristics	Description
GND	Ground Input	Ground
V_{DD}	1.8V nominal	Power Supply Voltage
V_{REF}	0.9V nominal	Input Reference Clock
CLK	Differential Input	Positive Master Clock Input
$\overline{\text{CLK}}$	Differential Input	Negative Master Clock Input
C	LVCMOS Input	Configuration Control Inputs - Register A or Register B
$\overline{\text{RESET}}$	LVCMOS Input	Asynchronous Reset Input. Resets registers and disables Vref data and clock differential-input receivers.
CSGEN	LVCMOS Input	Chip select gate enable – When high, D1-D28 inputs will be latched only when at least one chip select input is low during the rising edge of the clock. When low, the D1-D28 inputs will be latched and redriven on every rising edge of the clock.
D1 - D28	SSTL_18 Input	Data Input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$.
$\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$	SSTL_18 Input	Chip select inputs – These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to redrive all D inputs (CSGEN high) only when at least one chip select input is low. If CSGEN, $\overline{\text{DCS0}}$, and $\overline{\text{DCS1}}$ inputs are high, D1-D28 inputs will be disabled.
DCKE0, DCKE1	SSTL_18 Input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ controls
DODT0, DODT1	SSTL_18 Input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ controls
PAR_IN	SSTL_18 Input	Parity Input arrives one cycle after corresponding data input
Q1 - Q28	1.8V CMOS	Data Outputs that are suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ controls
$\overline{\text{QCS0}}$, $\overline{\text{QCS1}}$	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ controls
QCKE0, QCKE1	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ controls
QODT0, QODT1	1.8V CMOS	Data Output that will not be suspended by the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ controls
$\overline{\text{QERR}}$	Open Drain Output	Output Error bit, generated one cycle after the corresponding data output
NC		No Connection

Operating Characteristics, T_A = 25°C

The $\overline{RESET}$ and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is Low.

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{DD}	I/O Supply Voltage		1.7	1.8	1.9	V
V_{REF}	Reference Voltage		0.49 * V_{DD}	0.5 * V_{DD}	0.51 * V_{DD}	V
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input Voltage		0		V_{DD}	V
V_{IH}	AC High-Level Input Voltage	Data $\overline{CSR}$ and PAR_IN inputs	V_{REF} + 0.25			V
V_{IL}	AC Low-Level Input Voltage				V_{REF} - 0.25	
V_{IH}	DC High-Level Input Voltage		V_{REF} + 0.125			
V_{IL}	DC Low-Level Input Voltage				V_{REF} - 0.125	
V_{IH}	High-Level Input Voltage	$\overline{RESET}$, C0, C1	0.65 * V_{DDQ}			V
V_{IL}	Low-Level Input Voltage				0.35 * V_{DDQ}	
V_{ICR}	Common Mode Input Range	CLK, $\overline{CLK}$	0.675		1.125	V
V_{ID}	Differential Input Voltage		600			mV
I_{OH}	High-Level Output Current				-6	mA
I_{OL}	Low-Level Output Current				6	
T_A	Operating Free-Air Temperature		0		+70	°C

DC Electrical Characteristics Over Operating Range

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = 0°C to +70°C, V_{DDQ}/V_{DD} = 2.5V ± 0.2V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = -6mA, V_{DDQ} = 1.7V	1.2			V
V_{OL}	Output LOW Voltage	I_{OL} = 6mA, V_{DDQ} = 1.7V			0.5	V
I_{IL}	All Inputs	V_I = V_{DD} or GND; V_{DD} = 1.9V	-5		+5	μA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 1.9V, $\overline{\text{RESET}}$ = GND			200	μA
	Static Operating	I_O = 0, V_{DD} = 1.9V, $\overline{\text{RESET}}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK = $\overline{\text{CLK}}$ = $V_{IH(AC)}$ or $V_{IL(AC)}$			10	mA
		I_O = 0, V_{DD} = 1.9V, $\overline{\text{RESET}}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK = $V_{IH(AC)}$, $\overline{\text{CLK}}$ = $V_{IL(AC)}$		200		
I_{DDD}	Dynamic Operating (clock only)	I_O = 0, V_{DD} = 1.8V, $\overline{\text{RESET}}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle		500		μA/Clock MHz
	Dynamic Operating (per each data input) 1:2 mode	I_O = 0, V_{DD} = 1.8V, $\overline{\text{RESET}}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.		44		μA/Clock MHz/ Data
C_I	Data Inputs	V_I = V_{REF} ± 250mV	2		3.5	pF
	CLK and $\overline{\text{CLK}}$	V_{ICR} = 0.9V, V_{IPP} = 600mV	2.5		4	
	$\overline{\text{RESET}}$	V_I = V_{DD} or GND		5		

Timing Requirements Over Recommended Operating Free-Air Temperature Range

Symbol	Parameter		V_{DD} = 1.8V ± 0.1V Min.	Max.	Units
f_{CLOCK}	Clock Frequency			410	MHz
t_W	Pulse Duration, CLK, $\overline{CLK}$ HIGH or LOW		1		ns
t_{ACT}[1,2]	Differential Inputs Active Time			10	ns
t_{INACT}[1,3]	Differential Inputs Inactive Time			15	ns
t_{SU}	Setup Time	$\overline{DCS0}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS1}$ and CSGEN HIGH; $\overline{DCS1}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS0}$ and CSGEN HIGH;	0.7		ns
		$\overline{DCS0}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS1}$ LOW and CSGEN HIGH or LOW; $\overline{DCS1}$ before CLK↑, $\overline{CLK}$↓, $\overline{DCS0}$ LOW and CSGEN HIGH or LOW	0.5		ns
		DODTn, DCKEn, PAR_IN, and data before CLK↑, $\overline{CLK}$↓	0.5		ns
t_H	Hold Time	$\overline{DCSn}$, DODT,n DCKEn, and data after CLK↑, $\overline{CLK}$↓	0.5		ns
		PAR_IN after CLK↑, $\overline{CLK}$↓	0.5		ns

1 This parameter is not production tested.

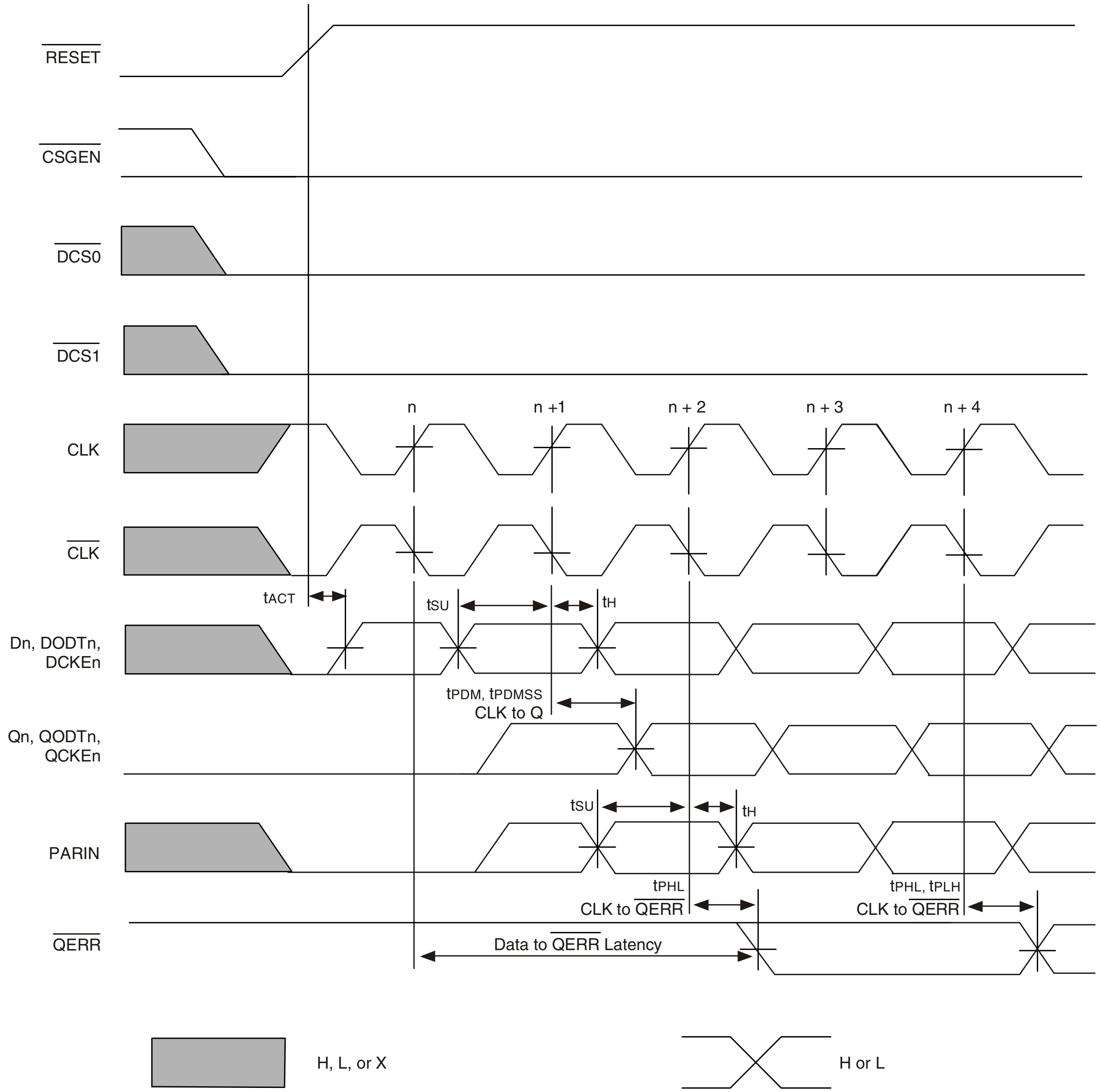
2 V_{REF} must be held at a valid input voltage level and data inputs must be held at valid voltage levels for a minimum time of t_{ACT} (max) after $\overline{RESET}$ is taken HIGH.

3 V_{REF} data and clock inputs must be held at valid input voltage levels (not floating) for a minimum time of t_{INACT} (max) after $\overline{RESET}$ is taken LOW.

Switching Characteristics Over Recommended Free Air Operating Range (unless otherwise noted)

Symbol	Parameter	V_{DD} = 1.8V ± 0.1V Min.	Max.	Units
f_{MAX}	Max Input Clock Frequency	410		MHz
t_{PDM}	Propagation Delay, single bit switching, CLK↑ / $\overline{CLK}$↓ to Qn	1.3	1.9	ns
t_{PDMSS}	Propagation Delay, simultaneous switching, CLK↑ / $\overline{CLK}$↓ to Qn		2	ns
t_{LH}	LOW to HIGH Propagation Delay, CLK↑ / $\overline{CLK}$↓ to $\overline{QERR}$	0.9	3	ns
t_{HL}	HIGH to LOW Propagation Delay, CLK↑ / $\overline{CLK}$↓ to $\overline{QERR}$	0.7	2.4	ns
t_{PLH}	HIGH to LOW Propagation Delay, $\overline{RESET}$↓ to Qn↓		3	ns
t_{PHL}	LOW to HIGH Propagation Delay, $\overline{RESET}$↓ to $\overline{QERR}$↑		3	ns

Register Timing

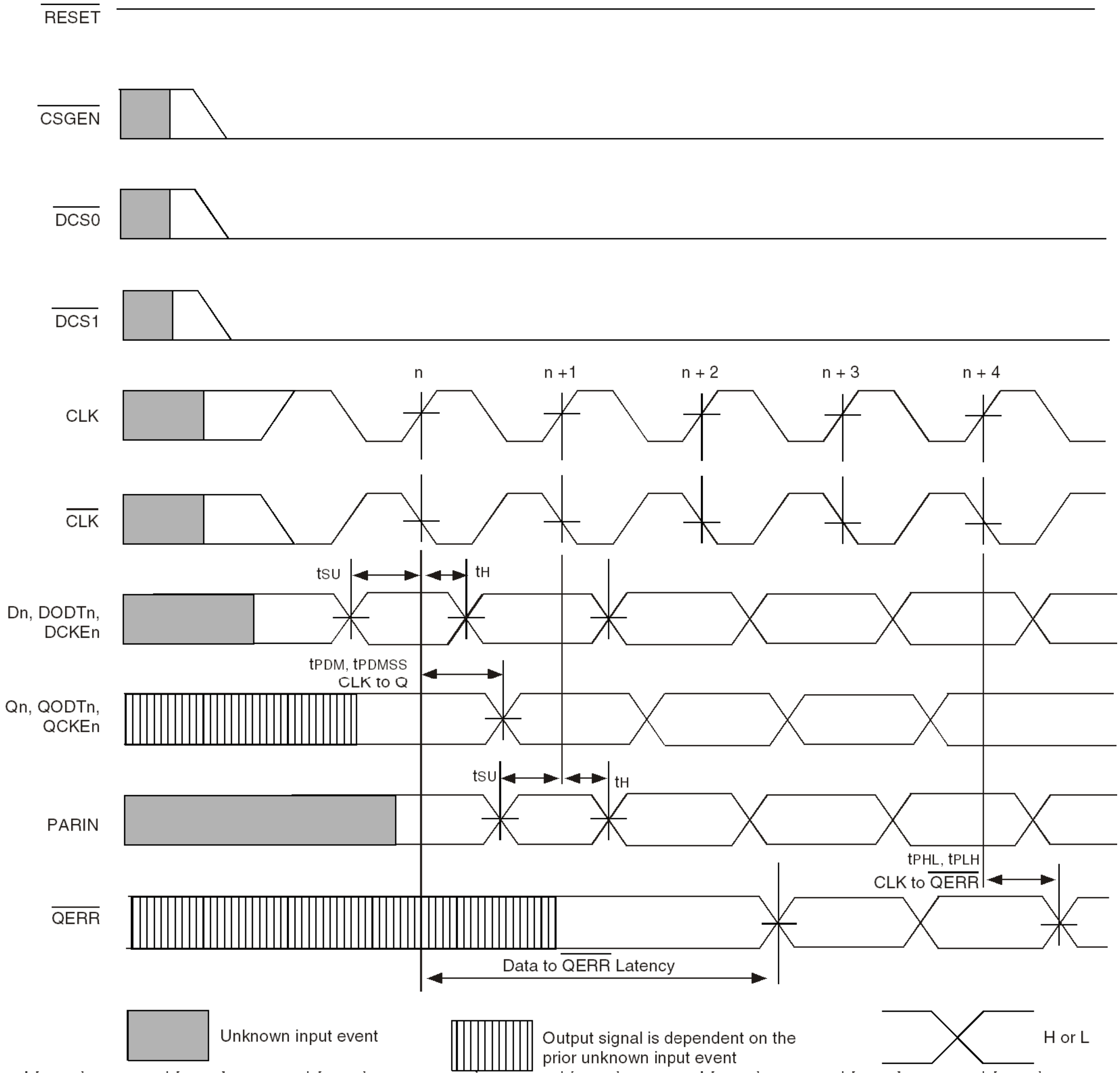


NOTES:

1.After $\overline{\text{RESET}}$ is switched from LOW to HIGH, all data and PAR_IN inputs signals must be set and held LOW for a minimum time of t_{ACTMAX}, to avoid false error.

2.If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse.

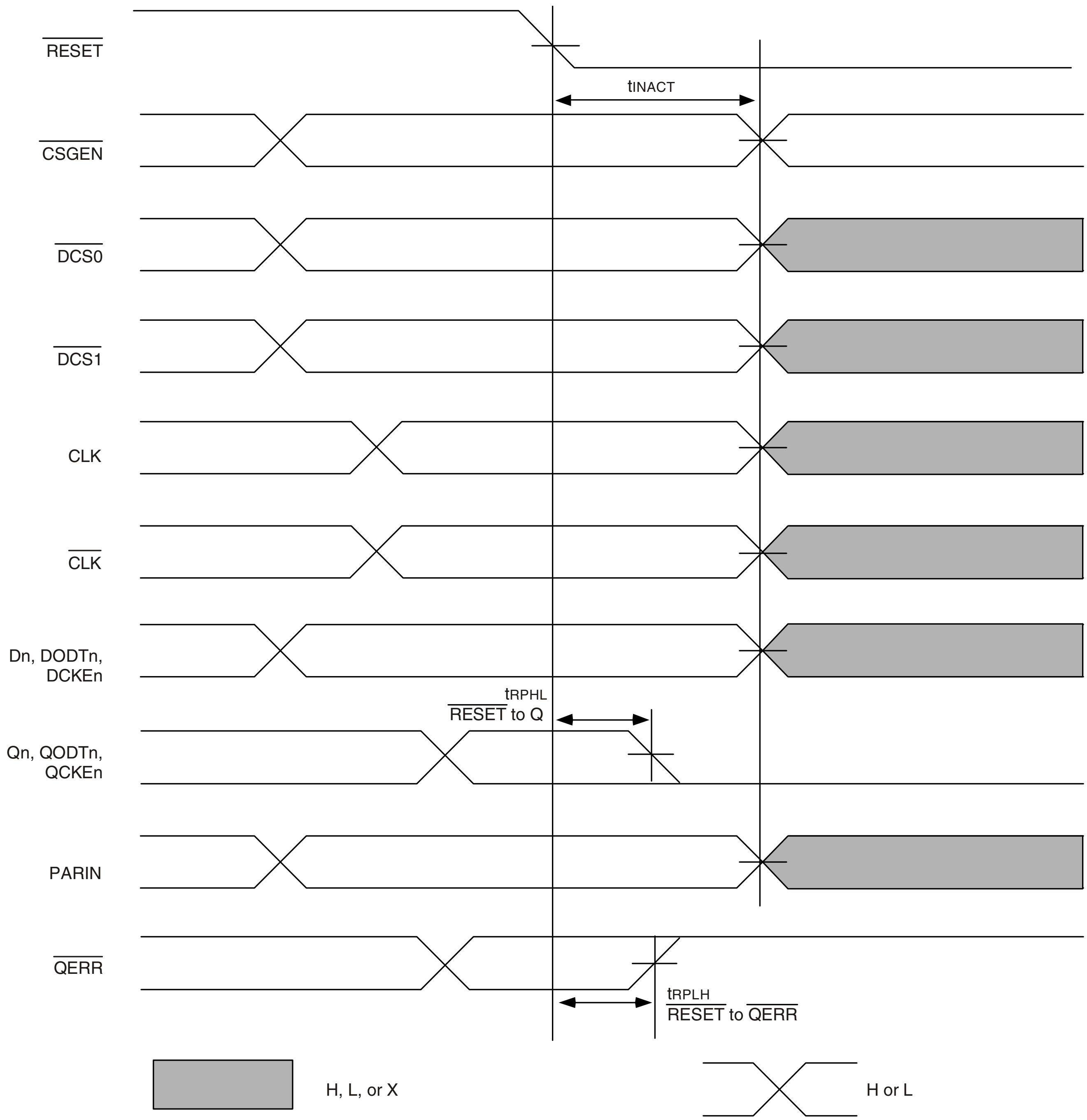
Register Timing



NOTE:

1.If the data is clocked in on the n clock pulse, the $\overline{\text{QERR}}$ output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven LOW, it stays latched LOW for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven LOW.

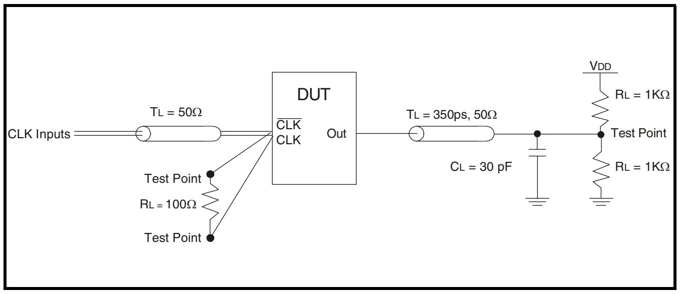
Register Timing



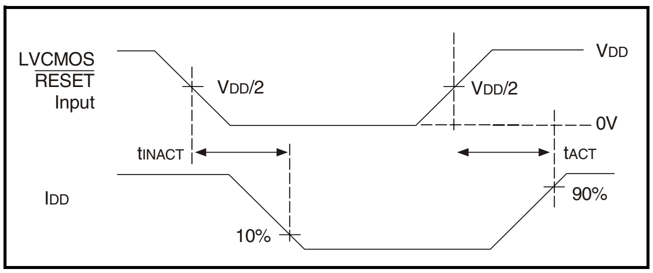
NOTE:

1.After RESET is switched from LOW to HIGH, all data and clock inputs signals must be set and held at valid logic levels (not floating) for a minimum time of tINACTMAX.

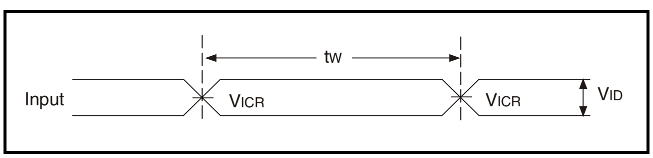
Test Circuits and Waveforms (V_{DD} = 1.8V ± 0.1V)



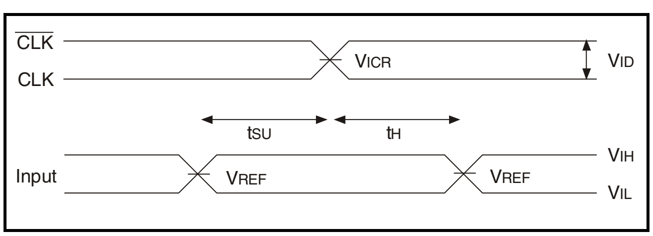
Simulation Load Circuit



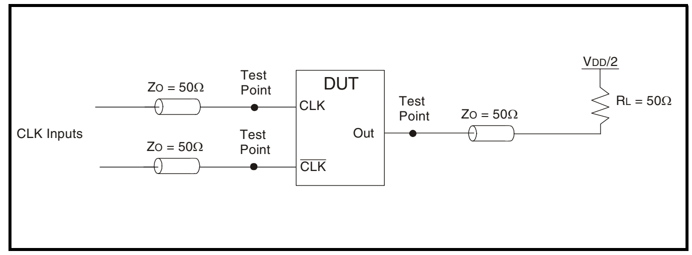
Voltage and Current Waveforms Inputs Active and Inactive Times



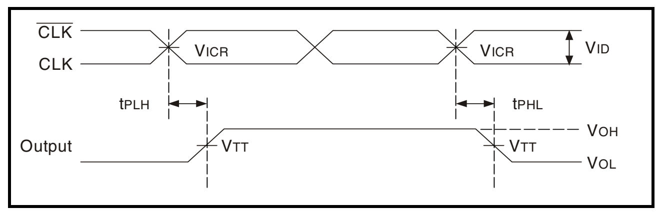
Voltage Waveforms - Pulse Duration



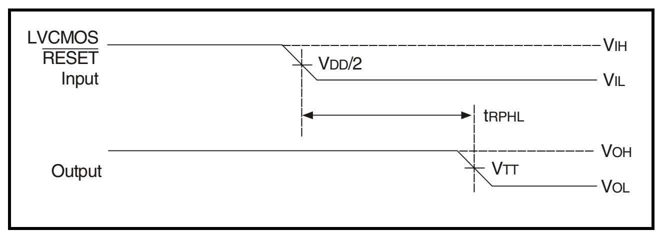
Voltage Waveforms - Setup and Hold Times



Production-Test Load Circuit



Voltage Waveforms - Propagation Delay Times

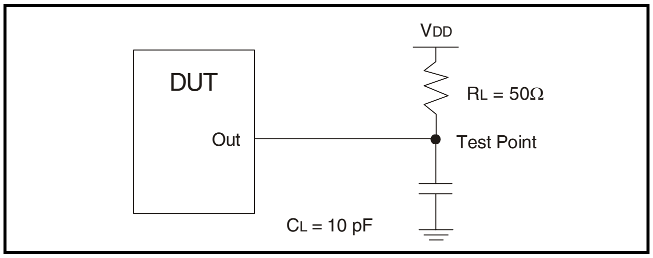


Voltage Waveforms - Propagation Delay Times

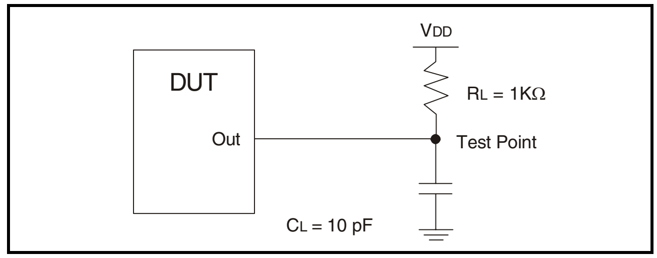
NOTES:

1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and Io = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{TT} = V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF}$ + 250mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
7. $V_{IL} = V_{REF}$ - 250mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600mV.
9. t_{PLH} and t_{PHL} are the same as t_{PDM}.

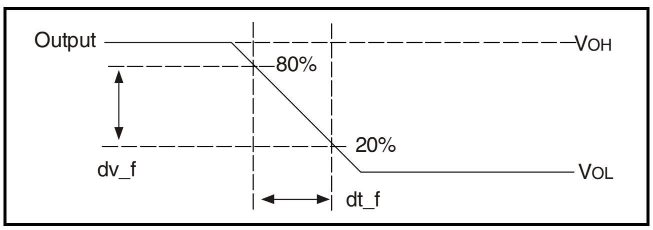
Test Circuits and Waveforms (VDD = 1.8V ± 0.1V)



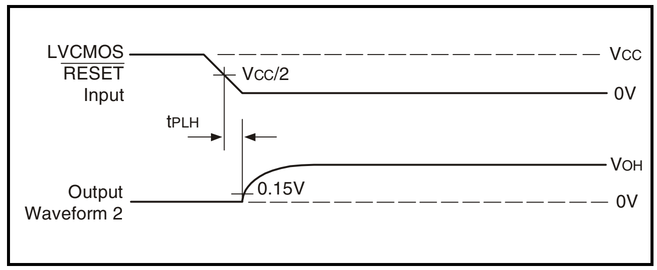
Load Circuit: High-to-Low Slew-Rate Adjustment



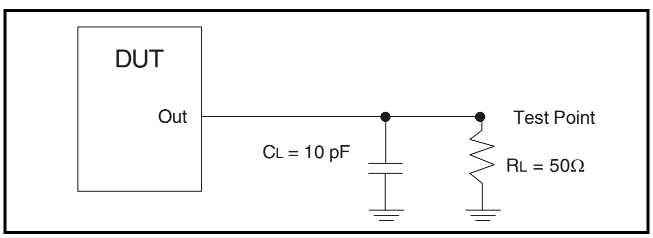
Load Circuit: Error Output Measurements



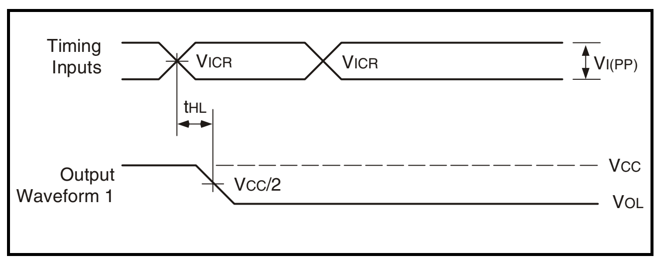
Voltage Waveforms: High-to-Low Slew-Rate Adjustment



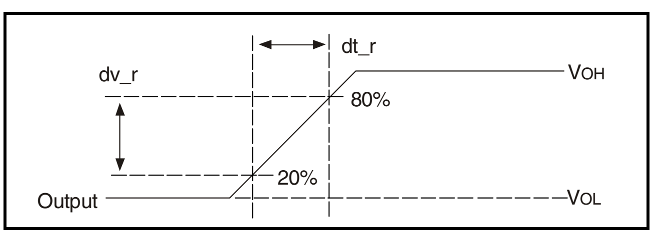
Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to RESET input)



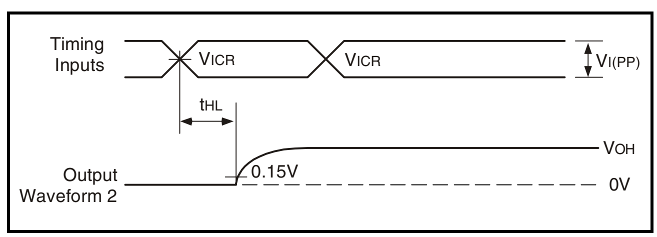
Load Circuit: Low-to-High Slew-Rate Adjustment



Voltage Waveforms: Open Drain Output High-to-Low Transition Time (with respect to clock inputs)



Voltage Waveforms: Low-to-High Slew-Rate Adjustment



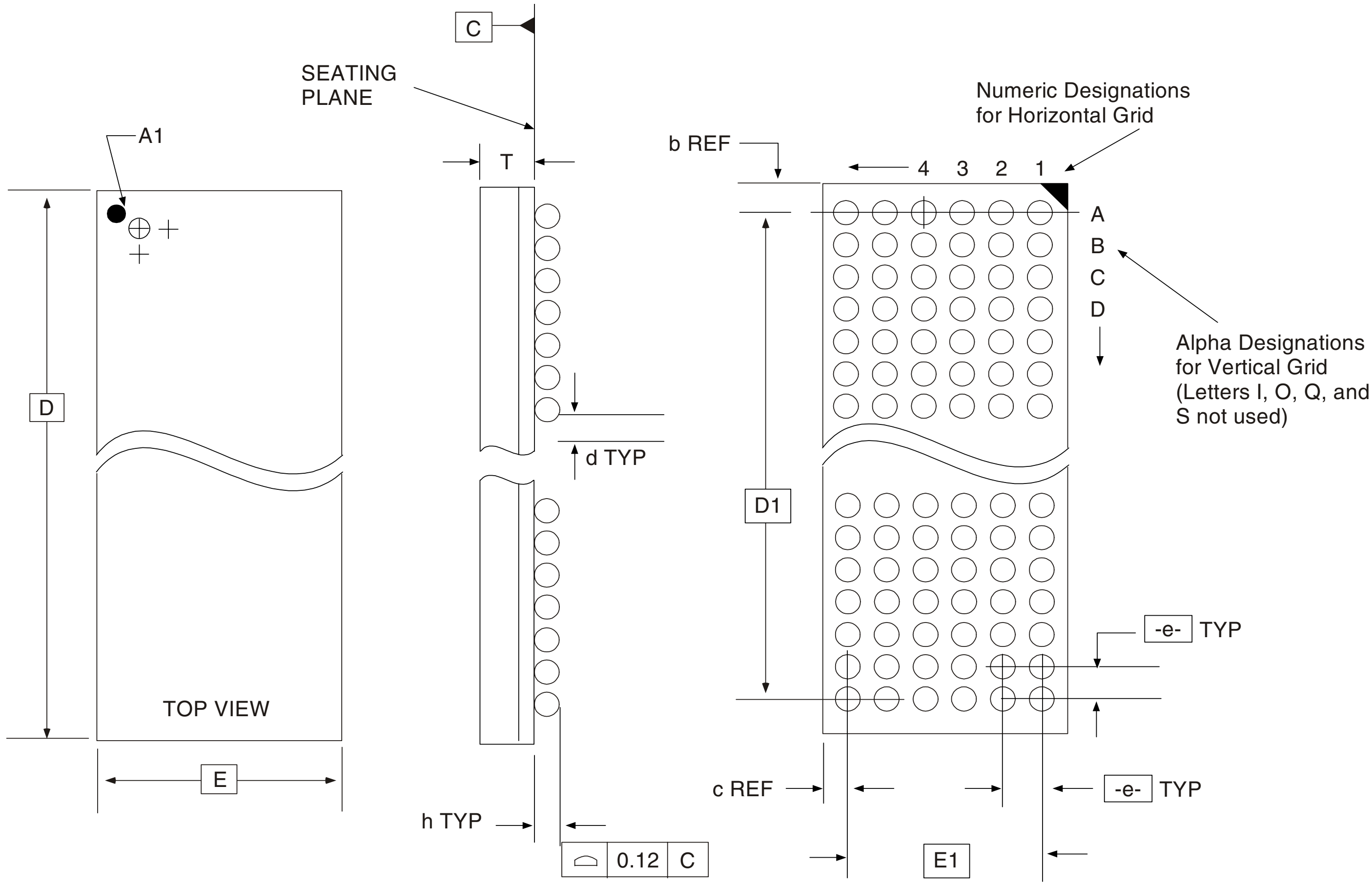
Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to clock inputs)

NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

Package Outline and Package Dimensions - BGA

Package dimensions are kept current with JEDEC Publication No. 95



ALL DIMENSIONS IN MILLIMETERS

D	E	T Min/Max	e	BALL GRID Horiz	BALL GRID Vert	BALL GRID Total	d Min/Max	h Min/Max	D1	E1	REF. DIMS b	REF. DIMS c	
15.00 Bsc	6.00 Bsc	0.94/1.20	0.65 Bsc	8	22	176	0.35/0.45	0.25/0.35	13.65 Bsc	4.55 Bsc	0.675	0.725	***

NOTE: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

* Source Ref.: JEDEC Publication 95, MO-205*, MO-255**, MO-246***

10-0055

Ordering Information

ICSSSTUAF XX XXX XX X

Family	Device Type	Package	Shipping Carrier
XX	XXX	XX	X

Code	Description
T	Tape and Reel
HLF	Low Profile, Fine Pitch, Ball Grid Array - Lead-Free
868B	28-Bit Configurable Registered Buffer for DDR2
32	Double Density

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