

NLAST4501

Analog Switch

The NLAST4501 is an analog switch manufactured in sub-micron silicon-gate CMOS technology. It achieves very low R_{ON} while maintaining extremely low power dissipation. The device is a bilateral switch suitable for switching either analog or digital signals, which may vary from zero to full supply voltage.

The NLAST4501 is a low voltage, TTL (low threshold) compatible device, pin for pin compatible with the MAX4501.

The Enable pin is compatible with standard TTL level outputs when supply voltage is nominal 5.0 Volts. It is also over-voltage tolerant, making it a very useful logic level translator.

- Guaranteed R_{ON} of 32 Ω at 5.5 V
- Low Power Dissipation: $I_{CC} = 2 \mu A$
- Low Threshold Enable pin TTL compatible at 5.0 Volts
- TTL version and pin for pin with NLAS4501
- Provides Voltage translation for many different voltage levels
 - 3.3 to 5.0 Volts, Enable pin may go as high as +5.5 Volts
 - 1.8 to 3.3 Volts
 - 1.8 to 2.5 Volts
- Improved version of MAX4501 (at any voltage between 2 and 5.5 Volts)
- Chip Complexity: FETs = 11

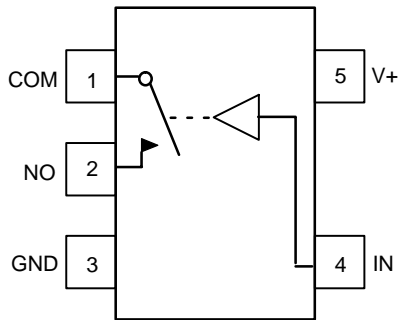


Figure 1. Pinout (Top View)



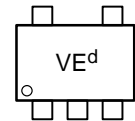
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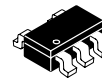
MARKING DIAGRAMS



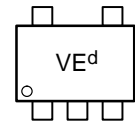
SC-88A / SOT-353/SC-70
DF SUFFIX
CASE 419A



Pin 1
d = Date Code



TSOP-5/SOT-23/SC-59
DT SUFFIX
CASE 483



Pin 1
d = Date Code

PIN ASSIGNMENT

Pin	Function
1	COM
2	NO
3	GND
4	Enable
5	V_{CC}

FUNCTION TABLE

On/Off Enable Input	State of Analog Switch
L	Off
H	On

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	Digital Input Voltage (Enable)	-0.5 to +7.0	V
V_{IS}	Analog Output Voltage (V_{NO} or V_{COM})	-0.5 to V_{CC} +0.5	V
I_{IK}	DC Current, Into or Out of Any Pin	± 20	mA
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$
T_J	Junction Temperature under Bias	+150	$^{\circ}C$
θ_{JA}	Thermal Resistance	SC-88 TSOP-5	$^{\circ}C/W$
P_D	Power Dissipation in Still Air at 85 $^{\circ}C$	SC-88 TSOP-5	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating	Oxygen Index: 30% - 35%	UL-94-VO (0.125 in)
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 100 N/A
$I_{Latch-Up}$	Latch-Up Performance	Above V_{CC} and Below GND at 85 $^{\circ}C$ (Note 5)	± 300

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	2.0	5.5	V
V_{IN}	Digital Input Voltage (Enable)	GND	5.5	V
V_{IO}	Static or Dynamic Voltage Across an Off Switch	GND	V_{CC}	V
V_{IS}	Analog Input Voltage (NO, COM)	GND	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	-55	+125	$^{\circ}C$
t_r, t_f	Input Rise or Fall Time, (Enable Input)	$V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature $^{\circ}C$	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

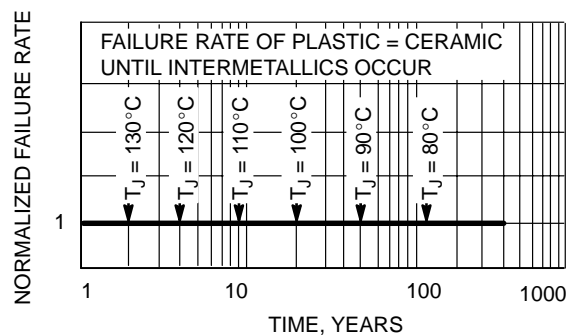


Figure 2. Failure Rate vs. Time Junction Temperature

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DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC}	Guaranteed Max Limit			Unit
				–55°C to 25°C	< 85°C	< 125°C	
V _{IH}	Minimum High-Level Input Voltage, Enable Inputs		3.0	1.4	1.4	1.4	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage, Enable Inputs		3.0	0.53	0.53	0.53	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
I _{IN}	Maximum Input Leakage Current, Enable Inputs	V _{IN} = 5.5 V or GND	0 V to 5.5 V	±0.1	±1.0	±1.0	µA
I _{CC}	Maximum Quiescent Supply Current (per package)	Enable and V _{IS} = V _{CC} or GND	5.5	1.0	1.0	2.0	µA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V _{CC}	Guaranteed Max Limit			Unit
				–55°C to 25°C	< 85°C	< 125°C	
R _{ON}	Maximum ON Resistance (Figures 8 – 12)	V _{IN} = V _{IH} V _{IS} = V _{CC} to GND I _{IS} = ≤ 10.0 mA	3.0	45	50	55	Ω
			4.5	30	35	40	
			5.5	25	30	35	
R _{FLAT(ON)}	ON Resistance Flatness	V _{IN} = V _{IH} I _{IS} = ≤ 10.0 mA V _{IS} = 1 V, 2 V, 3.5 V	4.5	4	4	5	Ω
I _{NO(OFF)}	NO Off Leakage Current (Figure 3)	V _{IN} = V _{IL} V _{NO} = 1.0 V or 4.5 V V _{COM} = 4.5 V or 1.0 V	5.5	1	10	100	nA
I _{COM(OFF)}	COM Off Leakage Current (Figure 3)	V _{IN} = V _{IL} V _{NO} = 4.5 V or 1.0 V V _{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions	V _{CC} (V)	Guaranteed Max Limit									Unit
				–55°C to 25°C			< 85°C			< 125°C			
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{ON}	Turn-On Time	R _L = 300 Ω, C _L = 35 pF (Figures 4, 5, and 13)	2.0		7.0	14			16			16	ns
			3.0		5.0	10			12			12	
			4.5		4.5	9			11			11	
			5.5		4.5	9			11			11	
t _{OFF}	Turn-Off Time	R _L = 300 Ω, C _L = 35 pF (Figures 4, 5, and 13)	2.0		11.0	22			24			24	ns
			3.0		7.0	14			16			16	
			4.5		5.0	10			12			12	
			5.5		5.0	10			12			12	
			Typical @ 25, V_{CC} = 5.0 V										
C _{IN}	Maximum Input Capacitance, Select Input							8				pF	
C _{NO} or C _{NC}	Analog I/O (switch off)							10					
C _{COM(OFF)}	Common I/O (switch off)							10					
C _{COM(ON)}	Feedthrough (switch on)							20					

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ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V _{CC} V	Limit	Unit
				25°C	
BW	Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response	V _{IS} = 0 dBm V _{IS} centered between V _{CC} and GND (Figures 6 and 14)	3.0	190	MHz
			4.5	200	
			5.5	220	
V _{ONL}	Maximum Feedthrough On Loss	V _{IS} = 0 dBm @ 10 kHz V _{IS} centered between V _{CC} and GND (Figure 6)	3.0	-2	dB
			4.5	-2	
			5.5	-2	
V _{ISO}	Off-Channel Isolation	f = 100 kHz; V _{IS} = 1 V RMS V _{IS} centered between V _{CC} and GND (Figures 6 and 15)	3.0	-93	dB
			4.5		
			5.5		
Q	Charge Injection Enable Input to Common I/O	V _{IS} = V _{CC} to GND, F _{IS} = 20 kHz t _r = t _f = 3 ns R _{IS} = 0 Ω, C _L = 1000 pF Q = C _L * ΔV _{OUT} (Figures 7 and 16)	3.0	1.5	pC
			5.5	3.0	
THD	Total Harmonic Distortion THD + Noise	F _{IS} = 20 Hz to 1 MHz, R _L = R _{gen} = 600 Ω, C _L = 50 pF V _{IS} = 3.0 V _{PP} sine wave V _{IS} = 5.0 V _{PP} sine wave (Figure 17)	3.3	0.3	%
			5.5	0.15	

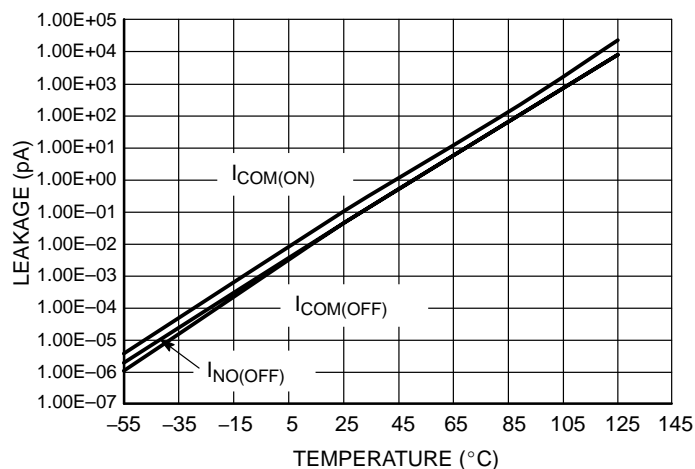


Figure 3. Switch Leakage vs. Temperature

NLAST4501

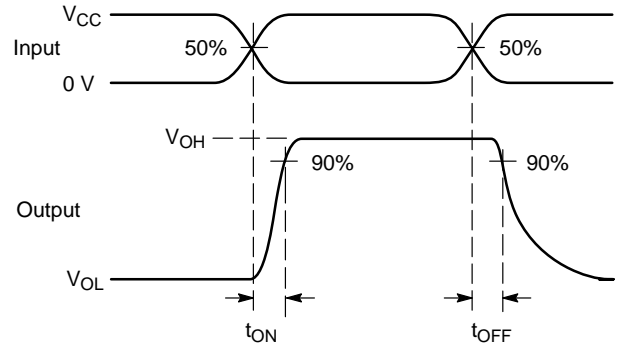
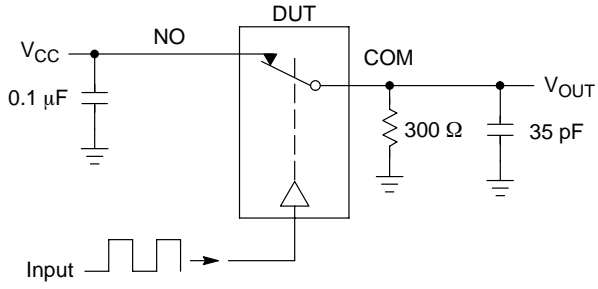


Figure 4. t_{ON}/t_{OFF}

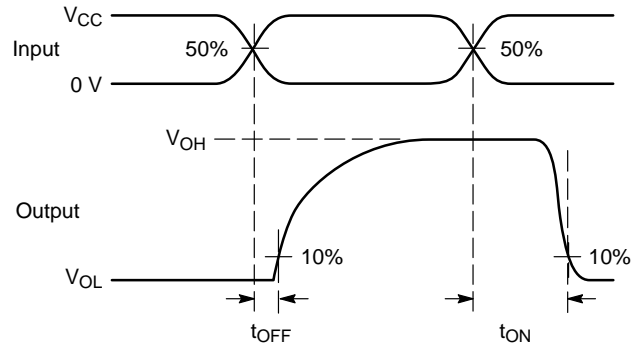
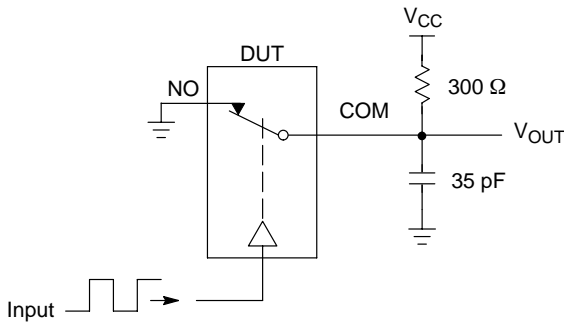
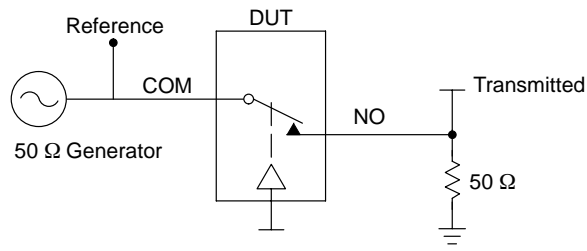


Figure 5. t_{ON}/t_{OFF}

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

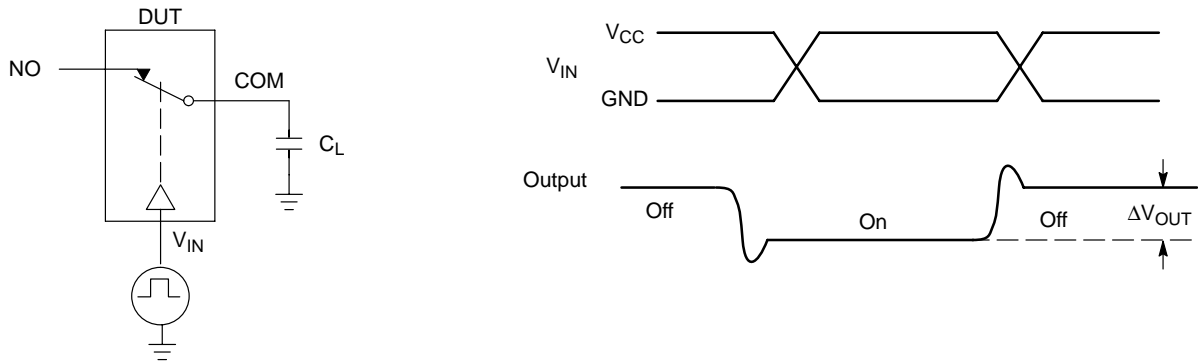


Figure 7. Charge Injection: (Q)

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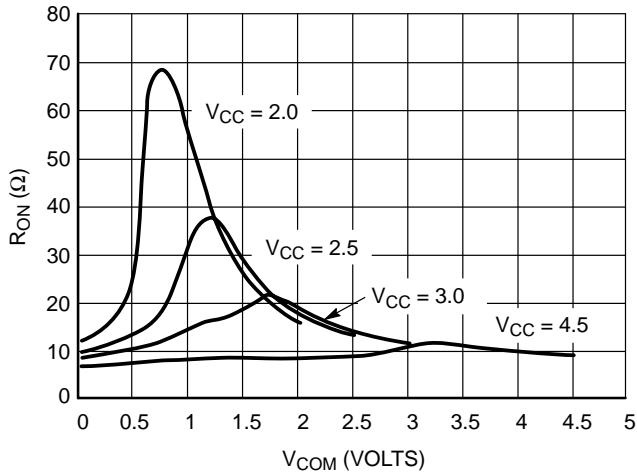


Figure 8. R_{ON} vs. V_{COM} and V_{CC} (@25°C)

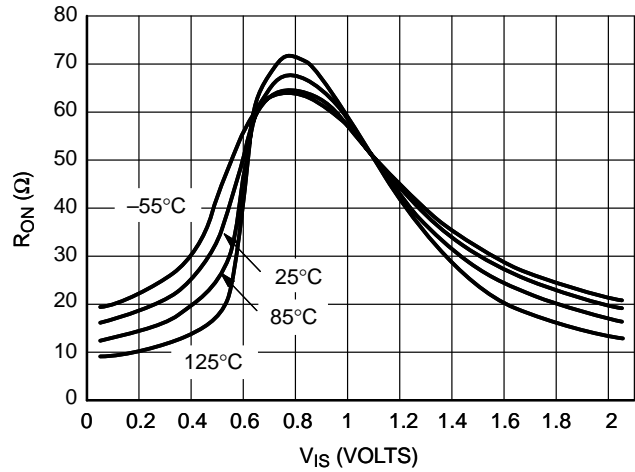


Figure 9. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 2.0$ V

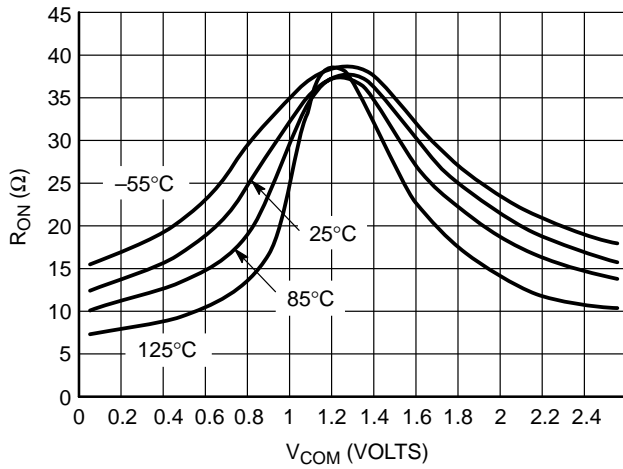


Figure 10. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 2.5$ V

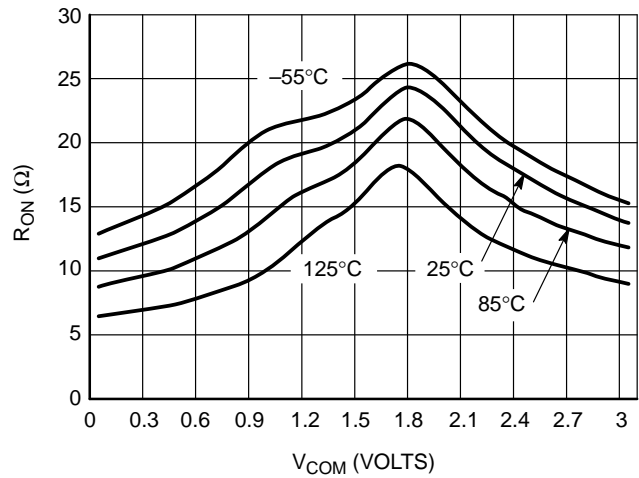


Figure 11. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 3.0$ V

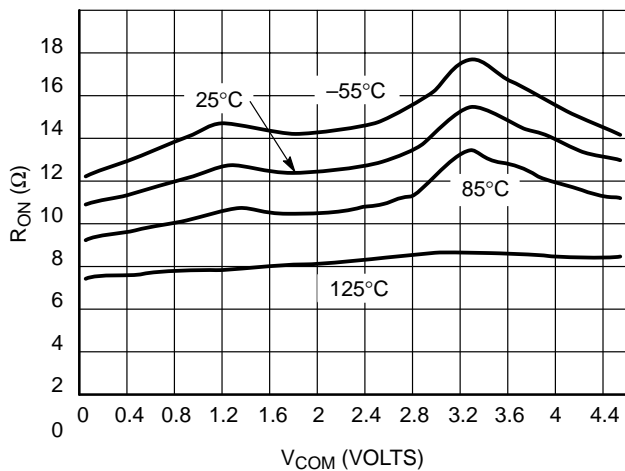


Figure 12. R_{ON} vs. V_{COM} and Temperature, $V_{CC} = 4.5$ V

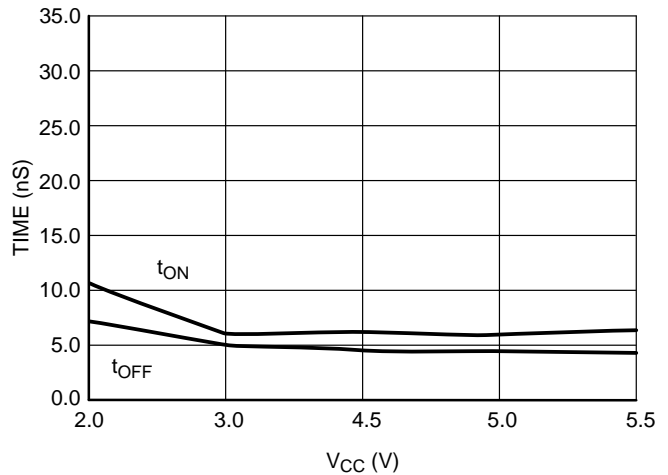


Figure 13. Switching Time vs. Supply Voltage, $T = 25^\circ\text{C}$

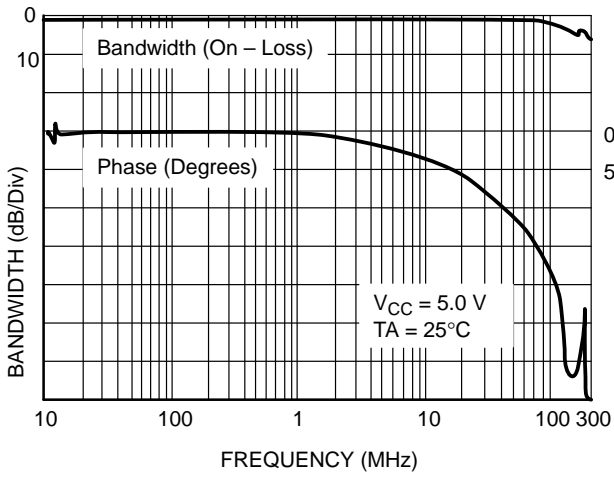


Figure 14. ON Channel Bandwidth and Phase Shift Over Frequency

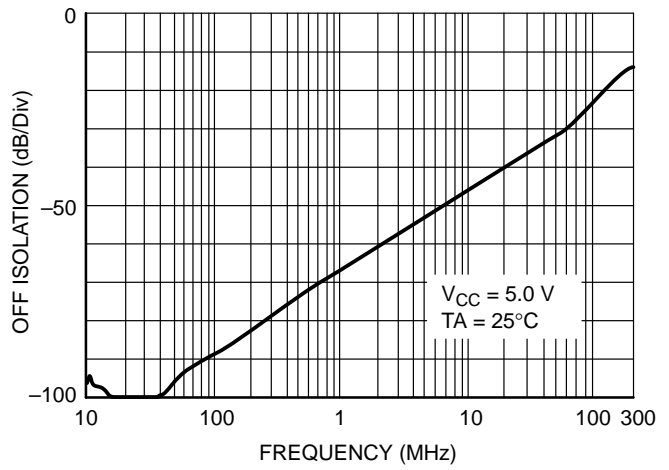


Figure 15. Off Channel Isolation

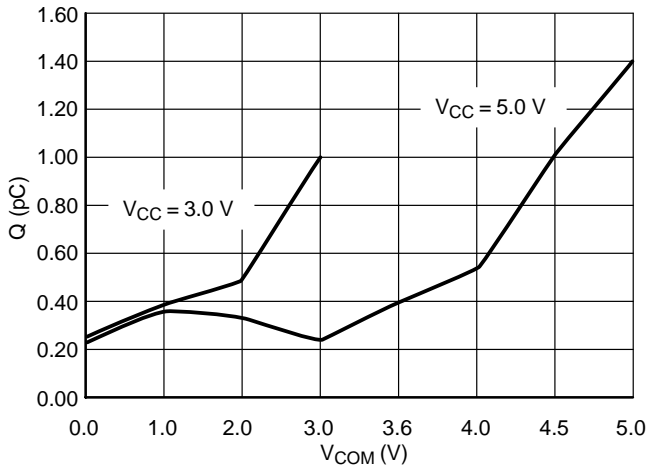


Figure 16. Charge Injection vs. V_{COM}

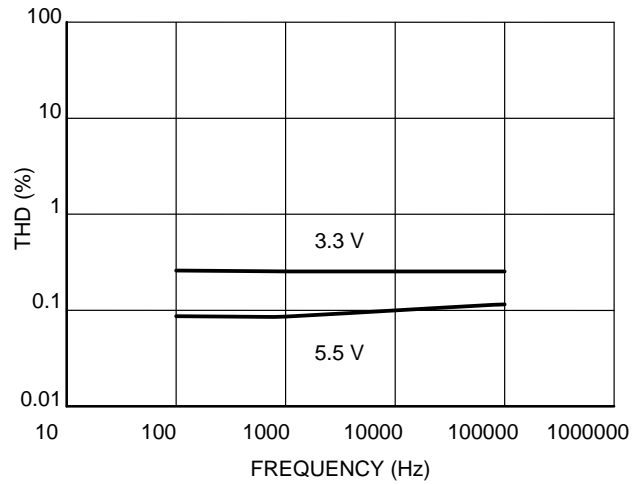


Figure 17. THD vs. Frequency

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DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/Common Name)	Tape & Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAST4501DFT2	NLAS	74	VHC1G	66	DF	T2	SC-88A/ SOT-353/ SC-70	178 mm (7 in) 3000 Unit
NLAST4501DTT1	NLAS	74	VHC1G	66	DT	T1	TSOPS/ SOT-23/ SC-59	178 mm (7 in) 3000 Unit

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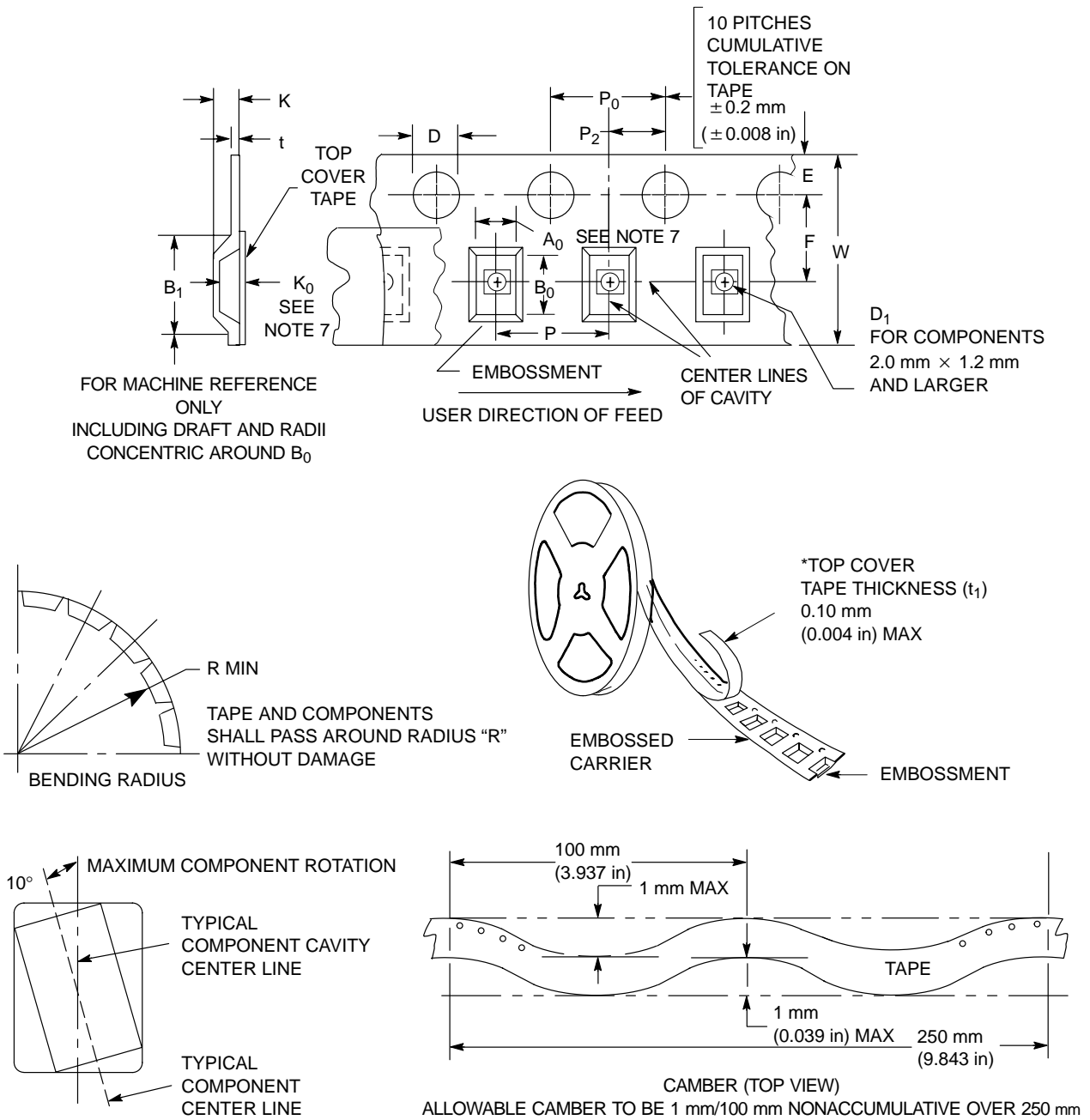


Figure 18. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.171 in)	1.5 +0.1/ -0.0 mm (0.059 +0.004/ -0.0 in)	1.0 mm Min (0.039 in)	1.75 +0.1 mm (0.069 +0.004 in)	3.5 +0.5 mm (1.38 +0.002 in)	2.4 mm (0.094 in)	4.0 +0.10 mm (0.157 +0.004 in)	4.0 +0.1 mm (0.156 +0.004 in)	2.0 +0.1 mm (0.079 +0.002 in)	25 mm (0.98 in)	0.3 +0.05 mm (0.01 +0.0038/ -0.0002 in)	8.0 +0.3 mm (0.315 +0.012 in)

6. Metric Dimensions Govern—English are in parentheses for reference only.

7. A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

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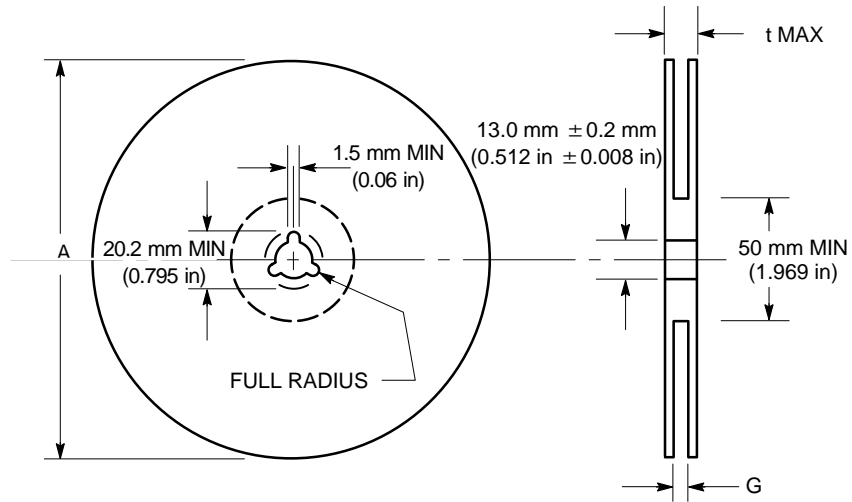


Figure 19. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, +1.5 mm, -0.0 (0.33 in + 0.059 in, -0.0)	14.4 mm (0.56 in)

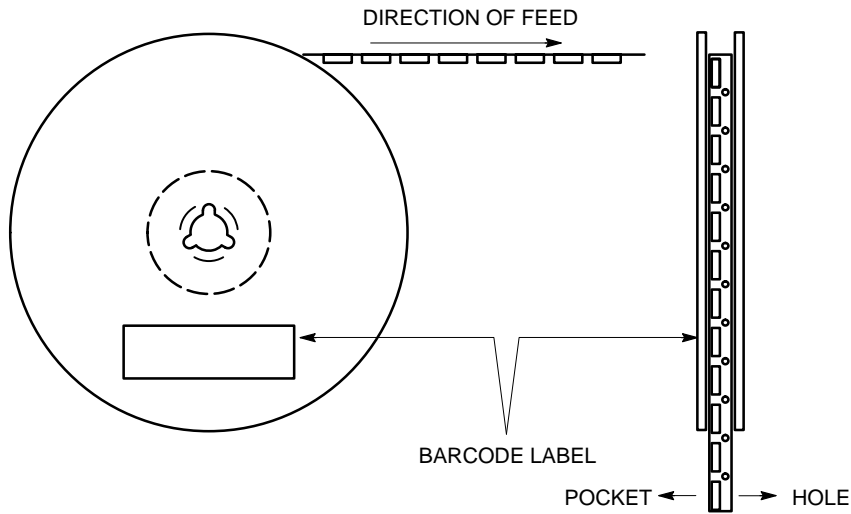


Figure 20. Reel Winding Direction

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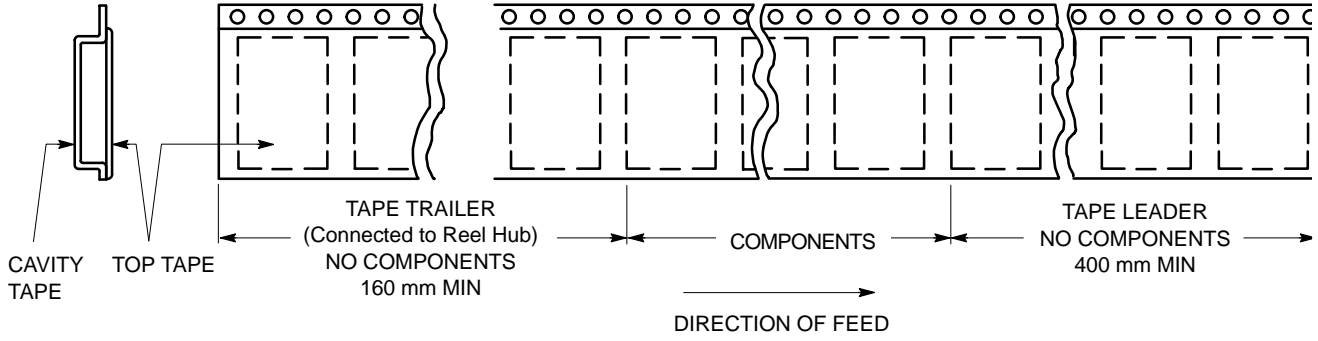


Figure 21. Tape Ends for Finished Goods

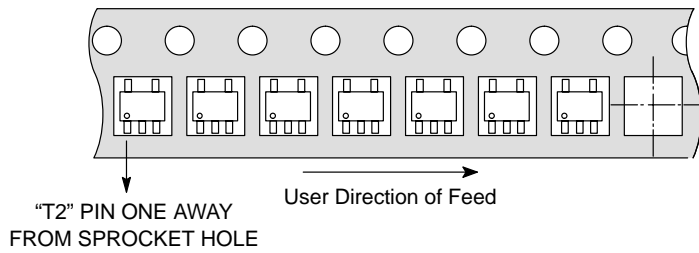


Figure 22. DFT2 (SC88A) Reel Configuration/Orientation

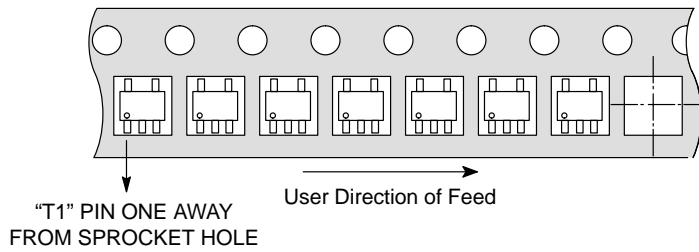
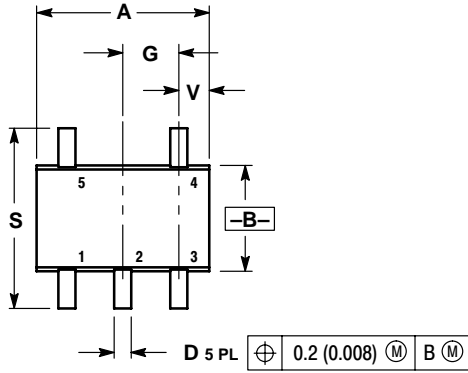


Figure 23. DTT1 (TSOP5) Reel Configuration/Orientation

NLAST4501

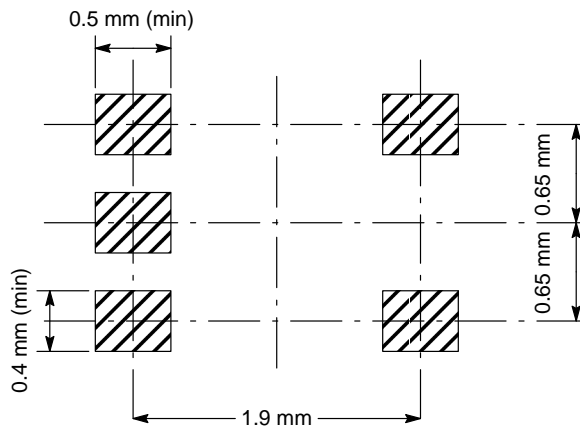
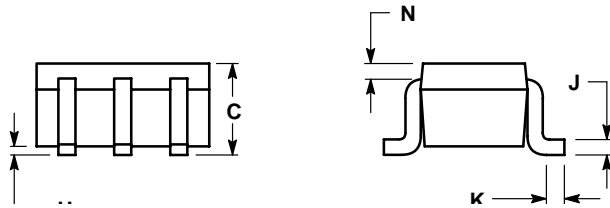
PACKAGE DIMENSIONS

SC-88A/SOT-353/SC-70
 DF SUFFIX
 5-LEAD PACKAGE
 CASE 419A-01
 ISSUE E



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

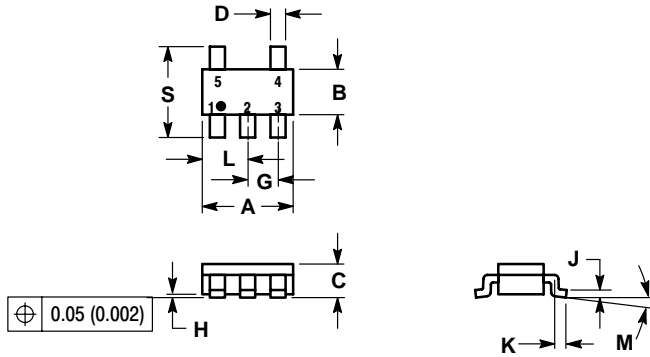
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40



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PACKAGE DIMENSIONS

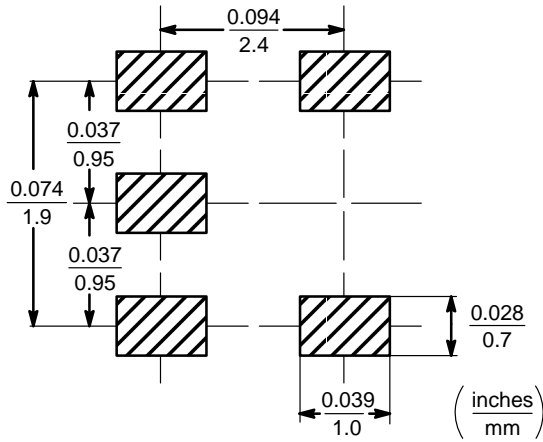
TSOP-5/SOT-23/SC-59
DT SUFFIX
5-LEAD PACKAGE
CASE 483-01
ISSUE A




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.00	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181



Notes

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