Chapter 7

Interface Guide

CHAPTER 7. INTERFACE GUIDE

CONTENTS

7. INTERFACE GUIDE

This chapter describes elements of the physical design of the DSP16 device that must be considered when designing practical physical systems. For timing characteristics and specifications, refer to an up-to-date *WE® DSP16 Digital Signal Processor* Data Sheet or *WE® DSP16A Digital Signal Processor* Data Sheet. For information concerning the 133-pin PGA package, refer to the *WE® DSP16 Digital Signal Processor For Military Applications* Data Sheet.

Note: When working with critical information, be sure it is the latest available. The date of publication can be found on the last page of data sheets and on the title page of manuals. Normally, data sheets are updated more frequently than information manuals.

7.1 PIN ASSIGNMENTS

Figure 7-1 is the pin diagram for the DSP16/DSP16A device. Table 7-1 is an alphabetical list of pin names.

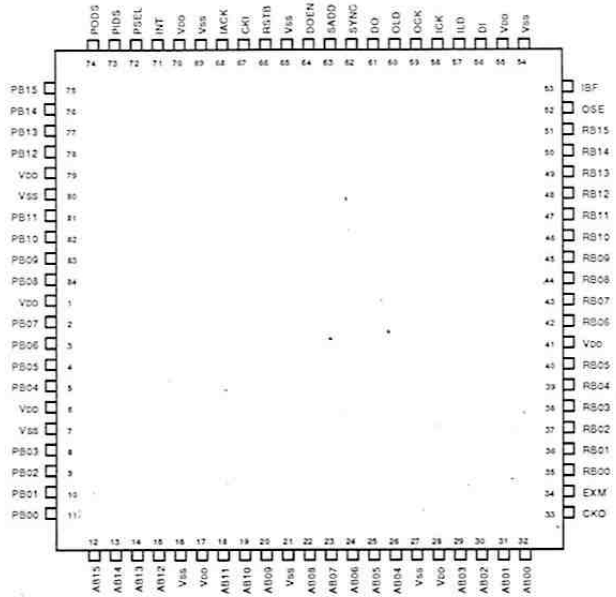

Figure 7-1. DSP16/DSP16A Digital Signal Processor – Pin Diagram

Table 7-1. DSP16/DSP16A Pin Names			
Symbol	Pin	Symbol	Pin
AB00—AB15	32—29, 26—22, 20—18, 15—12	OLD	60
		OSE	52
CKI	67	PB00—PB15	11—8, 5—2, 84—81, 78—75
CKO	33		
DI	56		
DO	61	PIDS	73
DOEN	64	PODS	74
EXM	34	PSEL	72
IACK	68	RB00—RB15	35—40, 42—51
IBF	53	RSTB	66
ICK	58	SADD	63
ILD	57	SYNC	62
INT	71	VDD	1, 6, 17, 28, 41, 55, 70, 79
OCK	59	VSS	7, 16, 21, 27, 54, 65, 69, 80

7.1.1 Device Pins by Numerical Order

Table 7-2. DSP16/DSP16A Pin Descriptions			
Pin	Symbol	Type*	Name/Description
1	VDD	P	5 V.
2	PB07	I/O†	Parallel I/O Data Bus – Bit 7.
3	PB06	I/O†	Parallel I/O Data Bus – Bit 6.
4	PB05	I/O†	Parallel I/O Data Bus – Bit 5.
5	PB04	I/O†	Parallel I/O Data Bus – Bit 4.
6	VDD	P	5 V.
7	VSS	P	Ground.
8	PB03	I/O†	Parallel I/O Data Bus – Bit 3.
9	PB02	I/O†	Parallel I/O Data Bus – Bit 2.
10	PB01	I/O†	Parallel I/O Data Bus – Bit 1.
11	PB00	I/O†	Parallel I/O Data Bus – Bit 0.
12	AB15	O†	ROM Address Bus – Bit 15.
13	AB14	O†	ROM Address Bus – Bit 14.
14	AB13	O†	ROM Address Bus – Bit 13.
15	AB12	O†	ROM Address Bus – Bit 12.

* I = Input; O = Output; P = Power Supply.
† 3-stated.

Table 7-2. DSP16/DSP16A Pin Descriptions (Continued)

Pin	Symbol	Type*	Name/Description
16	VSS	P	Ground.
17	VDD	P	5 V.
18	AB11	O†	ROM Address Bus – Bit 11.
19	AB10	O†	ROM Address Bus – Bit 10.
20	AB09	O†	ROM Address Bus – Bit 9.
21	VSS	P	Ground.
22	AB08	O†	ROM Address Bus – Bit 8.
23	AB07	O†	ROM Address Bus – Bit 7.
24	AB06	O†	ROM Address Bus – Bit 6.
25	AB05	O†	ROM Address Bus – Bit 5.
26	AB04	O†	ROM Address Bus – Bit 4.
27	VSS	P	Ground.
28	VDD	P	5 V.
29	AB03	O†	ROM Address Bus – Bit 3.
30	AB02	O†	ROM Address Bus – Bit 2.
31	AB01	O†	ROM Address Bus – Bit 1.
32	AB00	O†	ROM Address Bus – Bit 0.
33	CKO	O	**Clock Out.** Buffered clock at half the frequency of CKI.
34	EXM	I	**External Memory.** When high, all instructions and coefficients are fetched from external memory. When low: **DSP16** – forces use of internal ROM for instructions and coefficients. **DSP16A** – the first 4 Kwords of program memory are fetched from internal ROM; addresses beyond 4 Kwords are fetched from external memory.
35	RB00	I	ROM Data Bus – Bit 0.
36	RB01	I	ROM Data Bus – Bit 1.
37	RB02	I	ROM Data Bus – Bit 2.
38	RB03	I	ROM Data Bus – Bit 3.
39	RB04	I	ROM Data Bus – Bit 4.
40	RB05	I	ROM Data Bus – Bit 5.
41	VDD	P	5 V.
42	RB06	I	ROM Data Bus – Bit 6.
43	RB07	I	ROM Data Bus – Bit 7.
44	RB08	I	ROM Data Bus – Bit 8.
45	RB09	I	ROM Data Bus – Bit 9.
46	RB10	I	ROM Data Bus – Bit 10.

* I = Input; O = Output; P = Power Supply.
† 3-stated.

Table 7-2. DSP16/DSP16A Pin Descriptions (Continued)

Pin	Symbol	Type*	Name/Description
47	RB11	I	ROM Data Bus – Bit 11.
48	RB12	I	ROM Data Bus – Bit 12.
49	RB13	I	ROM Data Bus – Bit 13.
50	RB14	I	ROM Data Bus – Bit 14.
51	RB15	I	ROM Data Bus – Bit 15.
52	OSE	O†	**Output Shift Register Empty.** Indicates the end of a serial transmission. OSE is set either by emptying the output shift register or by asserting RSTB. OSE is reset by the DSP16 device writing a word to the output shift register.
53	IBF	O†	**Input Buffer Full.** IBF is set when the input buffer is filled and cleared by a read of the buffer. IBF is also cleared by asserting RSTB.
54	VSS	P	Ground.
55	VDD	P	5 V.
56	DI	I	Serial PCM data latched on rising edge of ICK, either LSB or MSB first, according to the status of the sioc register MSB field.
57	ILD	I/O†	**Input Load.** Falling edge of ILD indicates the beginning of a serial input word. In active mode, ILD is an output; in passive mode, ILD is an input, depending on the sioc register ILD field.
58	ICK	I/O†	**Input Clock.** Clock for serial PCM input data. In active mode, ICK is an output; in passive mode, ICK is an input, depending on the I/O format.
59	OCK	I/O†	**Output Clock.** Clock for serial PCM output data. In active mode, OCK is an output; in passive mode, OCK is an input, depending on the I/O format.
60	OLD	I/O†	**Output Load.** Clock for loading the parallel-to-serial converter from the output buffer (obuf). A falling edge of OLD indicates the beginning of a serial output word. In active mode, OLD is an output; in passive, OLD is an input, according to the sioc register OLD field.

* I = Input; O = Output; P = Power Supply.
† 3-stated.

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Table 7-2. DSP16/DSP16A Pin Descriptions (Continued)

Pin	Symbol	Type*	Name/Description
61	DO	O†	**Data Output.** Serial PCM data output from the output shift (osr) register, either LSB or MSB first, according to the sioc register MSB field. DO changes on the rising edges of OCK.
62	SYNC	I/O†	**Multiprocessor Synchronization.** A falling edge of SYNC indicates the first word of a TDM I/O stream. SYNC is an output when the tdms register transmit slot 0 is set; otherwise, it is input.
63	SADD	I/O†	**Multiprocessor Address (Active-Low).** An 8-bit serial bit stream used for addressing during multiprocessor communication between multiple DSP16 devices. SADD is an output when the tdms time slot dictates a serial transmission; otherwise, it is an input.
64	DOEN	I/O†	**Data Output Enable.** An output when in the multiprocessor mode (tdms register MODE field set) and an input otherwise. DO is 3-stated when DOEN is high.
65	VSS	P	**Ground.**
66	RSTB	I	**Reset.** A high-to-low transition causes entry into the reset state. The sioc, pioc (except bit 3, which is set), tdms, rb, and re register bits are cleared. Reset clears external flags IACK and IBF and sets external flag OSE. DAU condition flags and the auc register are not affected by reset. All output and bidirectional pins are 3-stated during reset. A low-to-high transition causes execution to begin at ROM location 0.
67	CKI	I	**Clock In.** Input clock at twice the frequency of internal operations.
68	IACK	O†	**Interrupt Acknowledge.** IACK signals when an interrupt is being serviced by the DSP16. The IACK remains high until normal instruction operation resumes.
69	VSS	P	**Ground.**
70	VDD	P	**5 V.**

* I = Input; O = Output; P = Power Supply.
† 3-stated.

Table 7-2. DSP16/DSP16A Pin Descriptions (Continued)

Pin	Symbol	Type*	Name/Description
71	INT	I	**Processor Interrupt.** Interrupt to DSP16. INT is acknowledged when interrupts are enabled by the pioc register.
72	PSEL	O†	**Peripheral Select.** PSEL is used in the input and output modes to address external devices. PSEL is low when register pdx0 is referenced, and high when pdx1 is referenced.
73	PIDS	I/O†	**Parallel Input Data Strobe.** Active mode (output) is controlled by data move instructions. Passive mode (input) is externally controlled. On low-to-high transition, data from the parallel I/O data bus is latched into the parallel input data register.
74	PODS	I/O†	**Parallel Output Data Strobe.** Active mode (output) is controlled by data move instructions. Passive mode (input) is externally controlled. When low, data from the parallel data output register is enabled into the parallel I/O data bus. The rising edge may be used as a latching clock. When high, the parallel I/O data bus is 3-stated.
75	PB15	I/O†	**Parallel I/O Data Bus – Bit 15**
76	PB14	I/O†	**Parallel I/O Data Bus – Bit 14**
77	PB13	I/O†	**Parallel I/O Data Bus – Bit 13**
78	PB12	I/O†	**Parallel I/O Data Bus – Bit 12**
79	VDD	P	**5 V.**
80	VSS	P	**Ground**
81	PB11	I/O†	**Parallel I/O Data Bus – Bit 11**
82	PB10	I/O†	**Parallel I/O Data Bus – Bit 10**
83	PB09	I/O†	**Parallel I/O Data Bus – Bit 9**
84	PB08	I/O†	**Parallel I/O Data Bus – Bit 8**

* I = Input; O = Output; P = Power Supply.
† 3-stated.

7.1.2 Pins by Functional Group

Table 7-3. External Memory Interface Group

Pin	Symbol	Type*	Name/Description
32	AB00		**ROM Address Bus – Bit 0.**
31	AB01		**ROM Address Bus – Bit 1.**
30	AB02		**ROM Address Bus – Bit 2.**
29	AB03		**ROM Address Bus – Bit 3.**
26	AB04		**ROM Address Bus – Bit 4.**
25	AB05		**ROM Address Bus – Bit 5.**
24	AB06		**ROM Address Bus – Bit 6.**
23	AB07		**ROM Address Bus – Bit 7.**
22	AB08	O†	**ROM Address Bus – Bit 8.**
20	AB09		**ROM Address Bus – Bit 9.**
19	AB10		**ROM Address Bus – Bit 10.**
18	AB11		**ROM Address Bus – Bit 11.**
15	AB12		**ROM Address Bus – Bit 12.**
14	AB13		**ROM Address Bus – Bit 13.**
13	AB14		**ROM Address Bus – Bit 14.**
12	AB15		**ROM Address Bus – Bit 15.**
34	EXM	I	**External Memory.** When high, all instructions and coefficients are fetched from external memory. When low: **DSP16** – forces use of internal ROM for instructions and coefficients. **DSP16A** – the first 4 Kwords of program memory are fetched from internal ROM; addresses beyond 4 Kwords are fetched from external memory.
35	RB00		**ROM Data Bus – Bit 0.**
36	RB01		**ROM Data Bus – Bit 1.**
37	RB02		**ROM Data Bus – Bit 2.**
38	RB03		**ROM Data Bus – Bit 3.**
39	RB04		**ROM Data Bus – Bit 4.**
40	RB05		**ROM Data Bus – Bit 5.**
42	RB06		**ROM Data Bus – Bit 6.**
43	RB07	I	**ROM Data Bus – Bit 7.**
44	RB08		**ROM Data Bus – Bit 8.**
45	RB09		**ROM Data Bus – Bit 9.**
46	RB10		**ROM Data Bus – Bit 10.**
47	RB11		**ROM Data Bus – Bit 11.**
48	RB12		**ROM Data Bus – Bit 12.**
49	RB13		**ROM Data Bus – Bit 13.**
50	RB14		**ROM Data Bus – Bit 14.**
51	RB15		**ROM Data Bus – Bit 15.**

* I = Input; O = Output
† 3-stated.

Table 7-4. SIO Interface Group

Pin	Symbol	Type*	Name/Description
52	OSE	O†	**Output Shift Register Empty.** Indicates the end of a serial transmission. OSE is set either by emptying the output shift register or by asserting RSTB. OSE is reset by the DSP16 writing a word to the output shift register.
53	IBF	O†	**Input Buffer Full.** IBF is set when the input buffer is filled and cleared by a read of the buffer. IBF is also cleared by asserting RSTB.
56	DI	I	**Data Input.** Serial PCM data latched on rising edge of ICK, either LSB or MSB first, according to the status of the sioc register MSB field.
57	ILD	I/O†	**Input Load.** Falling edge of ILD indicates the beginning of a serial input word. In active mode, ILD is an output; in passive mode, ILD is an input, depending on the sioc register ILD field.
58	ICK	I/O†	**Input Clock.** Clock for serial PCM input data. In active mode, ICK is an output; in passive mode, ICK is an input, depending on the I/O format.
59	OCK	I/O†	**Output Clock.** Clock for serial PCM output data. In active mode, OCK is an output; in passive mode, OCK is an input, depending on the I/O format.
60	OLD	I/O†	**Output Load.** Clock for loading the parallel-to-serial converter from the output buffer (obuf). A falling edge of OLD indicates the beginning of a serial output word. In active mode, OLD is an output; in passive mode, OLD is an input, according to the sioc register OLD field.
61	DO	O†	**Data Output.** Serial PCM data output from the output shift (osr) register, either LSB or MSB first, according to the sioc register MSB field. DO changes on the rising edges of OCK.

* I = Input; O = Output
† 3-stated.

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Table 7-4. SIO Interface Group (Continued)			
Pin	Symbol	Type*	Name/Description
62	SYNC	I/O†	**Multiprocessor Synchronization.** A falling edge of SYNC indicates the first word of a TDM I/O stream. SYNC is an output when the tdms register transmit slot 0 is set; otherwise, it is an input.
63	SADD	I/O†	**Multiprocessor Address (Active-Low).** An 8-bit serial bit stream used for addressing during multiprocessor communication between multiple DSP16 devices. SADD is an output when the tdms time slot dictates a serial transmission; otherwise, it is an input.
64	DOEN	I/O†	**Data Output Enable.** An output when in the multiprocessor mode (tdms register MODE field set) and an input otherwise. DO is 3-stated when DOEN is high.

Table 7-5. PIO Interface Group			
Pin	Symbol	Type*	Name/Description
11	PDB00	I/O†	**Parallel I/O Data Bus – Bit 0.**
10	PDB01		**Parallel I/O Data Bus – Bit 1.**
9	PDB02		**Parallel I/O Data Bus – Bit 2.**
8	PDB03		**Parallel I/O Data Bus – Bit 3.**
5	PDB04		**Parallel I/O Data Bus – Bit 4.**
4	PDB05		**Parallel I/O Data Bus – Bit 5.**
3	PDB06		**Parallel I/O Data Bus – Bit 6.**
2	PDB07		**Parallel I/O Data Bus – Bit 7.**
84	PDB08		**Parallel I/O Data Bus – Bit 8.**
83	PDB09		**Parallel I/O Data Bus – Bit 9.**
82	PDB10		**Parallel I/O Data Bus – Bit 10.**
81	PDB11		**Parallel I/O Data Bus – Bit 11.**
78	PDB12		**Parallel I/O Data Bus – Bit 12.**
77	PDB13		**Parallel I/O Data Bus – Bit 13.**
76	PDB14		**Parallel I/O Data Bus – Bit 14.**
75	PDB15		**Parallel I/O Data Bus – Bit 15.**

* I = Input; O = Output
† 3-stated.

Table 7-5. PIO Interface Group (Continued)			
Pin	Symbol	Type*	Name/Description
72	PSEL	O†	**Parallel Select.** PSEL is used to address external devices. PSEL is low when pdx0 is referenced and high when pdx1 is referenced.
73	PIDS	I/O†	**Parallel Input Data Strobe.** Active mode (output) is controlled by the data move instructions. Passive mode (input) is externally controlled. On low-to-high transition, data from the parallel I/O data bus is latched into the parallel input data register.
74	PODS	I/O†	**Parallel Output Data Strobe.** Active mode (output) is controlled by the data move instructions. Passive mode (input) is externally controlled. When low, data from the parallel data output register is placed into the parallel data bus. The rising edge may be used as a latching clock. When high, the parallel I/O data bus is 3-stated.

Table 7-6. Miscellaneous Function Group			
Pin	Symbol	Type*	Name/Description
33	CKO	O†	**Clock Out.** Buffered clock at half the frequency of CKI.
66	RSTB	I	**Reset.** A high-to-low transition causes entry into the reset state. The sioc, pioc (except bit 3, which is set), tdms, rb, and re register bits are cleared. Reset clears external flags IACK and IBF and sets external flag OSE. DAU condition flags and the auc register are not affected by reset. All output and bidirectional pins are 3-stated during reset. A low-to-high transition causes execution to begin at ROM location 0.
67	CKI	I	**Clock In.** Input clock at twice the frequency of internal operations.
68	IACK	O†	**Interrupt Acknowledge.** Interrupt acknowledge signals when an interrupt is being serviced by the DSP16 device. The IACK remains high until normal instruction operation resumes.
71	INT	I	**Processor Interrupt.** Interrupt to DSP16 device. INT is acknowledged when interrupts are enabled by the pioc register.

* I = Input; O = Output
† 3-stated.

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Table 7-7. Power and Ground Group			
Pin	Symbol	Type*	Name/Description
1	VDD	P	5 V.
6	VDD		5 V.
17	VDD		5 V.
28	VDD		5 V.
41	VDD		5 V.
55	VDD		5 V.
70	VDD		5 V.
79	VDD		5 V.
7	VSS	P	Ground.
16	VSS		Ground.
21	VSS		Ground.
27	VSS		Ground.
54	VSS		Ground.
65	VSS		Ground.
69	VSS		Ground.
80	VSS		Ground.

* P = Power Supply.

7.2 ELECTRICAL CHARACTERISTICS

The parameters are valid for the following conditions: T_C = 0 to 85 °C; V_{DD} = 5 V ± 10%; V_{SS} = 0 V; t = 2 × tCKIHCKIH.

Table 7-8. Electrical Characteristics				
Parameter	Sym	Min	Max	Unit
Input Voltage				
Low	V_{IL}	—	0.8	V
High	V_{IH}	2.0	—	V
Output Voltage				
Low (I_{OL}=2.0 mA)	V_{OL}	—	0.4	V
High (I_{OH}= –2.0 mA)	V_{OH}	2.4	—	V
Output Current				
Low (I_{OL}=0.4 V)	I_{OL}	—	2.0	mA
High (I_{OH}=2.4 V)	I_{OH}	—	–2.0	mA
Output Short-Circuit Current (V_{OH}=0 V)	I_{OS}	—	–200	mA
Output 3-State Current				
Low (V_{IL} = 0.8)	I_{OZL}	–75	75	µA
High (V_{IH} = 2.0)	I_{OZH}	–75	75	µA
Input Current				
Low (V_{IL} = 0.8)	I_{IL}	—	–25	µA
High (V_{IH} = 2.0)	I_{IH}	—	25	µA
Input Capacitance	C_I	—	15	pF

Absolute Maximum Ratings

Voltage on any pin with respect to ground ..... –0.5 V to +6 V
Power dissipation ..... 1 W
Ambient temperature range ..... –40 °C to +120 °C
Storage temperature range ..... –65 °C to +150 °C

Maximum ratings are the limiting conditions that can be applied to all variations of circuit and environmental conditions without the occurrence of permanent damage.

Bonding and soldering of the external leads of these devices can be performed safely at temperatures up to 300 °C.

7.3 EXTERNAL MEMORY

Figure 7-2 shows the external memory interface timing. Note that there are no read or write signals. The external memory interface was primarily provided to allow users to place programs in external ROM, rather than having to order mask-programmed devices. In some applications, such as the DSP16 and DSP16A Development Systems, the external memory is RAM, which is loaded by a microcomputer and then read by the DSP16/DSP16A device.

DSP16 Only

When the EXM pin is tied high, the internal ROM of the device can be replaced with up to 64 Kwords of external memory. The address space starts at address zero. Addresses are generated by the XAAU (ROM addressing unit) and supplied off-chip on the address bus (AB00—AB15).

DSP16A Only

When the EXM pin is tied low, the processor augments the low 4 Kwords of on-chip program ROM with up to 60 Kwords of external program memory. When the EXM pin is tied high, the entire 64 Kword address space is mapped into external program memory.

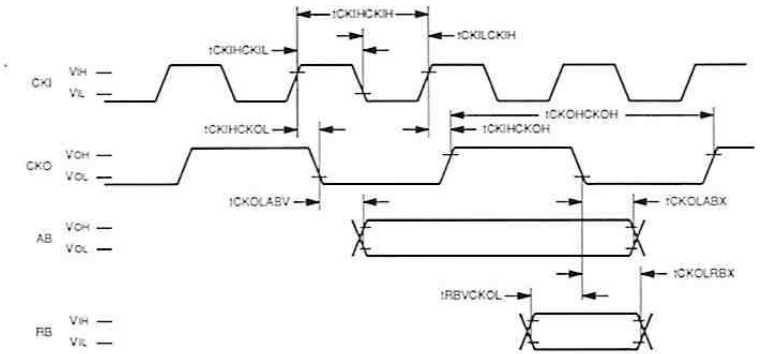
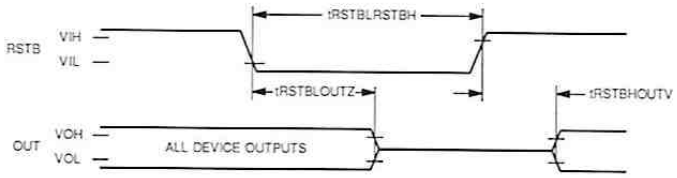


Figure 7-2. External Memory Interface Timing

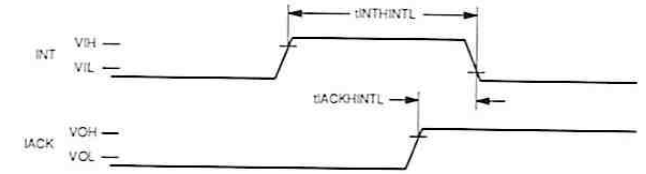
7.4 RESET AND INTERRUPT CONTROL

The DSP16/DSP16A device can be reset by the use of the RSTB input. Asserting RSTB (low) causes all device outputs to 3-state. The next low-to-high transition causes the device to begin program execution from address zero. Part A of Figure 7-3 shows the timing of the RSTB input and device outputs.

Part B of Figure 7-3 shows the timing of the INT (interrupt request) input. When an external device requests an interrupt, the DSP16 device recognizes an interrupting condition at the next interruptible instruction (provided the INT interrupt enable bit in the pioc register is set), the interrupt acknowledge signal (IACK) is asserted, and program execution branches to address one. At the end of the interrupt service routine, as determined by the iretum instruction, IACK is negated.



A. Reset Timing



B. Interrupt Timing

Figure 7-3. Reset and Interrupt Timing

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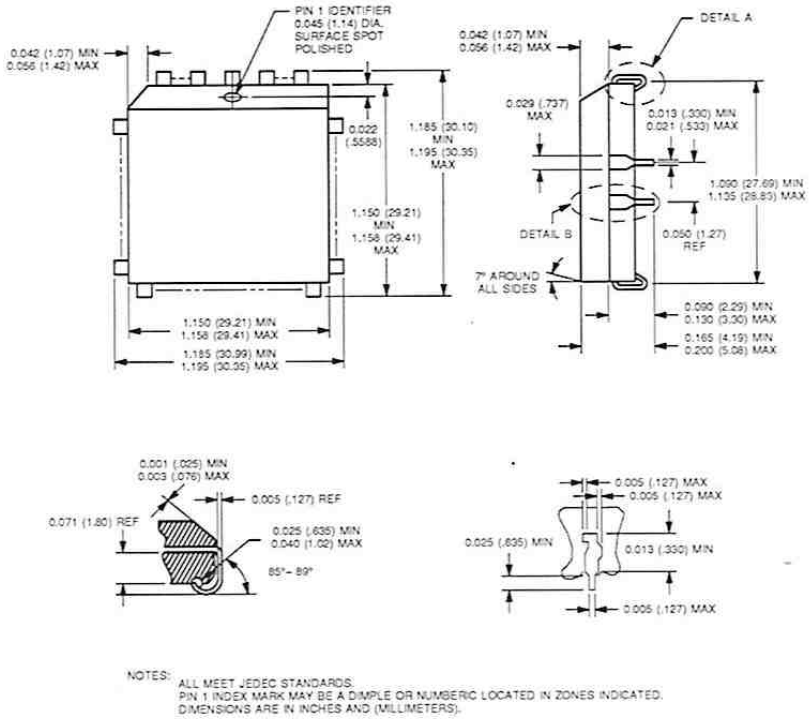
7.5 DEVICE PACKAGE OUTLINE



NOTES: ALL MEET JEDEC STANDARDS.
PIN 1 INDEX MARK MAY BE A DIMPLE OR NUMBERIC LOCATED IN ZONES INDICATED.
DIMENSIONS ARE IN INCHES AND (MILLIMETERS).

Figure 7-4. 84-Pin PLCC Device Outline