S5K433CA, S5K433LA
(1/4” VGA CMOS Image Sensor)

Preliminary Specification

Revision 0.3.1

July 2002

DOCUMENT TITLE

1/4" Optical Size 640x480(VGA) 3.3V/2.8V CMOS Image Sensor

REVISION HISTORY

Revision No.	History	Draft Date	Remark
0.0	Initial Draft	Feb. 16, 2002	Preliminary
0.1	Pin description error corrected (LHOLD polarity). Timing chart added.	Feb. 21, 2002	Preliminary
0.2	STRB signal polarity error corrected SFCM timing diagram corrected Operation description added.	Apr. 10, 2002	Preliminary
0.3	DC timing characteristics specification changed AC timing characteristics specification changed STRB and LHOLD pins are deleted	July 8, 2002	Preliminary
0.3.1	Minor description error corrected	July 15, 2002	Preliminary

INTRODUCTION

The S5K433CA and S5K433LA are highly integrated single chip CMOS image sensors fabricated by SAMSUNG 0.35μm CMOS image sensor process technology. It is developed for imaging application to realize high-efficiency and low-power photo sensor. The sensor has 640 x 480 effective pixels with 1/4 inch optical format. The sensor has on-chip 10-bit ADC blocks to digitize the pixel output and also on-chip CDS to reduce Fixed Pattern Noise (FPN) drastically. With its few interface signals and 10-bit raw data directly connected to the external devices, a camera system can be configured easily. S5K433CA is suitable for a camera system with standard 3.3V logic operation and S5K433LA is suitable for low power camera module with 2.8V power supply.

FEATURES

- Process Technology: 0.35μm DPTM CMOS
- Optical Size: 1/4 inch
- Unit Pixel: 5.6 μm X 5.6 μm
- Effective Resolution: 640X480, VGA
- Line Progressive Read Out.
- 10-bit Raw Image Data Output
- Programmable Exposure Time
- Programmable Gain Control
- Auto Dark Level Compensation
- Windowing and Panning
- Sub-Sampling (2X, 3X, 4X)
- Standby-Mode for Power Saving
- Maximum 36 Frame per Second
- Bad Pixel Replacement
- Single Power Supply Voltage: 3.3V or 2.8V
- Package Type: 48-CLCC/PLCC

PRODUCTS

Product Code	Power Supply	Backend Process	Description
S5K433CA01	3.3 V	None	Monochrome image sensor
S5K433LA01	2.8 V		
S5K433CA02	3.3 V	On-chip micro lens	High sensitivity monochrome Image sensor
S5K433LA02	2.8 V		
S5K433CA03	3.3 V	On-chip color filter and micro lens	RGB color image sensor
S5K433LA03	2.8 V		

BLOCK DIAGRAM

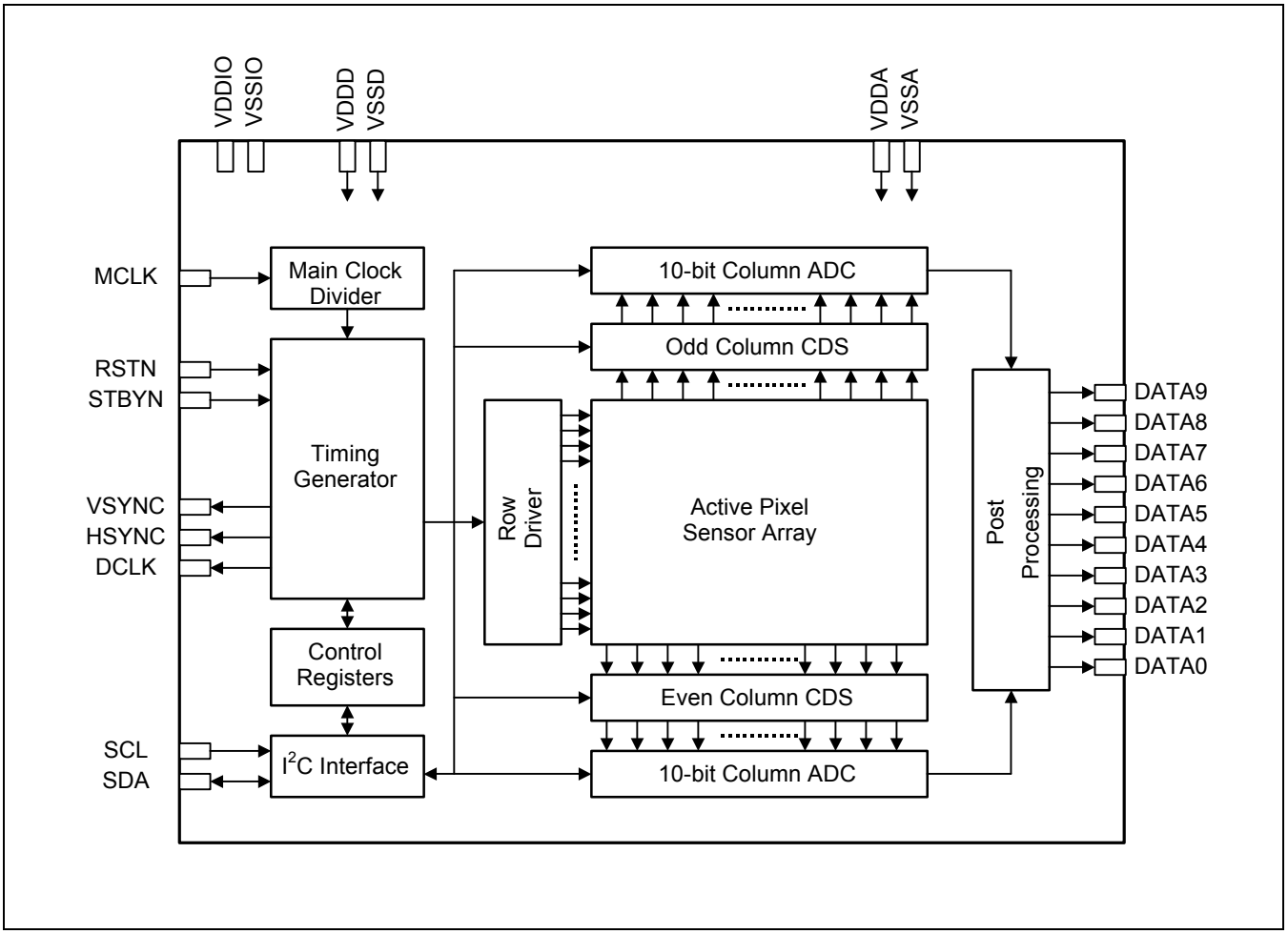


Figure 1. Block Diagram

PIXEL ARRAY

(TOP VIEW ON CHIP. DISPLAYED IMAGE WILL BE FLIPPED.)

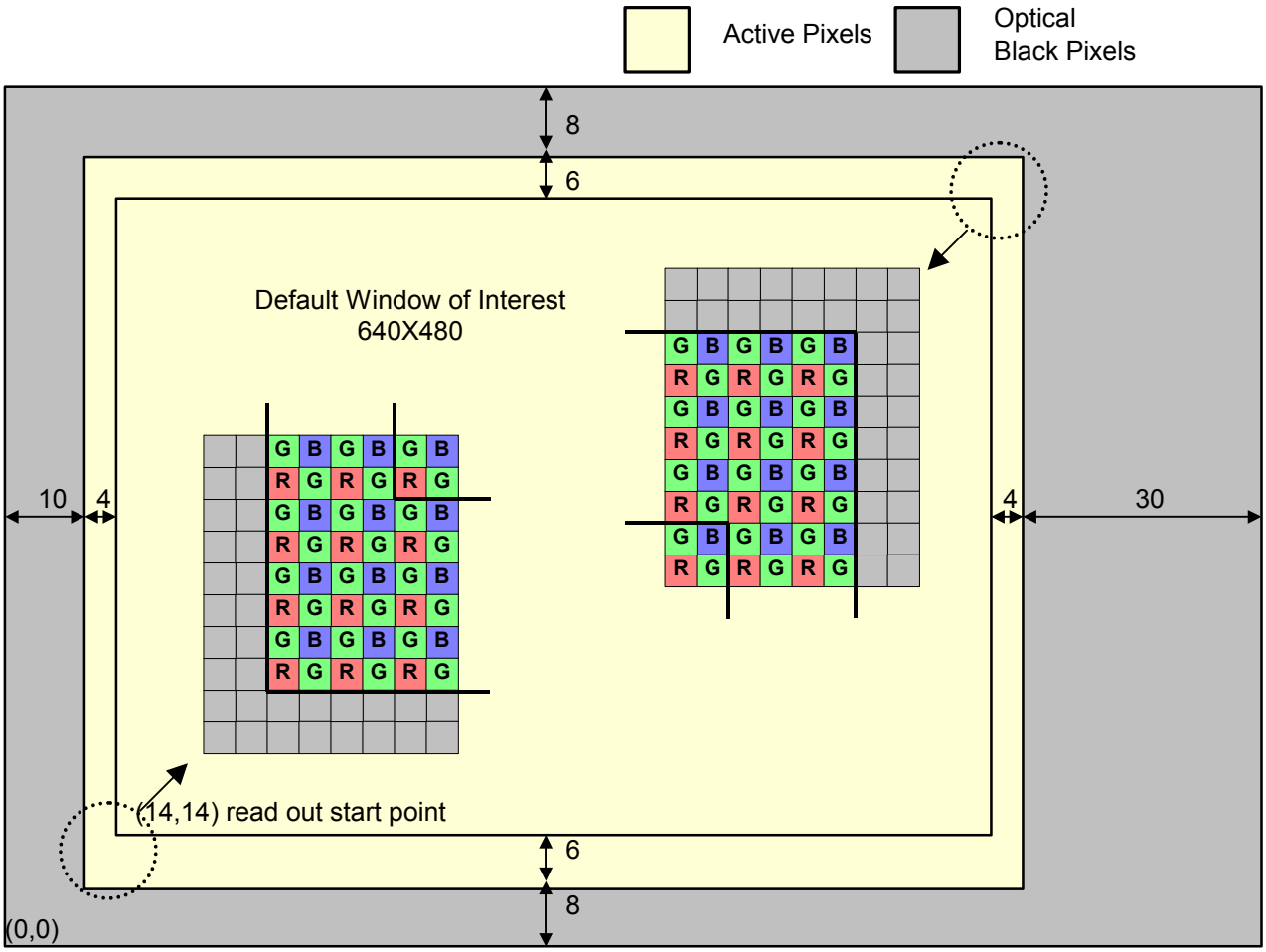


Figure 2. Pixel Array Configuration

PIN CONFIGURATION

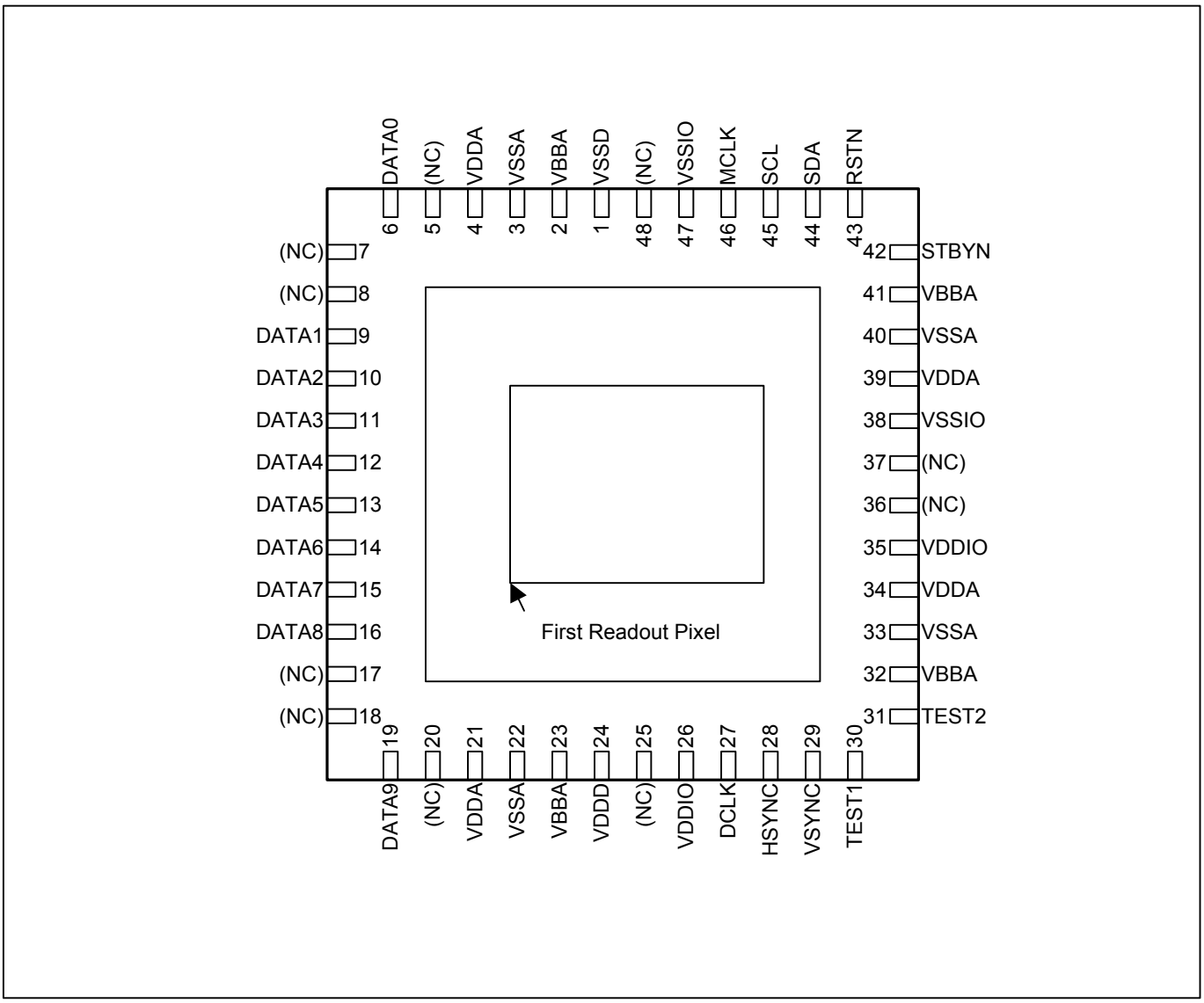


Figure 3. Pin Configuration

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit
Operating voltage (VDDD, VDDIO, VDDA supply relative to VSSD, VSSIO, VSSA, VBBA)	V_{DD}	-0.3 to 3.8	V
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3 (Max. 3.8)	
Operating temperature	T_{OPR}	-20 to +60	°C
Storage temperature	T_{STG}	-40 to +125(1)	
		-40 to +85(2)	

NOTES:

1. The maximum allowed storage temperature for S5K433C(L)X01.
2. The maximum allowed storage temperature for S5K433C(L)X02 and S5K433C(L)X03.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(T_A = -20 to +60°C, C_L = 15pF)

Characteristics	Symbol	Condition		Min	Typ	Max	Unit
Operating voltage	V_{DD}	VDDD, VDDIO, VDDA	S5K433CA	3.0	3.3	3.6	V
			S5K433LA	2.55	2.8	3.05	
Input voltage (1)	V_{IH}	-		$0.8V_{DD}$	-	-	
	V_{IL}	-		0	-	$0.2V_{DD}$	
Input leakage current(2)	I_{IL}	V_{IN} = V_{DD} to V_{SS}		-10	-	10	µA
Input leakage current with pull-down(3)	I_{ILD}	V_{IN} = V_{DD}		10	30	60	
High Level Output voltage (4)	V_{OH}	I_{OH} = -1µA		V_{DD}-0.05	-	-	V
		I_{OH} = -4mA	S5K433CA	2.4	-	-	
			S5K433LA	1.9	-	-	
Low Level Output voltage (5)	V_{OL}	I_{OL} = 1µA		-	-	0.05	
		I_{OL} = 4mA		-	-	0.4	
High-Z output leakage current (6)	I_{OZ}	V_{OUT} = V_{DD}		-	-	10	µA
Supply current	I_{STB}	STBYN=Low(Active) All input clocks = Low		-	-	10	µA
	I_{DD}	f_{MCLK} = 24.54MHz 0 lux illumination	V_{DD} = 3.3V (7)	-	27	-	mA
			V_{DD} = 2.8V (8)	-	18	-	

NOTES:

1. Applied to MCLK, RSTN, STBYN, SCL, SDA, TEST1, TEST2 pin.
2. MCLK, RSTN, STBYN, SCL, SDA pin
3. TEST1, TEST2 pin
4. DCLK, HSYNC, VSYNC, DATA0 to DATA9 pin
5. DCLK, HSYNC, VSYNC, DATA0 to DATA9, SCL, SDA pin
6. SDA pin when in High-Z output state
7. S5K433CA
8. S5K433LA

Imaging Characteristics

(Light source with 3200K of color temperature and IR cut filter (CM-500S, 1mm thickness) is used. Electrical operating conditions follow the recommended typical values. The control registers are set to the default values. T_A = 25◦C if not specified.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Saturation level(1)	V_{SAT}	S5K433CA	950	1000	-	mV
		S5K433LA	850	900	-	
Sensitivity(2)	S	S5K433(C,L)X01	-	1500	-	mV/lux sec
		S5K433(C,L)X02	-	4000	-	
		S5K433(C,L)X03	-	1500	-	
Dark level(3)	V_{DARK}	T_A = 40◦C	-	9	18	mV/sec
		T_A = 60◦C	-	50	100	
Dynamic range(4)	DR		-	60	-	dB
Signal to noise ratio(5)	S/N		-	40	-	
Dark signal non-uniformity(6)	DSNU	T_A = 60◦C	-	-	100	mV/sec
Photo response non-uniformity(7)	PRNU		-	4	8	%
Vertical fixed pattern noise(8)	VFPN			4	8	%
Horizontal fixed pattern noise(9)	HFPN			4	8	%

NOTES:

1. Measured minimum output level at 100 lux illumination for exposure time 1/30 sec. 7X7 rank filter is applied for the whole pixel area to eliminate the values from defective pixels.
2. Measured average output at 25% of saturation level illumination for exposure time 1/30 sec. Green channel output values are used for color version.
3. Measured average output at zero illumination without any offset compensation for exposure time 1/30 sec.
4. 20 log (saturation level/ dark level rms noise excluding fixed pattern noise). 60dB is limited by 10-bit ADC.
5. 20 log (average output level/rms noise excluding fixed pattern noise) at 25% of saturation level illumination for exposure time 1/30 sec.
6. Difference between maximum and minimum pixel output levels at zero illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
7, Difference between maximum and minimum pixel output levels divided by average output level at 25% of saturation level illumination for exposure time 1/30 sec. 7X7 median filter is applied for the whole pixel area to eliminate the values from defective pixels.
8. For the column-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 columns at 25% of saturation level illumination for exposure time 1/30 sec.
9. For the row-averaged pixel output values, maximum relative deviation of values from 7-depth median filtered values for neighboring 7 columns at 25% of saturation level illumination for exposure time 1/30 sec.

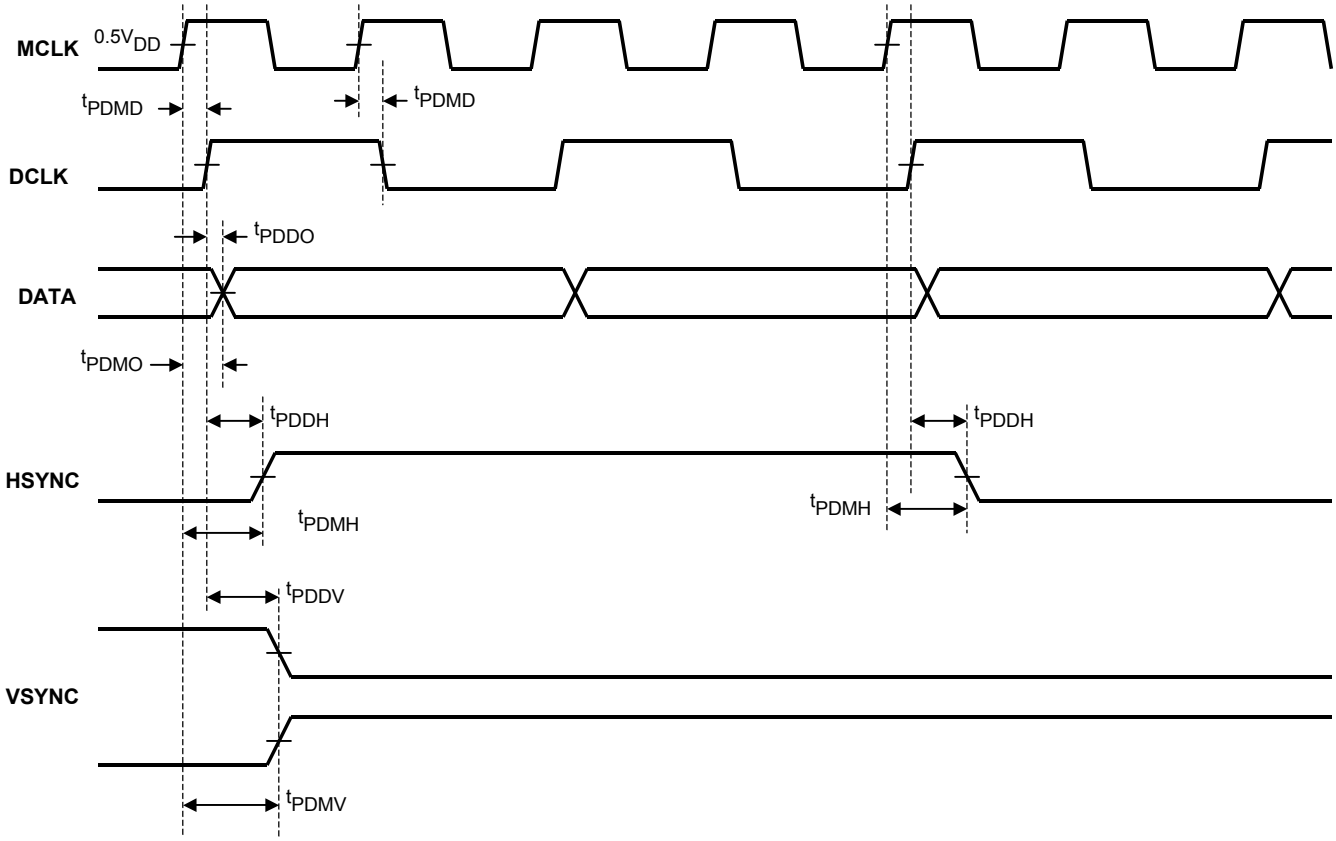
AC Characteristics

(V_{DD} = 3.0V to 3.6V for S5K433CA, V_{DD} = 2.55V to 3.05V for S5K433LA, Ta = -20 to + 60°C, C_L = 50pF)

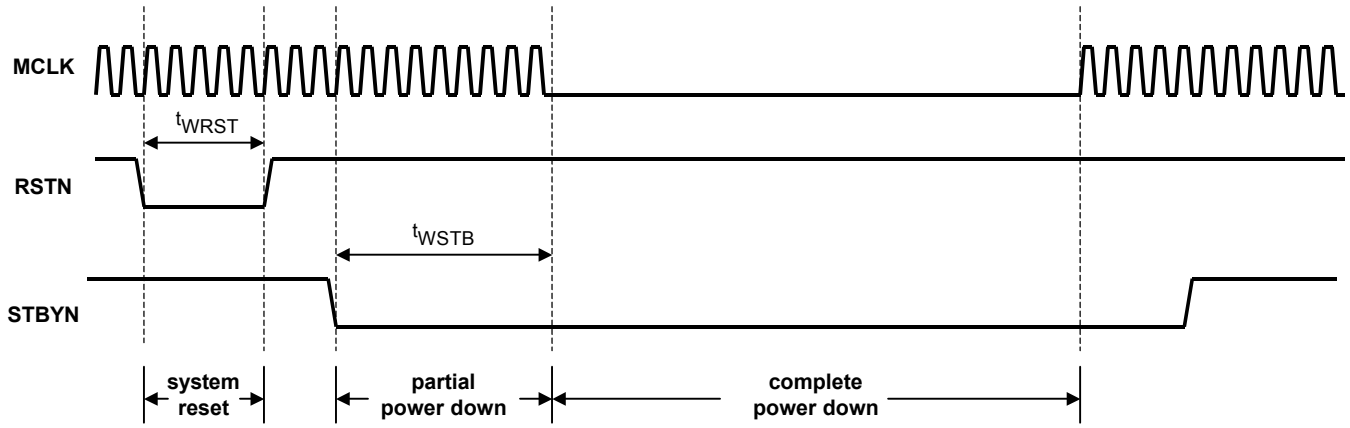
Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Main input clock frequency	f_{MCLK}	Duty = 50%	3(1)	24.54	30	MHz
Data output clock frequency	f_{DCLK}	-	2	12.27	15	
Propagation delay time from main input clock	t_{PDMD}	DCLK output	-	-	20	ns
	t_{PDMO}	DATA output	-	-	25	
	t_{PDMH}	HSYNC output	-	-	25	
	t_{PDMV}	VSYNC output	-	-	25	
Propagation delay time from data output clock	t_{PDDO}	DATA output	-	-	10	
	t_{PDDH}	HSYNC output	-	-	10	
	t_{PDDV}	VSYNC output	-	-	10	
Reset input pulse width	t_{WRST}	RSTN=low(active)	5	-	-	T_{MCLK}(2)
Standby input pulse width	t_{WSTB}	STBYN=low(active)	4	-	-	

NOTES:

1. 8-bit ADC resolution case. If 10-bit ADC resolution is used, the frequency should be over 12MHz.
2. The period time of main input clock, **MCLK**.

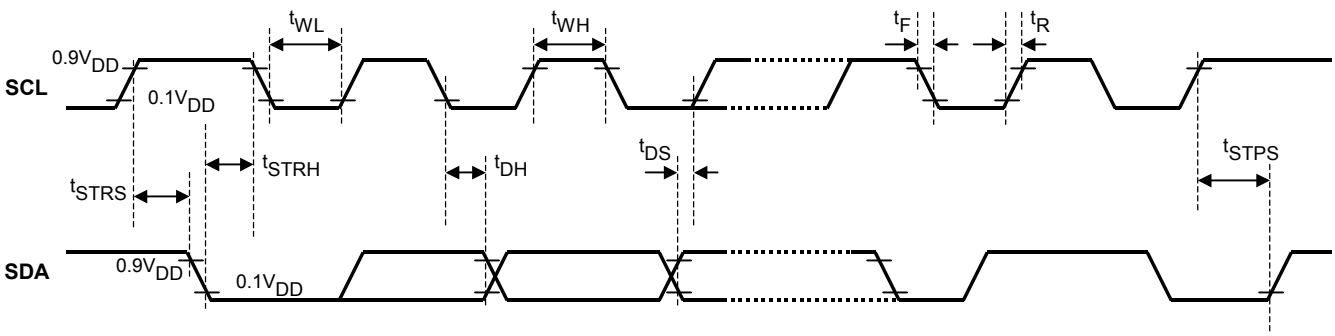


SAMSUNG ELECTRONICS



I²C Serial Interface Characteristics

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Clock frequency	f_{SCK}	-	-	-	400	kHz
Clock high pulse width	t_{WH}	SCL	800	-	-	ns
Clock low pulse width	t_{WL}	SCL	1000	-	-	
Clock rise/fall time	t_R/t_F	SCL, SDA	-	-	300	
Data set-up time	t_{DS}	SDA to SCL	300	-	-	
Data hold time	t_{DH}	SDA to SCL	1200	-	-	
START condition hold time	t_{STH}	-	4			T_{MCLK}
STOP condition setup time	t_{STS}	-	4	-	-	
STOP to new START gap	t_{GSS}	-	8	-	-	
Capacitance for each pin	C_{PIN}	SCL, SDA	-	-	4	pF
Capacitive bus load	C_{BUS}	SCL, SDA	-	-	200	
Pull-up resistor	R_{PU}	SCL, SDA to V_{DD}	1.5	-	10	kΩ



PIN DESCRIPTION

Pin No	I/O	Name	Function
VDDD (24)	Power	Digital power supply	For logical circuit (V_{DD} ± 10%)
VSSD (1)	Power		0V (GND)
VDDIO (26, 35)	Power	I/O power supply	For I/O circuit (V_{DD} ± 10%)
VSSIO (47, 38)	Power		0V (GND)
VDDA (4, 21, 34, 39)	Power	Analog power supply	For analog circuit (V_{DD} ± 10%)
VSSA (3, 22, 33, 40)	Power		0V (GND)
VBBA (2, 23, 32, 41)	Power		For analog circuit bulk bias (0V)
MCLK (46)	I	Master clock	Master clock pulse input for all timing generators.
RSTN (43)	I	Reset	Initializing all the device registers. (Active low)
STBYN (42)	I	Standby	Activating power saving mode. (high=normal operation, low=power saving mode)
DATA0~DATA9 (6, 9~16, 19)	O	Image data output	10-bit image data outputs. When ADC resolution is reduced, the unused lower bits are set to 0.
DCLK (27)	O	Data clock	Image data output synchronizing pulse output.
HSYNC (28)	O	Horizontal sync clock	Horizontal synchronizing pulse or data valid signal output.
VSYNC (29)	O	Vertical sync clock	Vertical synchronizing pulse or line valid signal output.
SCL (45)	I	Serial interface clock	I2C serial interface clock input
SDA (44)	I/O	Serial interface data	I2C serial interface data bus (external pull-up resistor required)
TEST1 (30)	I	Test input 1	Test input signal. Though it can be opened in normal operation (internally pulled down), it is recommended to ground the test pins.
TEST2 (31)	I	Test input 2	Test input signal. Though it can be opened in normal operation (internally pulled down), it is recommended to ground the test pins.

CONTROL REGISTERS

Address (Hex)	Reset Value	Bits	Mnemonic	Description
00h	02h	[5]	**bprm**	Bad pixel replacement mode 0b: disabled (default), 1b: enabled
		[4]	**dlcm**	Dark level compensation mode 0b: manual (default), 1b: auto
		[3]	**ccsm**	Color channel separation mode 0b: not separated (default), 1b: separated
		[2]	**shutc**	Electronic shutter mode 0b: disabled (default), 1b: enabled
		[1:0]	**adcres**	ADC resolution 00b: 8-bit, 01b: 9-bit, 10b: 10-bit (default)
01h	10h	[7]	**mircv**	Vertical mirror control 0b: normal (default), 1b: mirrored
		[6]	**mirch**	Horizontal mirror control 0b: normal (default), 1b: mirrored
		[5:4]	**mcdiv**	Main clock divider 00b: DCLK=MCLK, 01b: DCLK=MCLK÷2 (default) 10b: DCLK=MCLK÷4, 11b: DCLK=MCLK÷8
		[3:2]	**subsr**	Row subsampling mode 00b: disabled (default), 01b: 2X, 10b: 3X, 11b: 4X
		[1:0]	**subsc**	Column subsampling mode 00b: disabled (default), 01b: 2X, 10b: 3X, 11b: 4X
02h	00h	[0]	**wrp_high**	Row start point for window of interest wrp[8:0] = 14d(default)
03h	0Eh	[7:0]	**wrp_low**	
04h	00h	[0]	**wcp_high**	Column start point for window of interest wcp[8:0] = 14d(default)
05h	0Eh	[7:0]	**wcp_low**	
06h	01h	[0]	**wrd_high**	Row depth for window of interest wrd[8:0] = 480d(default)
07h	E0h	[7:0]	**wrd_low**	
08h	02h	[1:0]	**wcw_high**	Column width for window of interest wcw[9:0] = 640d(default)
09h	80h	[7:0]	**wcw_low**	
0Ah	80h	[7:0]		(Factory use only))

Address (Hex)	Reset Value	Bits	Mnemonic	Description
0Bh	02h	[4]		(factory use only)
		[3]		
		[2:0]		
0Ch	0Dh	[7:0]		
0Dh	01h	[4:0]	**cintr_high**	Row-step integration time in continuous frame capture mode cintr[12:0] = 262d (default)
0Eh	06h	[7:0]	**cintr_low**	
0Fh	00h	[5:0]	**cintc_high**	Column-step integration time in continuous frame capture mode cintc[13:0] = 0d (default)
10h	00h	[7:0]	**cintc_low**	
11h	01h	[7:0]	**vswd**	VSYNC width vswd[7:0] = 1d (default)
12h	00h	[5]	**vspolar**	VSYNC polarity 0: active high (default), 1: active low
		[4]	**vsdisp**	VSYNC display mode 0: sync mode (default), 1: data valid mode
		[1:0]	**vsstrt_high**	VSYNC start position vsstrt[9:0] = 0d (default)
13h	00h	[7:0]	**vsstrt_low**	
14h	00h	[4:0]	**vblank_high**	Vertical blank depth vblank[12:0] = 45d (default)
15h	2Dh	[7:0]	**vblank_low**	
16h	20h	[7:0]	**hswd**	HSYNC width hswd[7:0] = 32d (default)
17h	00h	[5]	**hspolar**	HSYNC polarity 0: active high (default), 1: active low
		[4]	**hsdisp**	HSYNC display mode 0: sync mode (default), 1: data valid mode
		[1:0]	**hsstart_high**	HSYNC start position hsstrt[9:0] = 0d (default)
18h	00h	[7:0]	**hsstart_low**	
19h	00h	[5:0]	**hblank_high**	Horizontal blank depth hblank[13:0] = 140d (default)
1Ah	8Ch	[7:0]	**hblank_low**	

Address (Hex)	Reset Value	Bits	Mnemonic	Description
1Bh	77h	[3:0]	**sgg1**	1st quadrisectional global gain sgg1[3:0] = 7d (default)
		[7:4]	**sgg2**	2nd quadrisectional global gain sgg2[3:0] = 7d (default)
1Ch	77h	[3:0]	**sgg3**	3rd quadrisectional global gain sgg3[3:0] = 7d (default)
		[7:4]	**sgg4**	4th quadrisectional global gain sgg4[3:0] = 7d (default)
1Dh	00h	[6:0]	**pgcr**	Red channel gain pgcr[6:0] = 0d (default)
1Eh	00h	[6:0]	**pgcg1**	Green(Red row) channel gain or all channel gain (**ccsm**=0) pgcg1[6:0] = 0d (default)
1Fh	00h	[6:0]	**pgcg2**	Green(Blue row) channel gain pgcg2[6:0] = 0d (default)
20h	00h	[6:0]	**pgcb**	Blue channel gain pgcb[6:0] = 0d (default)
21h	80h	[7:0]	**offsr**	Red channel analog offset offsr[7:0] = 128 (default)
22h	80h	[7:0]	**offsg1**	Green(Red row) channel analog offset or all channel offset (**ccsm**=0) offsg1[7:0] = 128 (default)
23h	80h	[7:0]	**offsg2**	Green(Blue row) channel analog offset offsg2[7:0] = 128 (default)
24h	80h	[7:0]	**offsb**	Blue channel analog offset offsb[7:0] = 128 (default)
25h	14h	[6:0]	**pthresh**	Bad pixel threshold pthresh[6:0] = 20d (default)
26h	00h	[7:0]	**adcoffs**	ADC offset adcoffs[7:0] = 0d (default)
27h	01h	[5]	**-**	(Factory use only)
		[4]	**-**	(Factory use only)
		[3:0]	**p12stp**	(Factory use only) P12 start control

Address (Hex)	Reset Value	Bits	Mnemonic	Description
28h	40h	[7:5]	-	(Factory use only) -
		[4:0]	-	(Factory use only) -
29h	00h	[7:0]	-	(Factory use only) -
2Ah	00h	[7:0]	**blank**	Blank register for general purpose
2Bh	02h	[5]	-	(Factory use only)
		[4]	-	(Factory use only)
		[3]	-	(Factory use only)
		[2]	-	(Factory use only)
		[1]	-	(Factory use only)
		[0]	-	(Factory use only)

OPERATION DESCRIPTION

1. Output Data Format

1-1. Main Clock Divider

All the data output and sync signals are synchronized to data clock output (**DCLK**). It is generated by dividing the input main clock (**MCLK**). The dividing ratio is 1, 2, 4, and 8 according to main clock dividing control register (**mcdiv**). For 10-bit ADC and VGA resolution, dividing ratio of more than 2 is required. If ratio of 1 is used, the duty must be within 40% to 60%.

1-2. Synchronous Signal Output

The horizontal sync(**HSYNC**) and vertical sync(**VSYNC**) signals are also available. The sync pulse width, polarity and position are programmable by control registers (ref. timing chart). When display mode is enabled, the sync signal outputs indicate that the output data is valid (**hsdisp**=1) or the output rows are valid (**vsdisp**=1).

1-3. Window of Interest Control

Window of Interest (WOI) is defined as the pixel address range to be read out. The WOI can be assigned anywhere on the pixel array. It is composed of four values: row start pointer(**wrp**), column start pointer(**wcp**), row depth(**wrd**) and column width(**wcw**). Each value can be programmed by control registers. For convenience of color signal processing, **wcp** is truncated to even numbers so that the starting data of each line is the red and green column of Bayer pattern. Figure 4 refers to a pictorial representation of the WOI on the displayed pixel image.

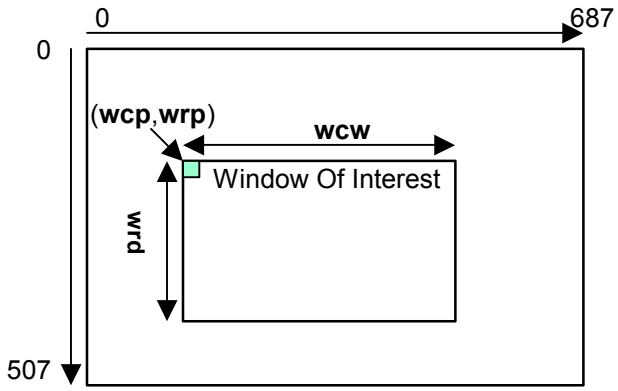


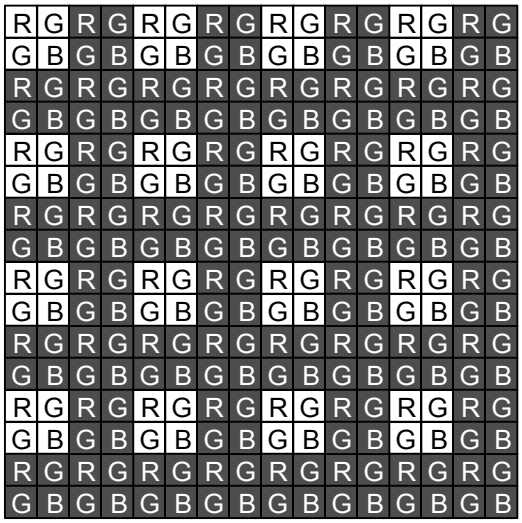
Figure 4. WOI definition.

1-4. Vertical Mirror and Horizontal Mirror Mode Control

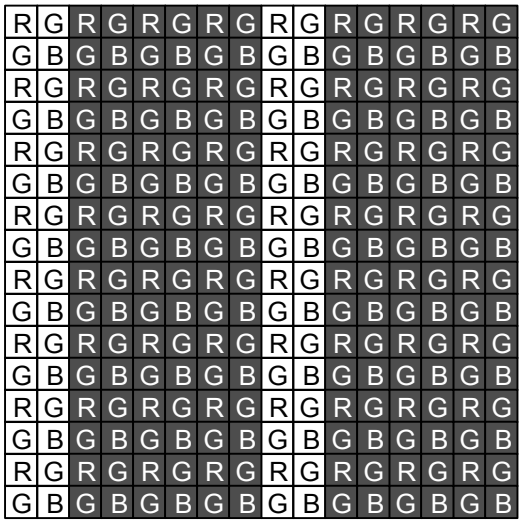
The pixel data are read out from left to right in horizontal direction and from top to bottom in vertical direction normally. By changing the mirror mode, the read-out sequence can be reversed and the resulting image can be flipped like a mirror image. Pixel data are read out from right to left in horizontal mirror mode and from bottom to top in vertical mirror mode. The horizontal and the vertical mirror mode can programmed by Horizontal Mirror Control Register (**mirch**) and Vertical Mirror Control Register (**mircv**).

1-5. Sub-sampling Control

The user can read out the pixel data in sub-sampling rate in both horizontal and vertical direction. Sub-sampling can be done in four rates : full, 1/2, 1/3 and 1/4. The user controls the sub-sampling using the Sub-sampling Control Registers, **subsr** and **subsc**. The sub-sampling is performed only in the Bayer space.



subsr=01b, **subsc**=01b



subsr=00b, **subsc**=11b

Figure 5. Bayer Space Sub-Sampling Examples

1-6. Line Rate and Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changeable by varying the size of virtual frame. The virtual frame’ s width and depth are controlled by effective WOI and blank depths. The effective WOI is scaled by the sub-sampling factors from WOI set by register values. For CDS and ADC function, the virtual column width must be larger than (**adcres**+1)*256/(2^**mcdiv**)+200, where **adcres** is the ADC resolution control register value. The horizontal and vertical blanking time (**hblank**, **vblank**) should be over 60 and 4, respectively. The resulting frame time and line time which are inverse of frame rate and line rate are represented by following equations:

1 frame time = { **wrd** / (**subsr**+1) + **vblank** } * (1 line time)
1 line time = { **wcw** / (**subsc**+1) + **hblank** } * (**DCLK** period)

1-7. Continuous Frame Capture Mode(CFCM) Integration Time Control (Electronic Shutter Control)

In CFCM operation, the integration time is controlled by shutter operation. The shutter operation is done when shutter control register (**shutc**) is set to “1”. In shutter operation, the integration time is determined by the Row Step Integration Time Control Register(**cintr**) and Column Step Integration Time Control Register(**cintc**). The resulting integration time is expressed as;

Integration Time = { TBD }
where **cintr** = 0 to {TBD}, **cintc** = 0 to {TBD}.

1-8. Single Frame Capture Mode(SFCM) Integration Time Control

To capture a still image, SFCM can be set by Single Frame Capture Enable Register(**sfcen**). There are two types of integration mode are implemented. In the rolling shutter mode (**sfcim**=0), the integration time is controlled by SFCM Integration Time Register (**sint**). The light integration period for each rows progresses with reading rows. The integration time is expressed as :

Integration Time = **sint** * (1 line time)

2. Analog to Digital Converter (ADC)

The image sensor has on-chip ADC. Two-channel column parallel ADC scheme is used for separated color channel gain and offset control.

2-1. ADC resolution

The default value of ADC resolution is 10bit and can be changed to 8bit or 9bit by control the ADC Resolution Control Register (**adcres**). Lowering ADC resolution reduces the required minimum line time. When the number of effective output bits is reduced, upper n-bits of output ports are valid and lower bits always has value of "0".

2-2. Correlated Double Sampling (CDS)

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise by the in-pixel amplifier offset deviation. To eliminate those noise components, a correlated double sampling(CDS) circuit is used before converting to digital. The output signal sampled twice, once for the reset level and once for the actual signal level sampling.

2-3. Programmable Gain and Offset Control

R	G1	R	G1
G2	B	G2	B
R	G1	R	G1
G2	B	G2	B

The user can controls the gain of individual color channel by the Programmable Gain Control Registers (**pgcr**, **pgcg1**, **pgcg2**, **pgcb**) and offset by Offset Control Registers (**offsr**, **offsg1**, **offsg2**, **offsb**). If the Color Channel Separation Mode is disabled (**ccsm**=0), **pgcg1** and **offsg1** change the gains and offsets for all channels. As increasing the gain control register, the ADC conversion input range decreases and the gain increased as following equation:

Channel Gain = 128 / (128 – Programmable Gain Control Register Value[6:0])

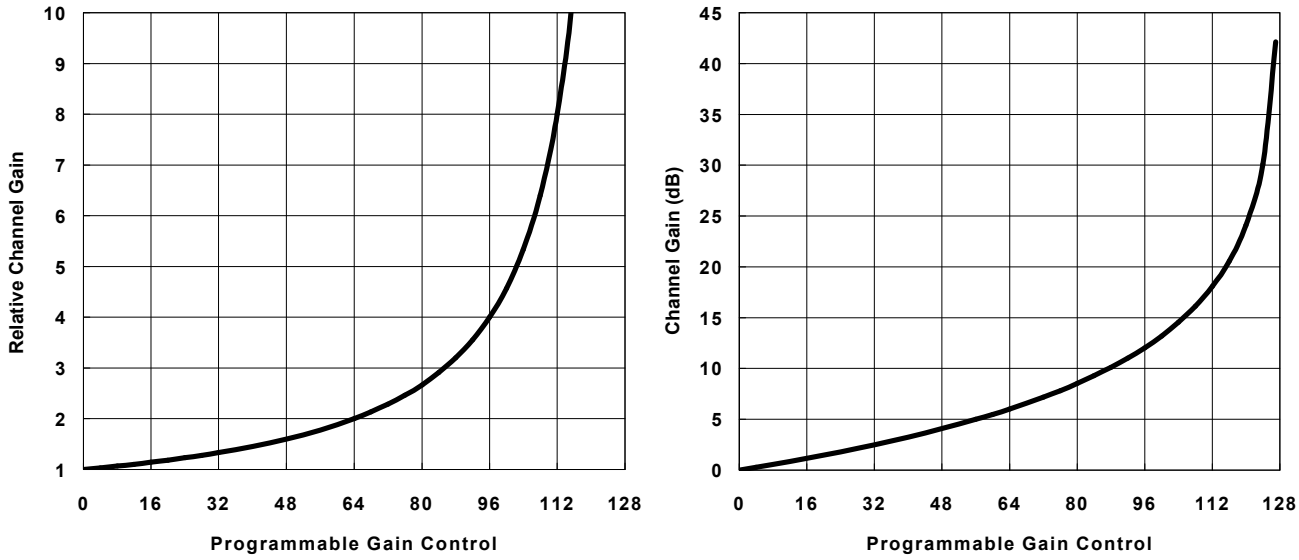


Figure 6. Relative Channel Gain

2-4. Quadrisectional Global Gain Control

The user can controls the global gain to change the gain for all color channels by the Global Gain Control Registers (**sgg1**, **sgg2**, **sgg3**, **sgg4**). The global gain control register is composed of four register groups and each register value decides the gain for each quarter section of output code level.

Global Gain = (**sgg**[3:0]+1) / 8

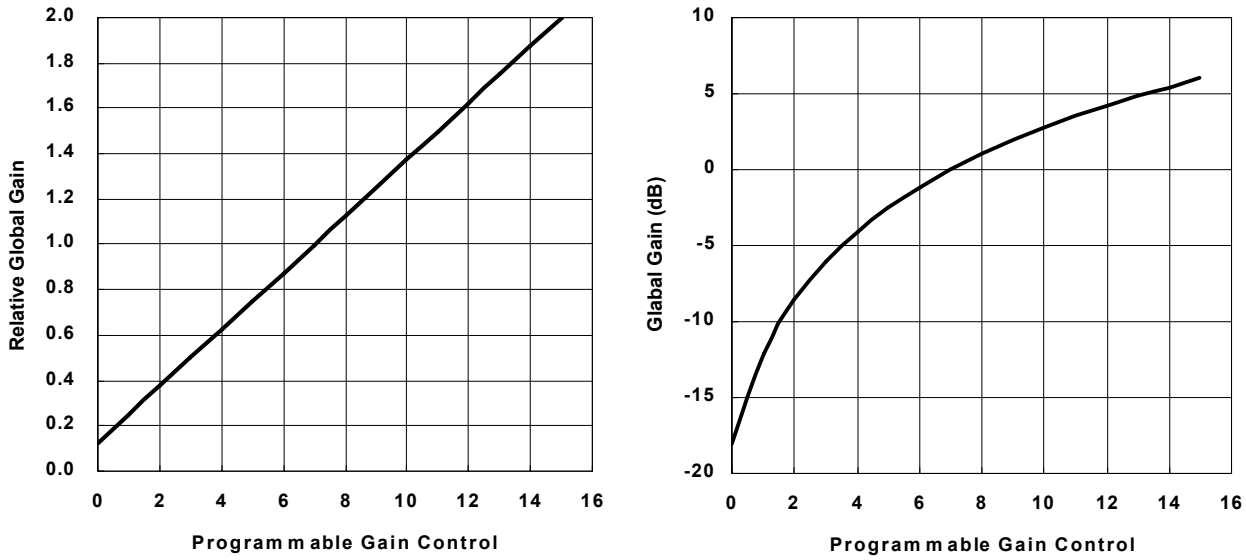


Figure 7. Relative Global Gain

The ADC gain is dependent on **MCLK** frequency (not on **DCLK** frequency) and ADC resolution. The default global gain is set for typical **MCLK** frequency (24MHz) and 10-bit ADC. When the frequency and ADC resolution is changed, the average global gain, (**sgg1**+**sgg2**+**sgg3**+**sgg4**+4)/32 should be changed to maintain the resulting gain over unity for assuring appropriate ADC conversion range.

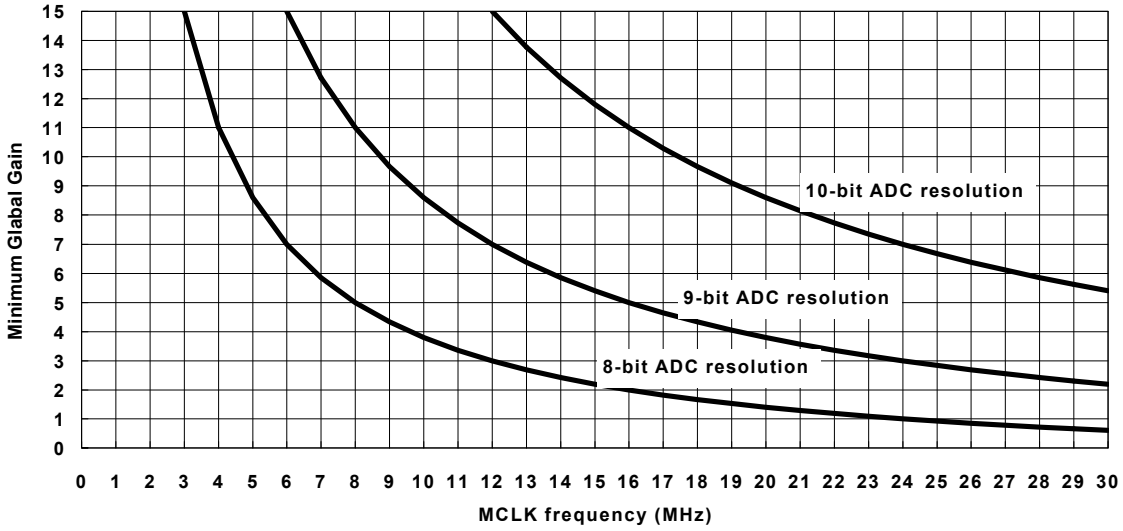


Figure 8. Recommended Minimum Global Gain Control Value

By appropriately programming these four register values, the different output resolution according to the signal can be achieved and the intra-scene dynamic range can be increased by 16 times. In another application, the sectional global gain control can be used as a rough gamma correction with four sectional linear approximation curve as shown in Figure 9.

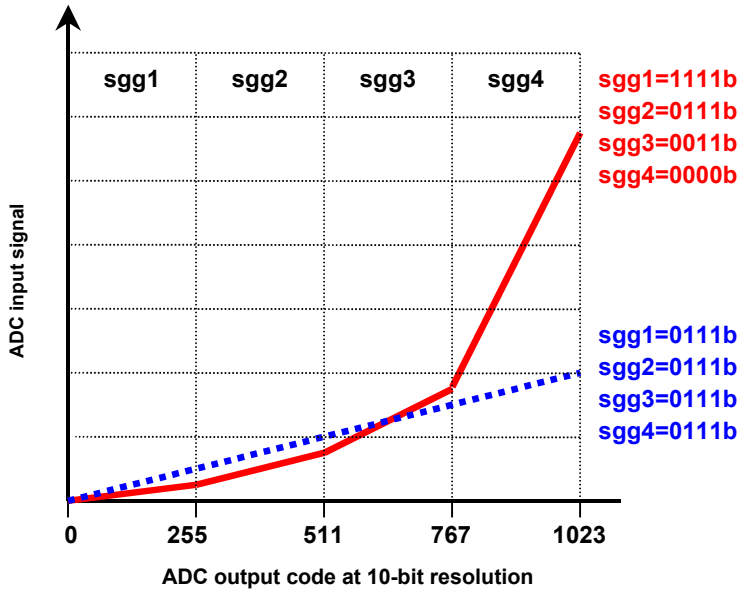


Figure 9. Quadrisectional Glabal Gain Control

3. Post Processing

3-1. Dark Level Compensation

The dark level of Image sensor is defined as average output level without illumination. It includes pixel output caused by leakage current of the photodiodes and ADC offset. To compensate the dark level, the output level of optical black(OB) pixels can be a good reference value. When Auto Dark Level Compensation Register (**dlcm**) is set, the image sensor detects the OB pixel level at the start of every frame and analog-to-digital conversion range is shifted to compensate the dark level for that frame. So, the resulting output data of that frame will be almost zero under dark state. If user wants the dark level which is not zero, the ADC Offset Register (**adcoffs**) can be used. The lower 7-bit value represent the offset value in output code for compensation and the MSB is the sign to define whether the offset is positive (**adcoffs**[7]=0) or negative (**adcoffs**[7]=1). When not in auto dark level compensation mode, the **adcoffs**[7:0] act as a output code value to subtract the output image data. Please notify that the all the 8-bit data are used for an offset value without sign bit.

3-2. Bad Pixel Replacement

When the Bad Pixel Replacement Register (**bprm**) is enabled, the image sensor check that the image data is less or greater than horizontally neighboring pixels in same color channel by the preset threshold value (**pthresh**). If satisfied, the output of the pixel is replaced by the averaged value of the neighboring two pixels. The detectable defected pixels are rare and the bad pixel replacement action can remove defected image effectively. But it reduces the line resolution in horizontal direction.

4. I²C Serial Interface

The I²C is an industry standard serial interface. The I²C contains a serial two-wire half duplex interface that features bi-directional operation, master or slave mode. The general **SDA** and **SCL** are the bi-directional data and clock pins, respectively. These pins are open-drain type ports and will require a pull-up resistor to VDD. The image sensor operates in salve mode only and the **SCL** is input only. The I²C bus interface is composed of following parts : START signal, 7-bit slave device address (0010001b) transmission followed by a read/write bit, an acknowledgement signal from the slave, 8-bit data transfer followed by an acknowledgement signal and STOP signal. The **SDA** bus line may only be changed while **SCL** is low. The data on the **SDA** bus line is valid on the high-to-low transition of **SCL**.

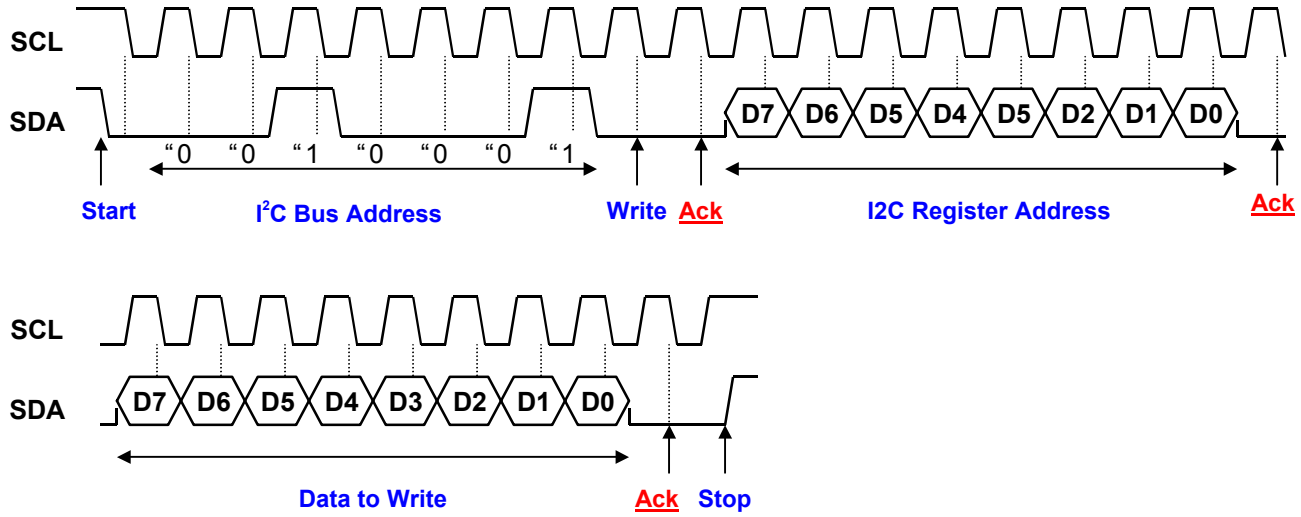


Figure 10. I²C Bus Write Cycle

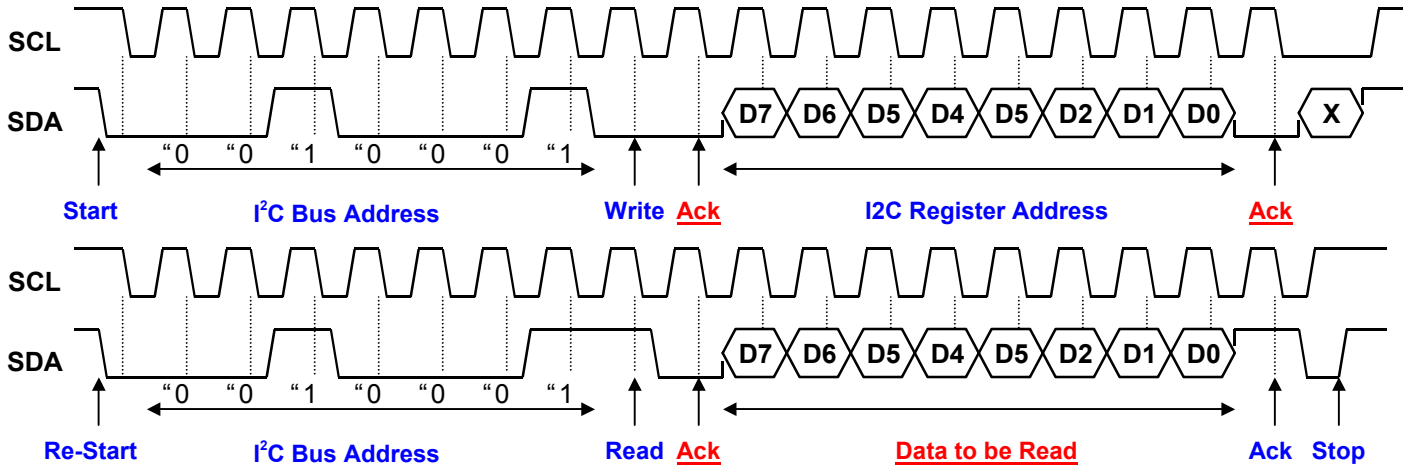


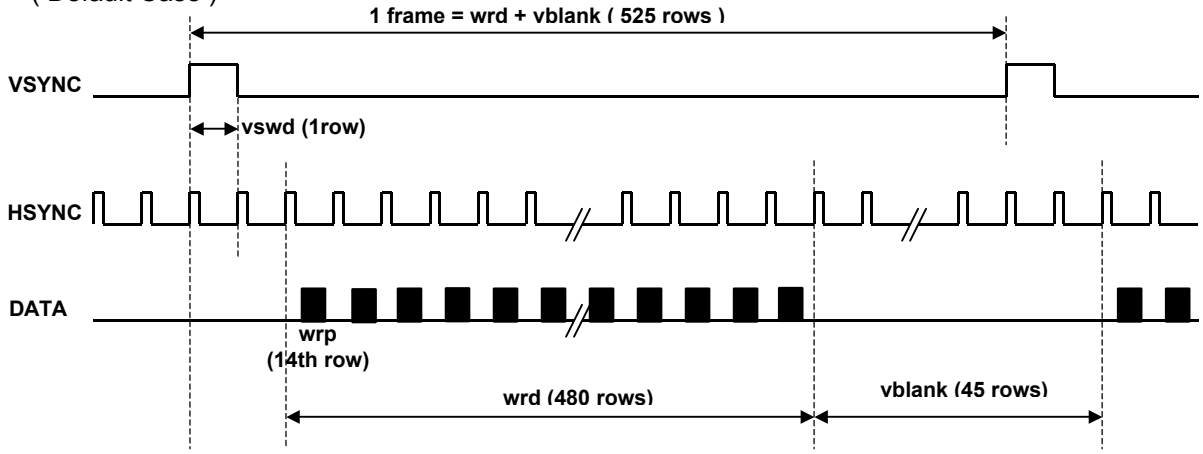
Figure 11. I²C Bus Read Cycle

TIMING CHART

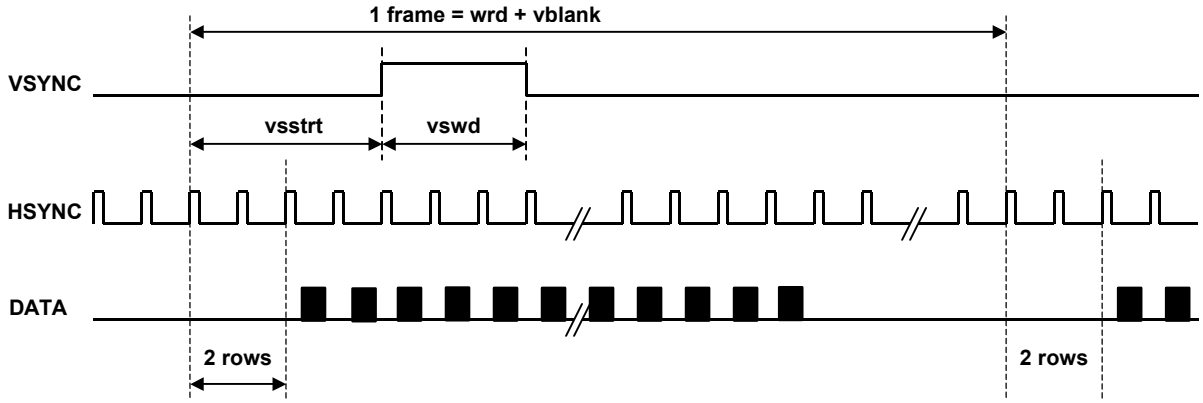
VERTICAL TIMING DIAGRAM

Continuous Frame Capture Mode

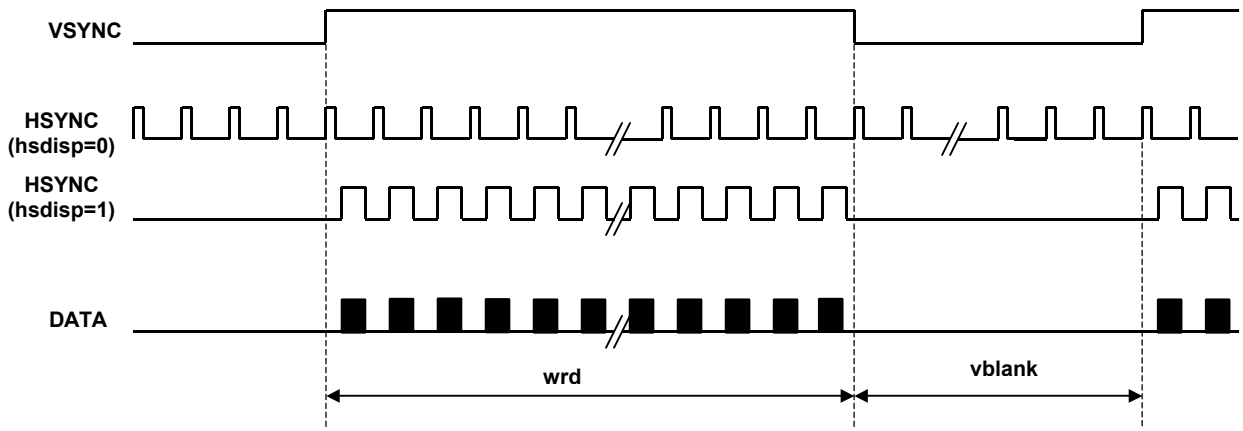
(Default Case)



(Delayed Vertical Sync Case)

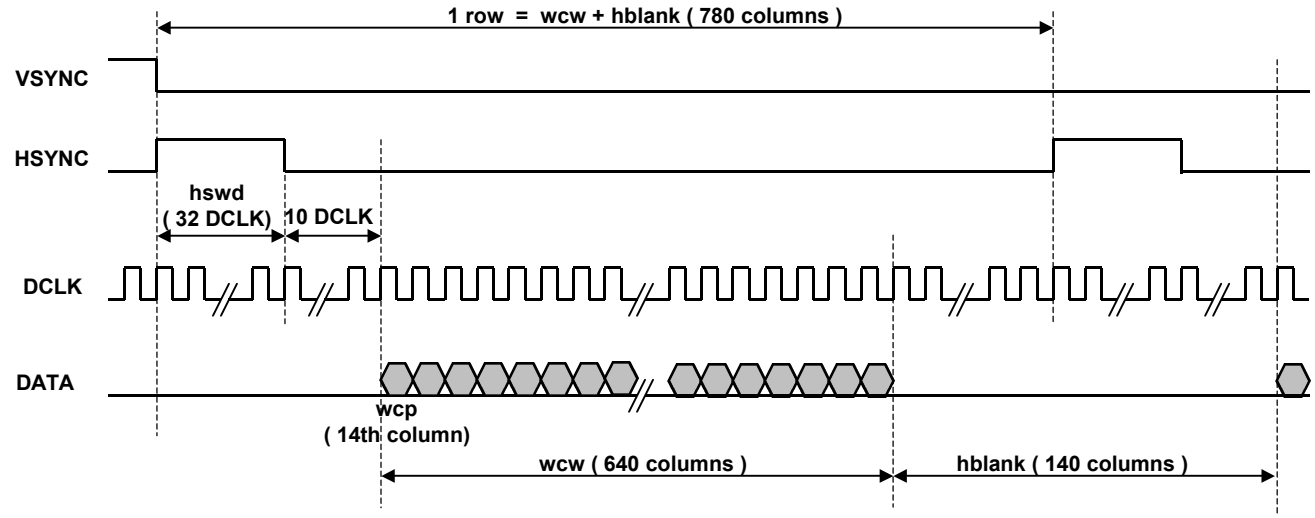


(Vertical Data Valid Mode Case) vsdisp=1

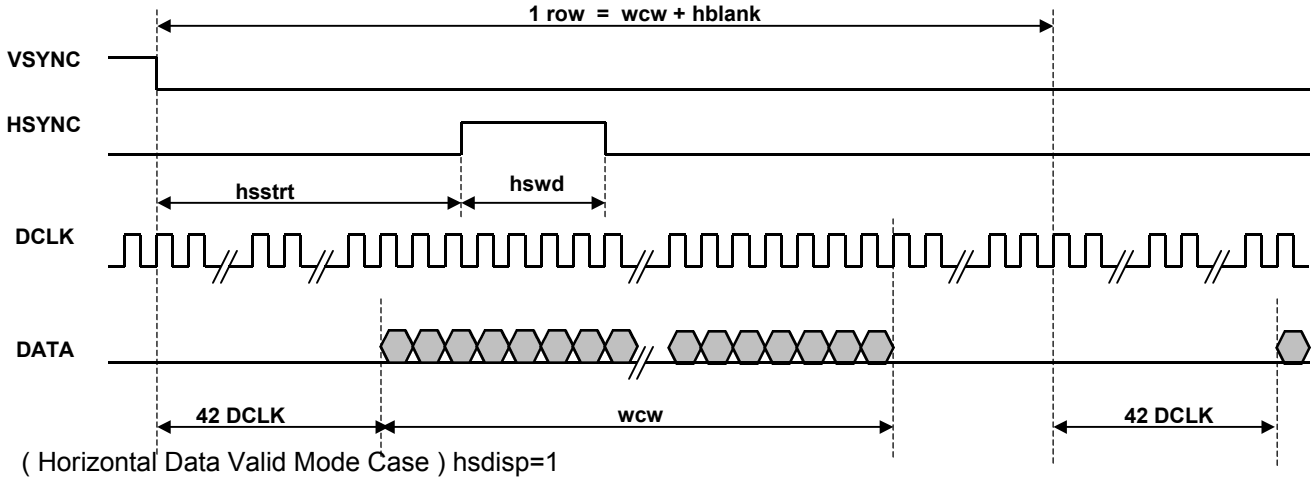


HORIZONTAL TIMING DIAGRAM

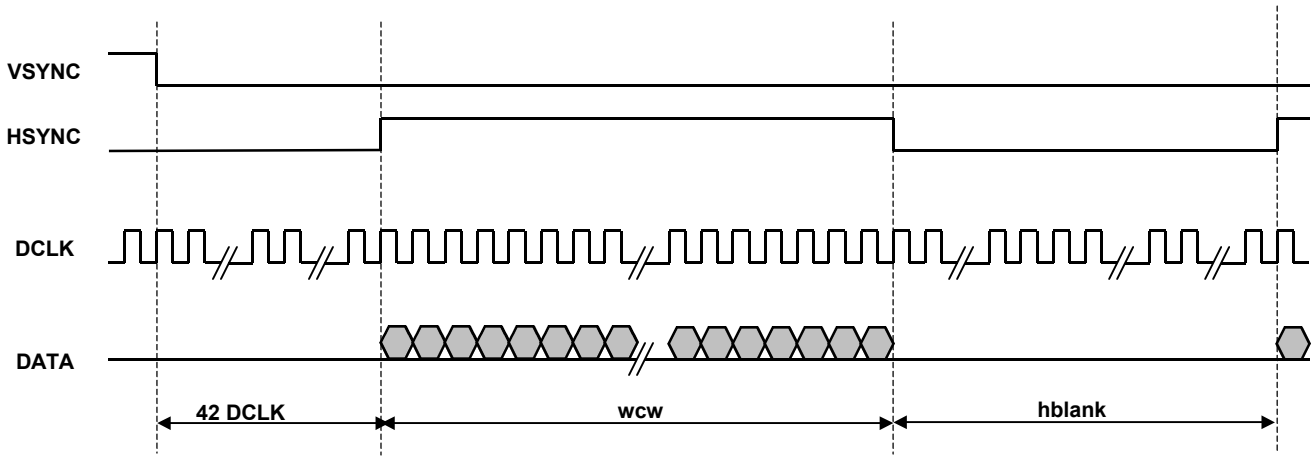
(Default Case)



(Delayed Horizontal Sync Case)



(Horizontal Data Valid Mode Case) hsdisp=1



PACKAGE DIMENSION

48pin CLCC