Advance Information

MPC7410RXPDPNS/D
Rev. 1, 10/2002

MPC7410 Part Number Specification for the MPC7410RXnnnPD Series

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Motorola Part Numbers Affected:

XPC7410RX450PD
XPC7410RX500PD
XPC7410RX533PD

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7410 Hardware Specifications* (order #: MPC7410EC/D).

Specifications provided in this document supersede those in the *MPC7410 Hardware Specifications*, for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to http://www.motorola.com/semiconductors or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification. Part numbers addressed in this document are listed in Table A. For more detailed ordering information, see Table 17.

Table A. Part Numbers Addressed by this Data Sheet

Motorola Part Number	Operating Conditions			Significant Differences from Hardware Specification
	CPU Frequency	Vdd	T_J (°C)	
XPC7410RX450PD	450 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 450Mhz frequency
XPC7410RX500PD	500 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 500Mhz frequency
XPC7410RX533PD	533 MHz	2.0V±50mV	0 to 65	Modified Voltage & Temperature Specification to achieve 533Mhz frequency

Note:
The X prefix in a Motorola PowerPC part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.2 Features

This section summarizes changes to the features of the MPC7410 described in the *MPC7410 Hardware Specifications*, which are none.

1.4.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7410 part numbers described herein.

Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit
Core supply voltage		Vdd	2.0V ± 50mV	V
PLL supply voltage		AVdd	2.0V ±5 0mV	V
L2 DLL supply voltage		L2AVdd	2.0V ± 50mV	V
Processor bus supply voltage	BVSEL = 1 or BVSEL = $\overline{\text{HRESET}}$	OVdd	2.5V ± 125mV	V
	BVSEL = GND	OVdd	1.8V ± 90mV	V
L2 bus supply voltage	L2VSEL = 1 or L2VSEL = $\overline{\text{HRESET}}$	L2OVdd	2.5V ± 125mV	V
	L2VSEL = GND	L2OVdd	1.8V ± 90mV	V

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit
Input voltage	Processor bus	V_{in}	GND to OVdd	V
	L2 Bus	V_{in}	GND to L2OVdd	V
	JTAG Signals	V_{in}	GND to OVdd	V
Die-junction temperature		T_j	0-65	°C

Note:
These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 6 provides the power consumption for the MPC7410 part at the frequencies described herein.

Table 6. Power Consumption for MPC7410

	Processor (CPU) Frequency	Processor (CPU) Frequency	Processor (CPU) Frequency	Unit	Notes
	450Mhz	500Mhz	533Mhz		
Full-On Mode					
Typical	5.9	6.5	6.9	W	1, 3
Maximum	13.2	14.7	15.6	W	1, 2
Doze Mode					
Maximum	4.5	5	5.3	W	1, 2
Nap Mode					
Maximum	2.13	2.25	2.33	W	1, 2
Sleep Mode					
Maximum	2.13	2.25	2.33	W	1, 2
Sleep Mode—PLL and DLL Disabled					
Typical	0.5	0.5	0.5	W	1, 3
Maximum	2.0	2.0	2.0	W	1, 2

Notes:
1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.
2. Maximum power is measured at 65 °C and Vdd = 2.0V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65 °C and Vdd = 2.0V in a system while running typical benchmarks.

1.4.2.1 Clock AC Specifications

Table 7 provides the additional clock AC timing specifications described in this document. Refer to the *MPC7410 Hardware Specification* for the remaining frequencies.

Table 7. Clock AC Timing Specifications

At recommended operating conditions (See Table 3.)

Characteristic	Symbol	450 MHz		500 MHz		533 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	300	450	300	500	300	533	MHz	
VCO frequency	f_{VCO}	600	900	600	1000	600	1066	MHz	
SYSCLK frequency	f_{SYSCLK}	33	133	33	133	33	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	30	7.5	30	7.5	30	ns	
SYSCLK rise and fall time	t_{KR}	—	1.0	—	1.0	—	1.0	ns	2
	t_{KF}	—	0.5	—	0.5	—	0.5	ns	3
SYSCLK duty cycle measured at OVdd/2	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	4
SYSCLK jitter		—	±150	—	±150	—	±150	ps	5
Internal PLL relock time		—	100	—	100	—	100	µs	6

Note:
See general hardware specification.

1.4.2.2 Processor Bus AC Specifications

Table 8 provides the processor bus AC timing specifications for the MPC7410 part described in this document.

Table 8. Processor Bus AC Timing Specifications

At Vdd=AVdd=2.0V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 2.5V±0.125V and OVdd = 1.8V±0.090V, 60X bus at 133MHz

Parameter	Symbol	450, 500, 533 Mhz		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	2,3,4,5
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	2,3,5
Setup Times:				ns	10
Address/Transfer Attribute	t_{AVKH}	1.4	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSVKH}	1.4	—		—
Data/Data Parity	t_{DVKH}	1.4	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARVKH}	1.4	—		—
All Other Inputs	t_{IVKH}	1.4	—		8
Input Hold Times:				ns	11
Address/Transfer Attribute	t_{AXKH}	0	—		6
Transfer Start ($\overline{\text{TS}}$)	t_{TSXKH}	0	—		—
Data/Data Parity	t_{DXKH}	0	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{ARXKH}	0	—		—
All Other Inputs	t_{IXKH}	0	—		8
Valid Times:				ns	12
Address/Transfer Attribute	t_{KHAV}	—	3.0		6
$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$	t_{KHTSV}	—	3.0		—
Data	t_{KHDV}	—	3.5		7
Data Parity	t_{KHDPV}	—	3.5		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{KHARV}	—	2.3		—
All Other Outputs	t_{KHOV}	—	3.0		9
Output Hold Times:				ns	13
Address/Transfer Attribute	t_{KHAX}	0.75	—		6
$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$	t_{KHTSX}	0.75	—		—
Data/Data Parity	t_{KHDX}	0.6	—		7
$\overline{\text{ARTRY}}$/$\overline{\text{SHD0}}$/$\overline{\text{SHD1}}$	t_{KHARX}	0.75	—		—
All Other Outputs	t_{KHOX}	0.75	—		9
SYSCLK to Output Enable	t_{KHOE}	0.5	—	ns	14
SYSCLK to Output High Impedance (all except $\overline{\text{TS}}$, $\overline{\text{ABB}}$/AMON(0), $\overline{\text{ARTRY}}$/$\overline{\text{SHD}}$, $\overline{\text{DBB}}$/DMON(0))	t_{KHOZ}	—	3.5	ns	15

Table 8. Processor Bus AC Timing Specifications (continued)

At Vdd=AVdd=2.0V±50mV; 0 ≤ Tj ≤ 65°C, OVdd = 2.5V±0.125V and OVdd = 1.8V±0.090V, 60X bus at 133MHz

Parameter	Symbol	450, 500, 533 Mhz		Unit	Notes
		Min	Max		
SYSCLK to $\overline{TS}$, $\overline{ABB/AMON(0)}$, $\overline{DBB/DMON(0)}$ High Impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	4,15, 16,17
Maximum Delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ Precharge	t_{KHARP}	—	1	t_{sysclk}	4,17
SYSCLK to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ High Impedance After Precharge	t_{KHARPZ}	—	2	t_{sysclk}	4,17

Note:
See general hardware specification.

1.4.2.3 L2 Clock AC Specifications

Table 9 provides the L2CLK Output AC Timing Specifications for the MPC7410 part described in this document.

Table 9. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3.)

Parameter	Symbol	450 MHz		500 MHz		533 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2CLK frequency	f_{L2CLK}	150	225	150	250	150	266	MHz	1
L2CLK cycle time	t_{L2CLK}	4.4	6.67	4.0	6.67	3.76	6.67	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	50		50		50		%	2
Internal DLL-relock time		640	—	640	—	640	—	L2CLK	4
DLL capture window			±200		±200		±200	ns	5

Note:
See general hardware specification.

1.4.2.4 L2 Bus AC Specifications

Table 10 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this document.

Table 10. L2 Bus Interface AC Timing Specifications

At Vdd=AVdd=L2AVdd= 2.05V±50mV; 0 ≤ Tj ≤ 65°C, L2OVdd = 2.5V±0.125V and L2OVdd =1.8V±0.090V

Parameter	Symbol	450 MHz		500 MHz		533 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR} & t_{L2CF}	—	1.0	—	1.0	—	1.0	ns	1
Setup Times: Data and parity	t_{DVL2CH}	1.375	—	1.250	—	1.168	—	ns	2
Input Hold Times: Data and parity	t_{DXL2CH}	—	0.0	—	0.0	—	0.0	ns	2
Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOV}	 - - - -	 2.375 TBD TBD TBD	 - - - -	 2.25 TBD TBD TBD	 - - - -	 2.17 TBD TBD TBD	ns	3,4
Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOX}	 0.55 TBD TBD TBD	 - - - -	 0.5 TBD TBD TBD	 - - - -	 0.47 TBD TBD TBD	 - - - -	ns	3
L2SYNC_IN to high impedance: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11	t_{L2CHOZ}	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	 - - - -	 2.0 2.5 3.0 3.5	ns	

Note:
See general hardware specification.

1.9 Document Revision History

Table 16 provides a revision history for this Part Number Specification.

Table 16. Document Revision History

Document Revision	Substantive Changes
Rev 0	Initial Release
Rev 1	Minor formatting
	Section 1.10.1 - added Table 17 - Part-Marking Nomenclature

1.10 Ordering Information

1.10.1 Part Numbers Addressed by this Specification

Table 17 provides the ordering information for the MPC7410 part described in this document.

Table 17. Part-Marking Nomenclature

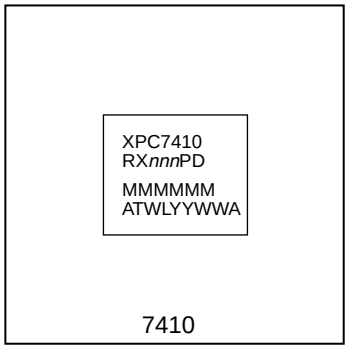
MPC 7410 RX *xxx* *x* *x*

Product Code	Part Identifier	Package	Processor Frequency[1]	Application Modifier	Revision Level
XPC [2]	7410	RX = CBGA	450 500 533	P: 2.0 V ± 50 mV 0 to 65 °C	D: 1.3; PVR = 800C 1103

Notes:
1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.
2. The X prefix in a Motorola PowerPC part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.10.3 Part Marking

Parts are marked as the example shown in Figure 26.



Notes:

nnn is the speed grade of the part
MMMMMM is the 6-digit mask number
ATWLYYWWA is the traceability code
CCCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

Figure 26. Motorola Part Marking for BGA Device

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