# Programmable logic sequencer ($16 \times 48 \times 8$)

# PLUS105–45



## DESCRIPTION

The PLUS105–45 is a bipolar programmable state machine of the Mealy type. Both the AND and the OR array are user-programmable. All 48 AND gates are connected to the 16 external dedicated inputs ($I_0$-$I_{15}$) and to the feedback paths of the 6 buried State Registers ($Q_{P0}$-$Q_{P5}$). Because the OR array is programmable, any one or all of the 48 transition terms can be connected to any or all of the State and Output Registers.

All state transition terms can include True, False and Don't Care states of the controlling state variables. A Complement Transition Array supports complex IF-THEN-ELSE state transitions with a single product term.

All buried State and Output registers are edge-triggered clocked S-R flip-flops. Asynchronous Preset/Output Enable functions are available.

The PLUS105–45 is pin-for-pin and software compatible with the Signetics PLS105 and PLS105A Logic Sequencers, as well as other commercially available 105-type programmable logic devices.

To facilitate testing of state machine designs, diagnostic mode features for register preset and buried state register observability have been incorporated into the PLUS105–45 device architecture.

Ordering codes are listed in the Ordering Information Table.

## FEATURES

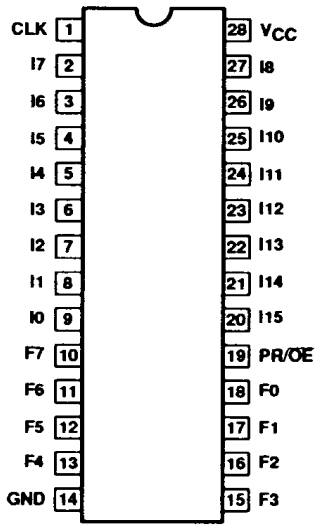
- 45MHz operating frequency
  - 55.6MHz clock rate
  - No OR term loading restrictions
- Available in 300mil skinny DIP, 600mil-wide Plastic DIP and PLCC packages
- Pin and software compatible with other commercially available 105 logic sequencers
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition complement array
- Positive edge-triggered clocked S-R flip-flops
- Security fuse
- Programmable Asynchronous Preset or Output Enable
- Power-on preset (to all "1"s) of internal registers
- Power dissipation: 800mW (typ.)
- TTL compatible
- Single +5V supply
- 3-State outputs

## APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security Locking systems
- Counters
- Shift registers

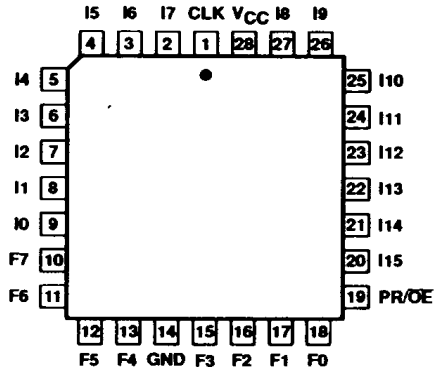
## PIN CONFIGURATIONS

### N Packages




N = Plastic DIP (600mil-wide)
N3 = Plastic DIP (300mil-wide)

### A Package




A = Plastic Leaded Chip Carrier

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE |
|---|---|
| 28-pin Plastic Dual-In-Line, 600mil-wide | PLUS105–45N |
| 28-pin Plastic Dual-In-Line, 300mil-wide | PLUS105–45N3 |
| 28-pin Plastic Leaded Chip Carrier, 450mil-square | PLUS105–45A |

# Programmable logic sequencer (16 × 48 × 8)

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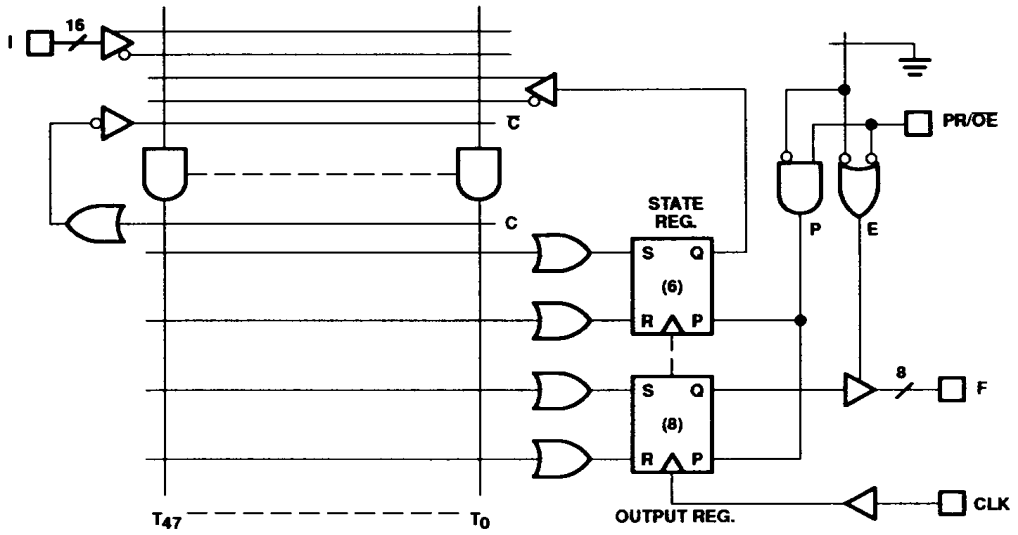
## FUNCTIONAL DIAGRAM




## PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION | POLARITY |
|---|---|---|---|
| 1 | CLK | **Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. | Active-High (H) |
| 2-9, 26, 27<br>20-22 | I0 - I9,<br>I13 - I15 | **Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L". | Active-High/Low (H/L) |
| 23 | I12 | **Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL levels. When I12 is held at +10V, device outputs F0 - F5 reflect the contents of State Register bits $P_0$ - $P_5$. The contents of each Output Register remains unaltered. | Active-High/Low (H/L) |
| 24 | I11 | **Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I11 is held at +10V, device outputs F0 - F5 become direct inputs for State Register bits $P_0$ - $P_5$; a Low-to-High transition on the clock line loads the values on pins F0 - F5 into the State Register bits $P_0$ - $P_5$. The contents of each Output Register remains unaltered. | Active-High/Low (H/L) |
| 25 | I10 | **Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When $I_{10}$ is held at +10V, device outputs F0 - F7 become direct inputs for Output Register bits Q0 - Q7; a Low-to-High transition on the clock line loads the values on pins F0 - F7 into the Output Register bits Q0 - Q7. The contents of each State Register remains unaltered. | Active-High/Low (H/L) |
| 10-13<br>15-18 | F0 - F7 | **Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register bits Q0 - Q7, when enabled. When I12 is held at +10V, F0 - F5 = ($P_0$ - $P_5$). When I11 is held at +10V, F0 - F5 become inputs to State Register bits $P_0$ - $P_5$. When I10 is held at +10V, F0 - F7 become inputs to Output Register bits Q0 - Q7. | Active-High (H) |
| 19 | PR/$\overline{OE}$ | **Preset or Output Enable Input:**<br>**A user programmable function:**<br>• **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. PR overrides Clock, and when held High, clocking is inhibited and F0 - F7 are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the Preset signal goes low. See timing definitions.<br>• **Output Enable:** Provides an output enable function to buffers F0 - F7 from the Output Registers. | Active-High (H)<br>Active-Low (L) |

# Programmable logic sequencer (16 × 48 × 8)





## TRUTH TABLE [1, 2, 3, 4, 5, 6, 7]

| $V_{CC}$ | OPTION PR | OPTION $\overline{OE}$ | I10 | I11 | I12 | CK | S | R | $Q_P$ | $Q_F$ | F |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | H | | * | * | * | X | X | X | H | H | $Q_F$ |
| | L | | +10V | X | X | ↑ | X | X | $Q_P$ | L | L |
| | L | | +10V | X | X | ↑ | X | X | $Q_P$ | H | H |
| | L | | X | +10V | X | ↑ | X | X | L | $Q_F$ | L |
| | L | | X | +10V | X | ↑ | X | X | H | $Q_F$ | H |
| | L | | X | X | +10V | X | X | X | $Q_P$ | $Q_F$ | $Q_P$ |
| | L | | X | X | X | X | X | X | $Q_P$ | $Q_F$ | $Q_F$ |
| | | H | X | X | * | X | X | X | $Q_P$ | $Q_F$ | Hi-Z |
| +5V | | X | +10V | X | X | ↑ | X | X | $Q_P$ | L | L |
| | | X | +10V | X | X | ↑ | X | X | $Q_P$ | H | H |
| | | X | X | +10V | X | ↑ | X | X | L | $Q_F$ | L |
| | | X | X | +10V | X | ↑ | X | X | H | $Q_F$ | H |
| | | L | X | X | +10V | X | X | X | $Q_P$ | $Q_F$ | $Q_P$ |
| | | L | X | X | X | X | X | X | $Q_P$ | $Q_F$ | $Q_F$ |
| | | L | X | X | X | ↑ | L | L | $Q_P$ | $Q_F$ | $Q_F$ |
| | | L | X | X | X | ↑ | L | H | L | L | L |
| | | L | X | X | X | ↑ | H | L | H | H | H |
| | | L | X | X | X | ↑ | H | H | IND. | IND. | IND. |
| ↑ | X | X | X | X | X | X | X | X | H | H | |

**NOTES:**

1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 + \ldots T_{47}$
   $T_n = (C_0)\ (I_0, I_1, I_2, \ldots)\ (P_0, P_1, \ldots P_5)$
2. Either Preset (Active-High) or Output Enable (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H or L or +10V
5. X = Don't Care (≤ 5.5V)
6. When using the $F_n$ pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.
7. IND. = Indeterminent; R = S = H is an illegal input condition.

## VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Note that even if the PR function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array preprogrammed with a standard test pattern. NOTE: The Test Array pattern must be deleted before incorporating a user program.

# Programmable logic sequencer (16 × 48 × 8)

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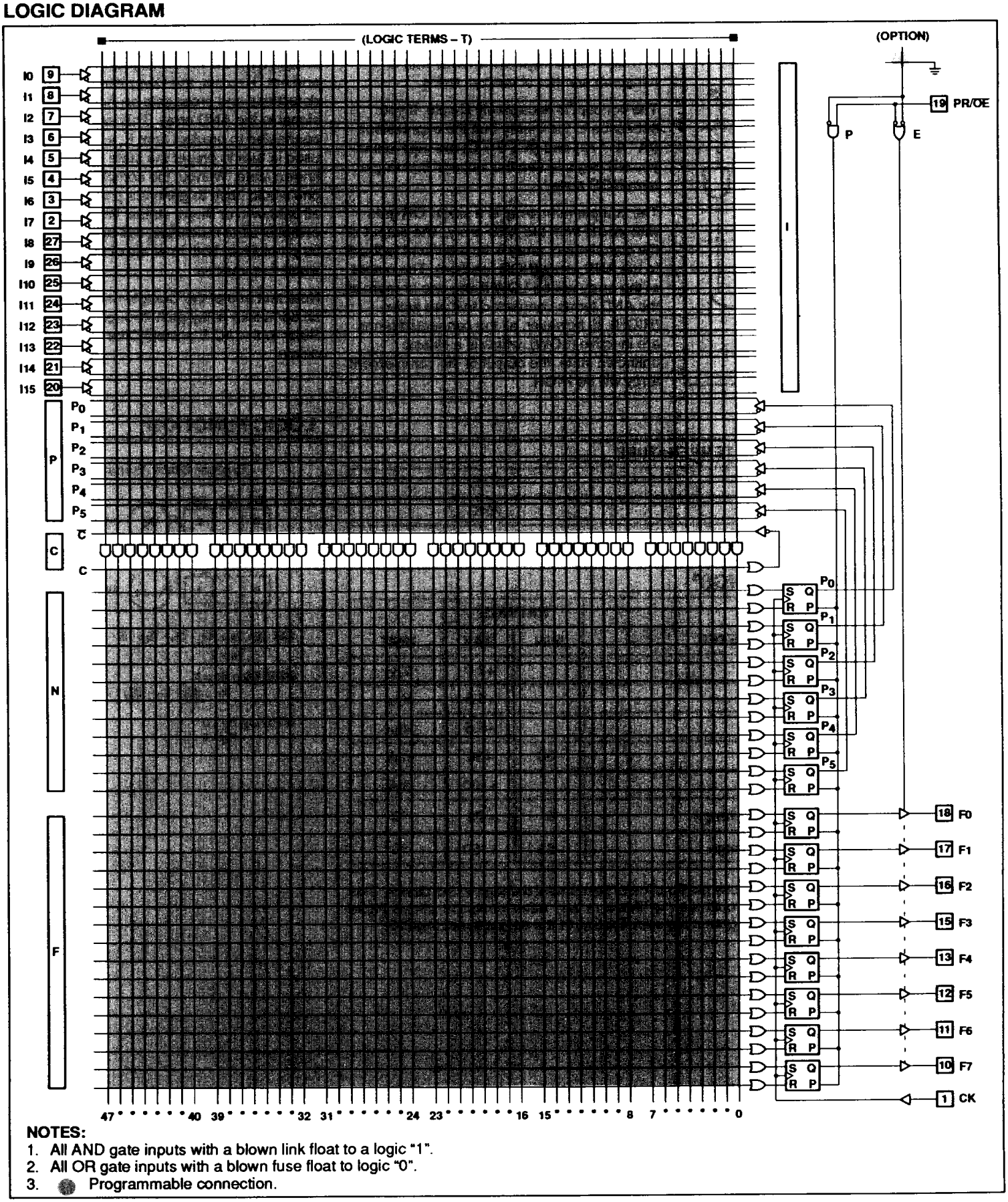
## LOGIC DIAGRAM




**NOTES:**

1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ● Programmable connection.

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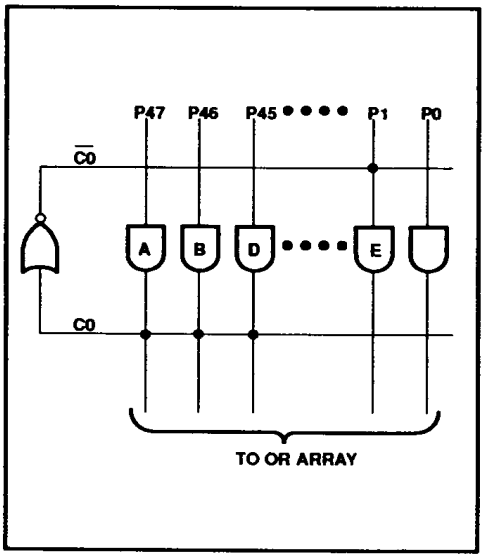
## COMPLEMENT ARRAY DETAIL




The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and $(\overline{A + B + C})$ are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and fedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to a known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that use of the Complement Array adds an additional delay path through the device. Refer to the AC Electrical Characteristics for details.

## THERMAL RATINGS

| TEMPERATURE | |
|---|---|
| Maximum junction | 150°C |
| Maximum ambient | 75°C |
| Allowable thermal rise ambient to junction | 75°C |

## ABSOLUTE MAXIMUM RATINGS[1]

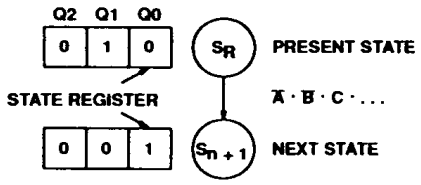
| SYMBOL | PARAMETER | RATINGS MIN | RATINGS MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | +7.0 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | | +5.5 | $V_{DC}$ |
| $V_{OUT}$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IN}$ | Input currents | –30 | +30 | mA |
| $I_{OUT}$ | Output currents | | +100 | mA |
| $T_{amb}$ | Operating temperature range | 0 | +75 | °C |
| $T_{stg}$ | Storage temperature range | –65 | +150 | °C |

**NOTE:**

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

## LOGIC FUNCTION

**Typical State Transition:**




SET $Q_0$: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET $Q_1$: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD $Q_2$: $S_2 = 0$
$R_2 = 0$

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## DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| **Input voltage[2]** | | | | | | |
| $V_{IH}$ | High | $V_{CC}$ = MAX | 2.0 | | | V |
| $V_{IL}$ | Low | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{IC}$ | Clamp[3] | $V_{CC}$ = MIN, $I_{IN}$ = −12mA | | −0.8 | −1.2 | V |
| **Output voltage[2]** | | | | | | |
| | | $V_{CC}$ = MIN | | | | |
| $V_{OH}$ | High | $I_{OH}$ = −2mA | 2.4 | | | V |
| $V_{OL}$ | Low | $I_{OL}$ = 9.6mA | | 0.35 | 0.45 | V |
| **Input current** | | | | | | |
| | | $V_{CC}$ = MAX | | | | |
| $I_{IH}$ | High | $V_{IN}$ = $V_{CC}$ | | <1 | 30 | µA |
| $I_{IL}$ | Low | $V_{IN}$ = 0.45V | | −20 | −250 | µA |
| **Output current** | | | | | | |
| | | $V_{CC}$ = MAX | | | | |
| $I_{O(OFF)}$ | Hi-Z state | $V_{OUT}$ = 2.7V | | 1 | 40 | µA |
| | | $V_{OUT}$ = 0.45V | | −1 | −40 | µA |
| $I_{OS}$ | Short circuit[3, 4] | $V_{OUT}$ = 0V | −15 | | −70 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[5] | $V_{CC}$ = MAX | | | 200 | mA |
| **Capacitance** | | | | | | |
| | | $V_{CC}$ = 5.0V | | | | |
| $C_{IN}$ | Input | $V_{IN}$ = 2.0V | | 8 | | pF |
| $C_{OUT}$ | Output | $V_{OUT}$ = 2.0V | | 10 | | pF |

**NOTES:**

1. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Duration of short circuit should not exceed 1 second.
5. $I_{CC}$ is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

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## AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30PF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

| SYMBOL | PARAMETER | FROM | TO | LIMITS MIN | LIMITS TYP[1] | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Pulse Width** | | | | | | | |
| $t_{CKH}$ | Clock High | CK + | CK – | 9 | 8 | | ns |
| $t_{CKL}$ | Clock Low | CK – | CK + | 9 | 8 | | ns |
| $t_{CKP}$ | Clock Period | CK + | CK + | 18 | 16 | | ns |
| $t_{PRH}$ | Preset pulse | PR + | PR - | 10 | 8 | | ns |
| **Setup Time** | | | | | | | |
| $t_{IS1}$ | Input | Input ± | CK+ | 13 | 12 | | ns |
| $t_{IS2}$ | Input (through Complement Array) | Input ± | CK + | 23 | 20 | | ns |
| $t_{VS}$ | Power-on preset | $V_{CC}$ + | CK – | 0 | –10 | | ns |
| $t_{PRS}$ | Clock resume (after preset) | PR – | CK – | 0 | –5 | | ns |
| $t_{NVCK}$ | Clock lockout (before preset) | CK – | PR – | 10 | 5 | | ns |
| **Hold Time** | | | | | | | |
| $t_{IH}$ | Input | CK + | Input ± | 0 | –5 | | ns |
| **Diagnostic Mode** | | | | | | | |
| $t_{RJS}$ | Initialization of diagnostic mode | $I_{10}$ or $I_{11}$ + (to 8V) | $F_n$ as inputs | 50 | 25 | | ns |
| $t_{RJH}$ | Clock for diagnostic mode | CK + | Register input jam | 50 | 25 | | ns |
| **Propagation Delay[3]** | | | | | | | |
| $t_{CKO}$ | Clock | CK + | Output ± | | 8 | 9 | ns |
| $t_{OE}$ | Output enable[2] | OE – | Output – | | 8 | 9 | ns |
| $t_{OD}$ | Output disable[2] | OE + | Output + | | 8 | 9 | ns |
| $t_{PR}$ | Preset | PR + | Output + | | 12 | 15 | ns |
| $t_{PPR}$ | Power-on preset | $V_{CC}$ + | Output + | | 0 | 10 | ns |
| **Frequency of Operation** | | | | | | | |
| $f_{MAX1}$ | Without Complement Array $\left(\frac{1}{t_{IS1} + t_{CKO}}\right)$ | Input ± | Output ± | 45.0 | 50.0 | | MHz |
| $f_{MAX2}$ | With Complement Array $\left(\frac{1}{t_{IS2} + t_{CKO}}\right)$ | Input thru Complement Array ± | Output ± | 31.3 | 35.7 | | MHz |
| $f_{MAX3}$ | Internal feedback without Complement Array $\left(\frac{1}{t_{CKL} + t_{CKH}}\right)$ | Register Output ± | Register Input ± | 55.6 | 62.5 | | MHz |
| $f_{MAX4}$ | Internal feedback with Complement Array $\left(\frac{1}{t_{IS2}}\right)$ | Register Output thru Complement Array ± | Register Input ± | 43.5 | 50.0 | | MHz |
| $f_{CLK}$ | Clock frequency | CK + | CK + | 55.6 | 62.5 | | MHz |

**NOTES:**

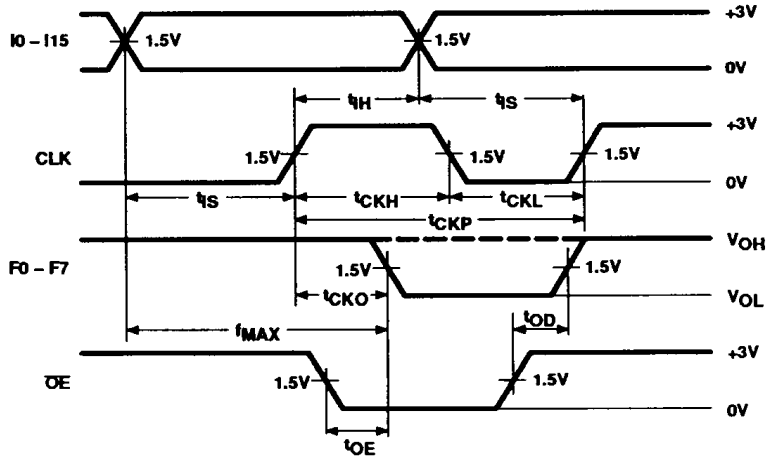
1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and $S_1$ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with $S_1$ open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with $S_1$ closed.
3. All propagation delays and setup times are meausred and specified under worst case conditions.

# Programmable logic sequencer (16 × 48 × 8)

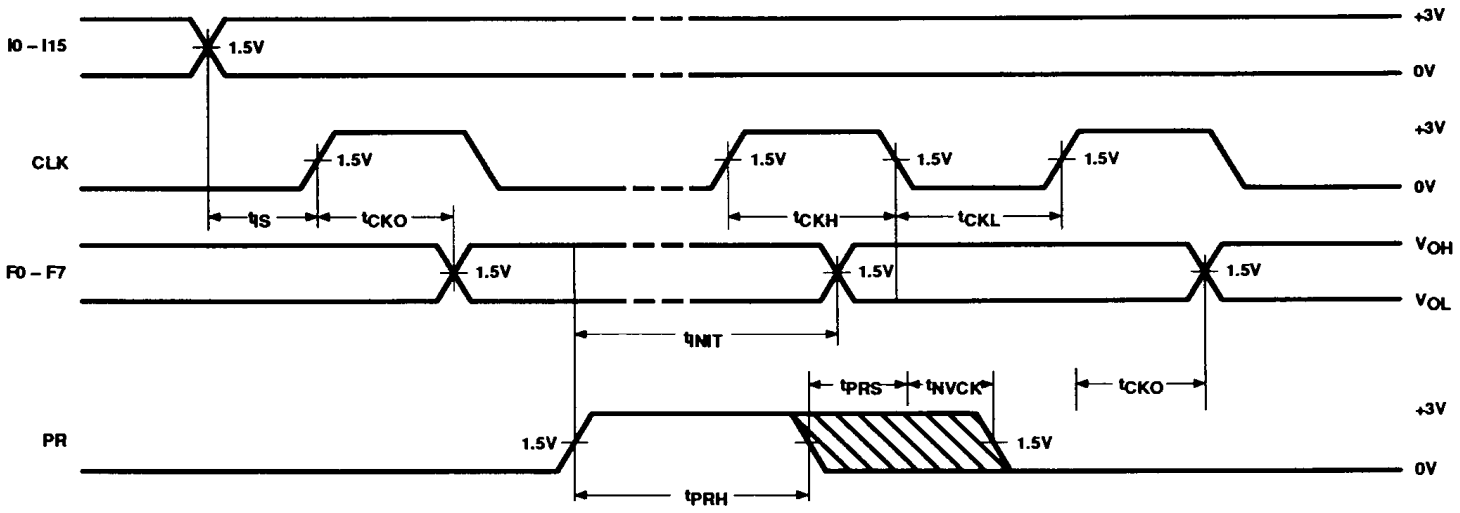




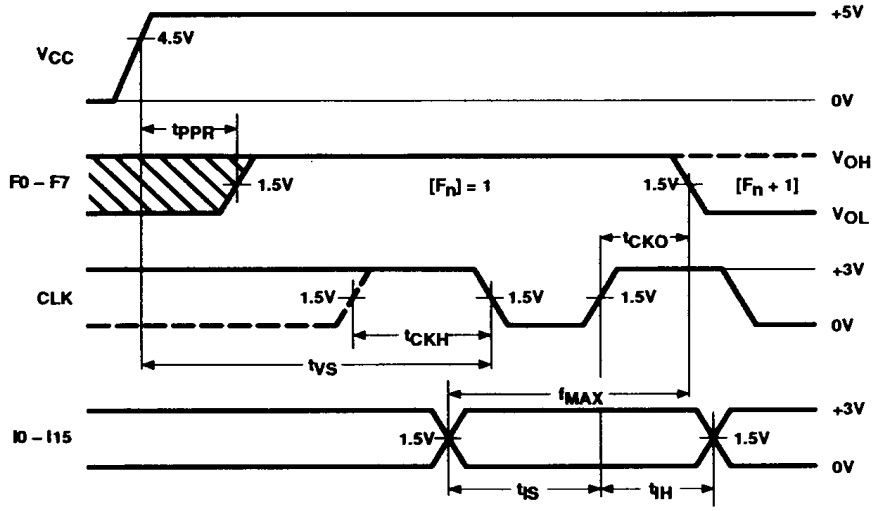
## TIMING DIAGRAMS




**Sequential Mode**

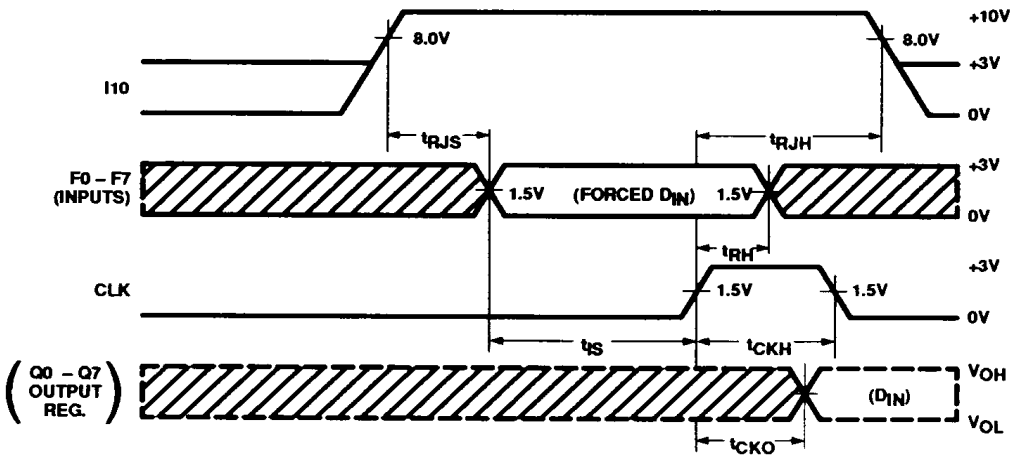



**Asynchronous Preset**

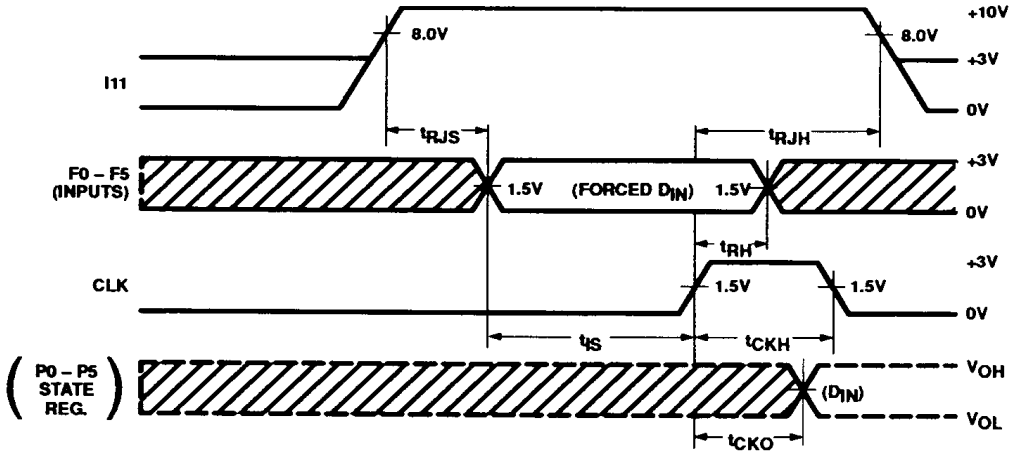



**Power-On Preset**

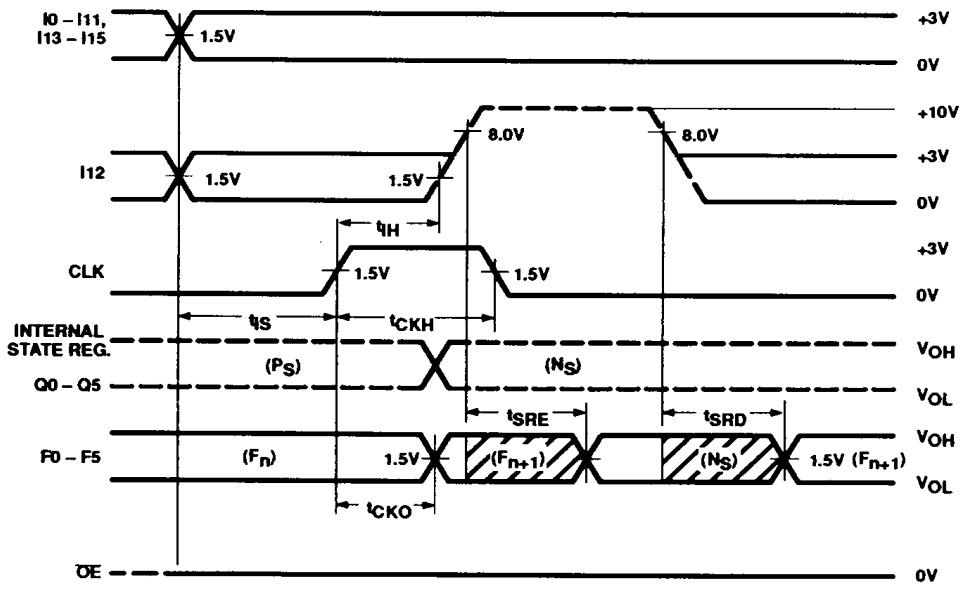
## TIMING DIAGRAMS (Continued)




**Diagnostic Mode—Output Register Input Jam**




**Diagnostic Mode—State Register Input Jam**




**Diagnostic Mode—State Register Outputs**

# Programmable logic sequencer (16 × 48 × 8)

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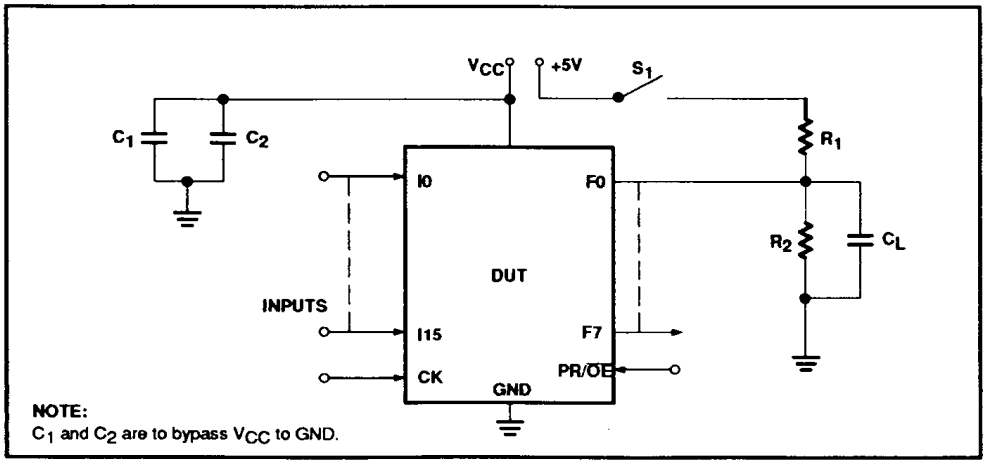
## TIMING DEFINITIONS

| SYMBOL | PARAMETER |
|---|---|
| $t_{IH}$ | Required delay between positive transition of Clock and end of valid Input data. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of Clock. |
| $t_{IS2}$ | Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array). |
| $t_{CKH}$ | Width of input clock pulse |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKO}$ | Delay between positive transition of Clock and when Outputs become valid (with PR/$\overline{OE}$ Low). |
| $t_{CKP}$ | Minimum guaranteed clock period. |
| $t_{NVCK}$ | Required delay between the negative transition of the clock and the negative transition of the Asynchronous PRESET to guarantee that the clock edge is not detected as a valid negative transition. |

| SYMBOL | PARAMETER |
|---|---|
| $t_{OD}$ | Delay between beginning of Output Enable High and when Outputs are in the OFF-state. |
| $t_{OE}$ | Delay between beginning of Output Enable Low and when Outputs become valid. |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power-on) and when Outputs become preset at "1". |
| $t_{PR}$ | Delay between positive transition of Preset and when Outputs become valid at "1". |
| $t_{PRH}$ | Width of preset input pulse. |
| $t_{PRS}$ | Required delay between negative transition of Asynchronous Preset and the first positive transition of Clock. |
| $t_{RH}$ | Required delay between positive transition of clock and the end of valid input data (F0–F7 as inputs), when jamming data into the State or Output registers in the Diagnostic Mode. |

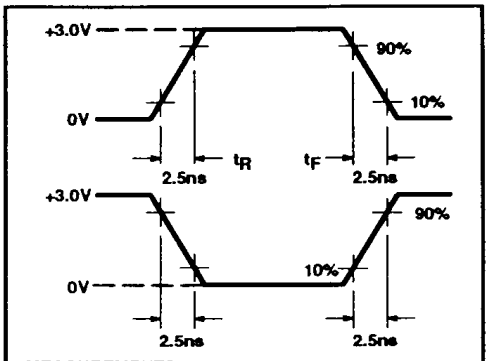
| SYMBOL | PARAMETER |
|---|---|
| $t_{RJH}$ | Required delay between positive transition of clock and return of input I10 or I11 from Diagnostic Mode (8V). |
| $t_{RJS}$ | Required delay between inputs I10 or I11 transition to Diagnostic Mode (8V), and when the output pins become available as inputs. |
| $t_{SRD}$ | Delay between input (I12) transition to Logic mode and when the Outputs reflect the contents of the Output Register. |
| $t_{SRE}$ | Delay between input I12 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register. |
| $t_{VS}$ | Required delay between $V_{CC}$ (after power-on) and negative transition of Clock preceding first reliable clock pulse. |
| $f_{CLK}$ | Minimum guaranteed clock frequency (register toggle frequency) |
| $f_{MAX}$ | Minimum guaranteed operating frequency. |

## TEST LOAD CIRCUITS




NOTE:
$C_1$ and $C_2$ are to bypass $V_{CC}$ to GND.

## VOLTAGE WAVEFORMS




MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

## LOGIC PROGRAMMING

PLUS105-45 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' SLICE and SNAP design software packages. Signetics' AMAZE design software may also be used to compile PLUS105 designs, however, the timing simulator does not reflect the actual performance of the device. ABEL™, CUPL™ and PALASM® 90 design software packages also support the PLUS105–45 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLUS105-45 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by AMAZE and SLICE only. Both AMAZE and SLICE design packages are available, free of charge, to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

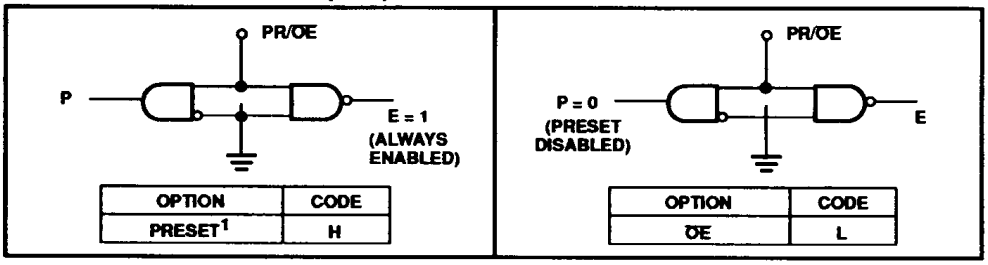
ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

# Programmable logic sequencer (16 × 48 × 8)

# PLUS105–45



## PRESET/OE OPTION – (P/E)

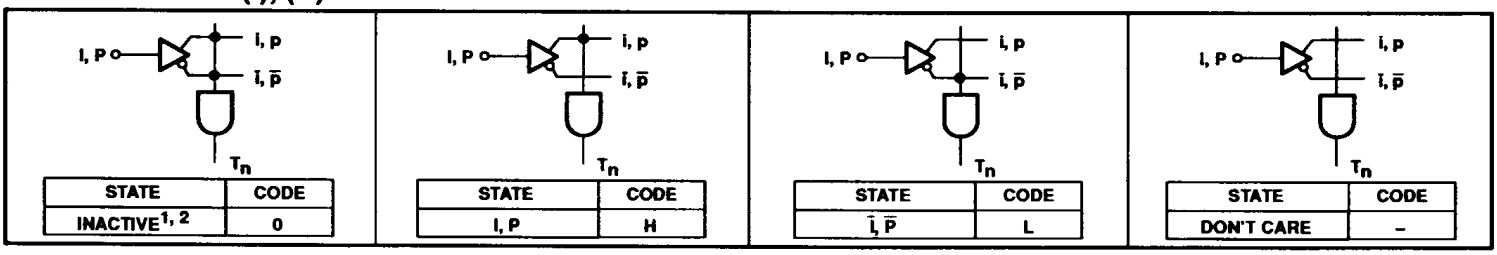



| OPTION | CODE |
|---|---|
| PRESET[1] | H |

| OPTION | CODE |
|---|---|
| $\overline{OE}$ | L |

**PROGRAMMING THE PLUS105–45:**
The PLUS105–45 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

## "AND" ARRAY – (I), (P)



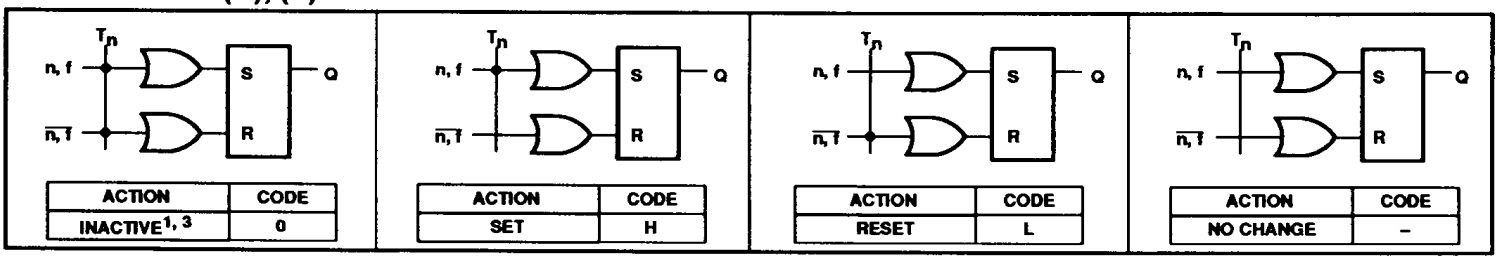

| STATE | CODE |
|---|---|
| INACTIVE[1, 2] | 0 |

| STATE | CODE |
|---|---|
| I, P | H |

| STATE | CODE |
|---|---|
| $\bar{I}$, $\bar{P}$ | L |

| STATE | CODE |
|---|---|
| DON'T CARE | – |

## "OR" ARRAY – (N), (F)



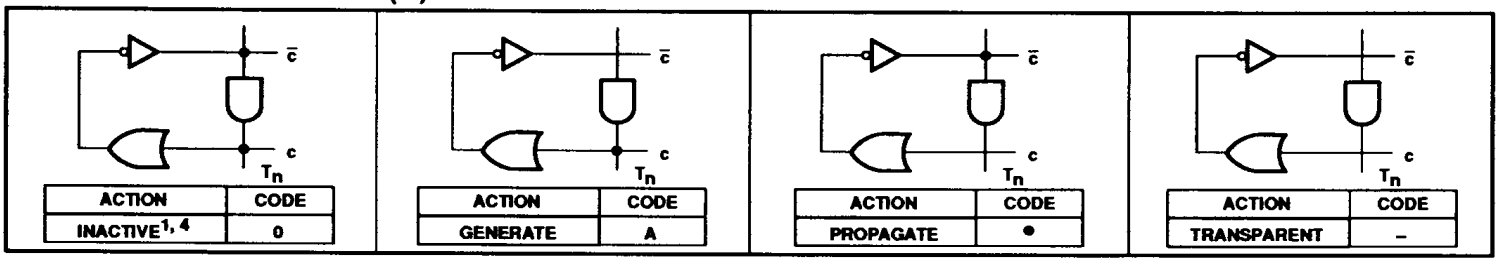

| ACTION | CODE |
|---|---|
| INACTIVE[1, 3] | 0 |

| ACTION | CODE |
|---|---|
| SET | H |

| ACTION | CODE |
|---|---|
| RESET | L |

| ACTION | CODE |
|---|---|
| NO CHANGE | – |

## "COMPLEMENT" ARRAY – (C)




| ACTION | CODE |
|---|---|
| INACTIVE[1, 4] | 0 |

| ACTION | CODE |
|---|---|
| GENERATE | A |

| ACTION | CODE |
|---|---|
| PROPAGATE | • |

| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

**NOTES:**

1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates $T_n$.
2. Any gate $T_n$ will be unconditionally inhibited if both the true and complement fuses of any input (I,P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates $T_n$ (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates $T_n$.

# Programmable logic sequencer (16 × 48 × 8)

PLUS105–45



## PLUS105 PROGRAM TABLE

CUSTOMER NAME _____
PURCHASE ORDER # _____
SIGNETICS DEVICE # CF (XXXX)
CUSTOMER SYMBOLIZED PART # _____
TOTAL NUMBER OF PARTS _____
PROGRAM TABLE _____
REV _____
DATE _____

**PROGRAM TABLE ENTRIES**

**AND**

| | |
|---|---|
| INACTIVE | 0 |
| GENERATE | A |
| PROPAGATE | • |
| TRANSPARENT | — |

$C_n$

| | |
|---|---|
| INACTIVE | 0 |
| I, P | H |
| $\overline{I}$, $\overline{P}$ | L |
| DON'T CARE | — |

$I_m$, $P_s$

**OR**

| | |
|---|---|
| INACTIVE | 0 |
| SET | H |
| RESET | L |
| NO CHANGE | — |

$N_s$, Fr

**OPTION**

| | |
|---|---|
| PRESET | H |
| $\overline{OE}$ | L |

P/E

| TERM | $C_n$ | AND: INPUT ($I_m$) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 | AND: PRESENT STATE ($P_s$) 5 4 3 2 1 0 | REMARKS | OPTION (P/E) OR: NEXT STATE ($N_s$) 5 4 3 2 1 0 | OPTION (P/E) OR: OUTPUT (Fr) 7 6 5 4 3 2 1 0 |
|---|---|---|---|---|---|---|
| 0 | | | | | | |
| 1 | | | | | | |
| 2 | | | | | | |
| 3 | | | | | | |
| 4 | | | | | | |
| 5 | | | | | | |
| 6 | | | | | | |
| 7 | | | | | | |
| 8 | | | | | | |
| 9 | | | | | | |
| 10 | | | | | | |
| 11 | | | | | | |
| 12 | | | | | | |
| 13 | | | | | | |
| 14 | | | | | | |
| 15 | | | | | | |
| 16 | | | | | | |
| 17 | | | | | | |
| 18 | | | | | | |
| 19 | | | | | | |
| 20 | | | | | | |
| 21 | | | | | | |
| 22 | | | | | | |
| 23 | | | | | | |
| 24 | | | | | | |
| 25 | | | | | | |
| 26 | | | | | | |
| 27 | | | | | | |
| 28 | | | | | | |
| 29 | | | | | | |
| 30 | | | | | | |
| 31 | | | | | | |
| 32 | | | | | | |
| 33 | | | | | | |
| 34 | | | | | | |
| 35 | | | | | | |
| 36 | | | | | | |
| 37 | | | | | | |
| 38 | | | | | | |
| 39 | | | | | | |
| 40 | | | | | | |
| 41 | | | | | | |
| 42 | | | | | | |
| 43 | | | | | | |
| 44 | | | | | | |
| 45 | | | | | | |
| 46 | | | | | | |
| 47 | | | | | | |
| PIN NO. | | 20 21 22 23 24 25 26 27 2 3 4 5 6 7 8 9 | | | | 10 11 12 13 15 16 17 18 |
| VARIABLE NAME | | | | | | |

**NOTES:**

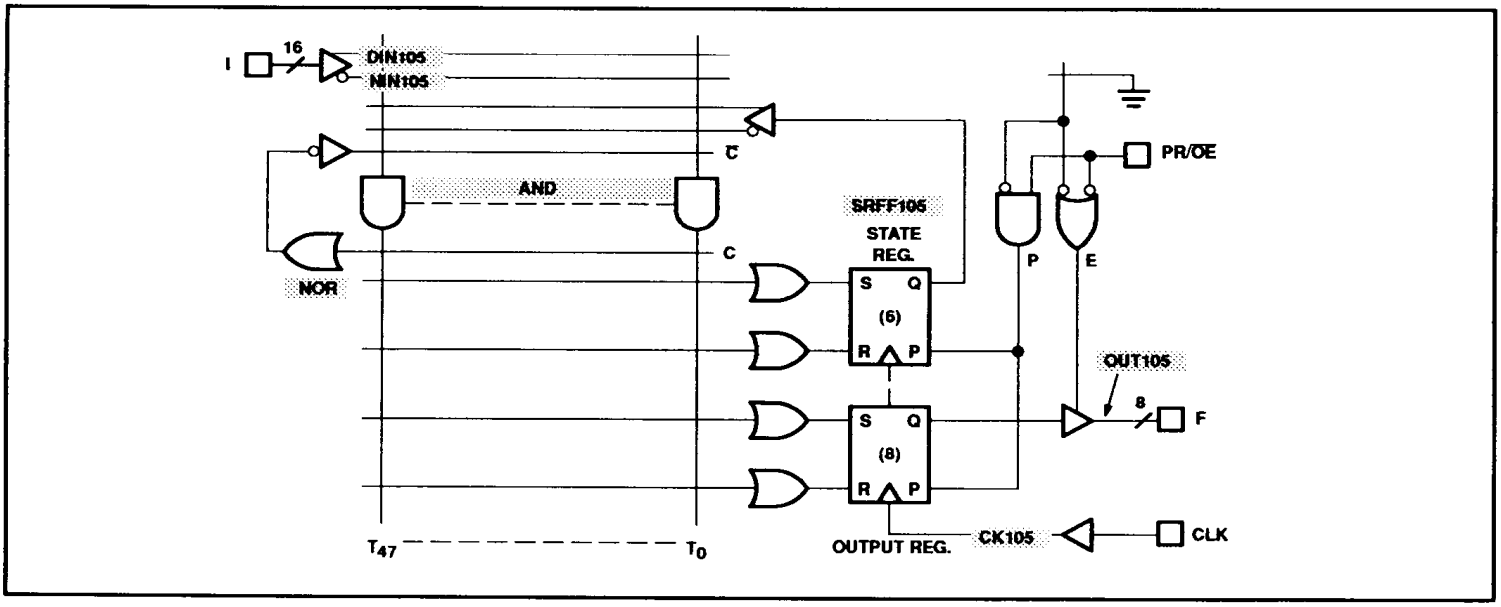
1. The device is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exists in the table, shown BLANK instead for clarity.
2. Unused $C_n$, $I_m$, and $P_s$ bits are normally programmed Don't Care (–).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (–) for maximum speed.
4. Letters in variable fields are used as identifiers by logic type programmers.

# Programmable logic sequencer (16 × 48 × 8)

PLUS105–45



## SNAP RESOURCE SUMMARY DESIGNATIONS



# Programmable logic sequencer (16 × 48 × 8)

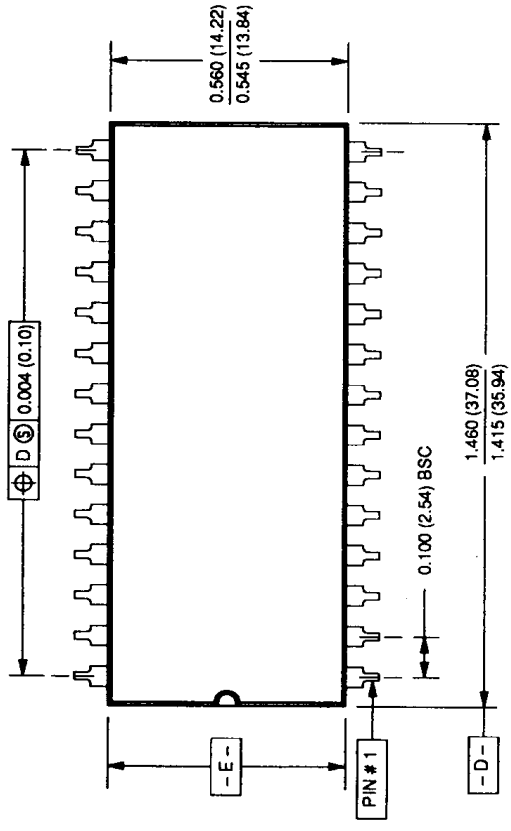
PLUS105-45

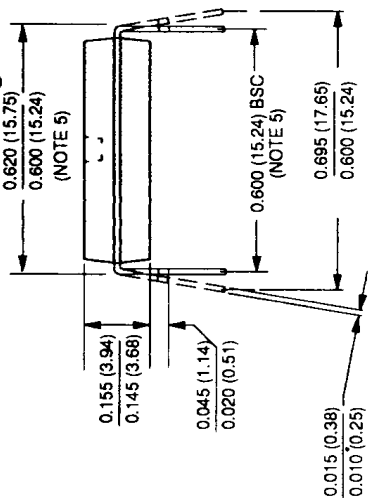


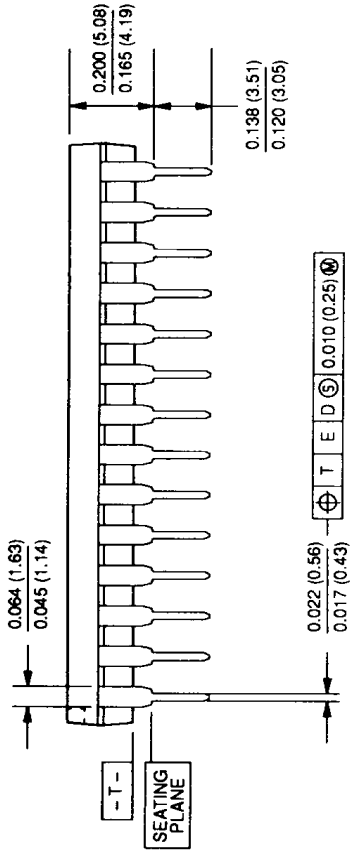
## 28-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

**NOTES:**

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AB for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 28 leads (Issue B, 7/84).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #28 when viewed from the top.




853-0413B 01988

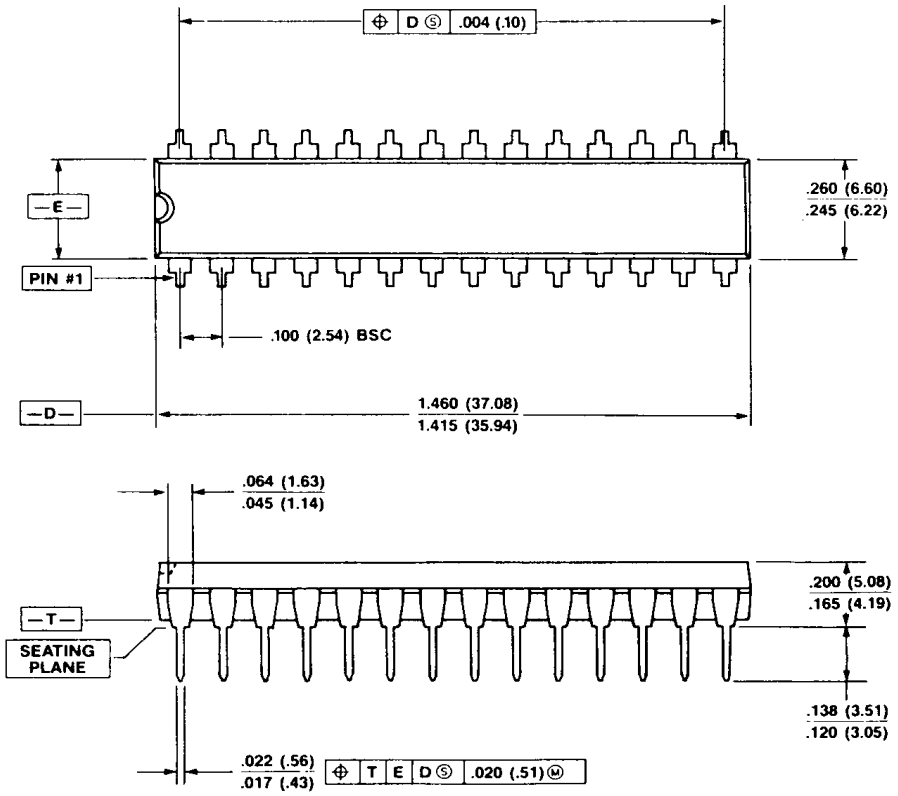
NQ3

# Programmable logic sequencer (16 × 48 × 8)





## 28-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N3) PACKAGE




**NOTES:**

1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensions are tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the molded body and do not include mold-flash or protrusions which shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0864 89398

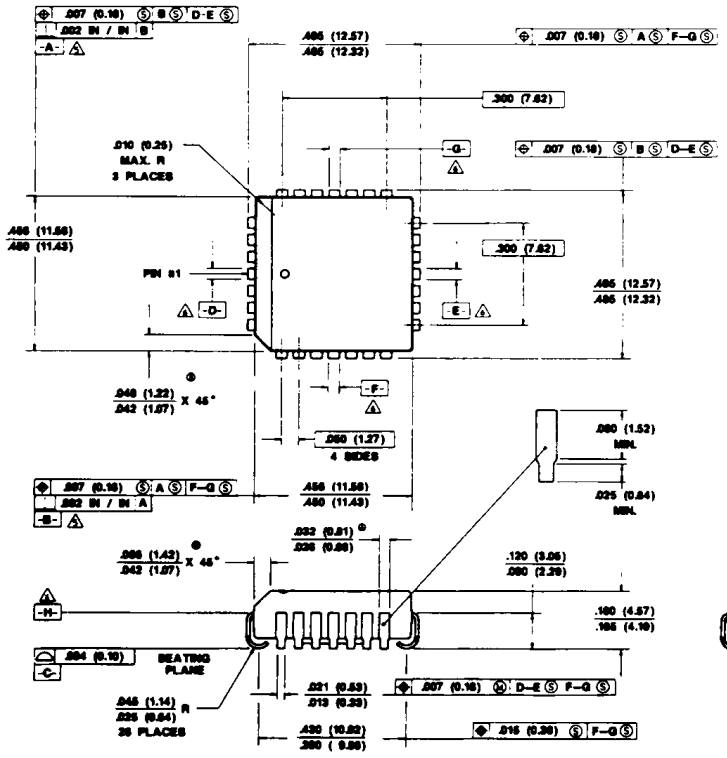
NQ1

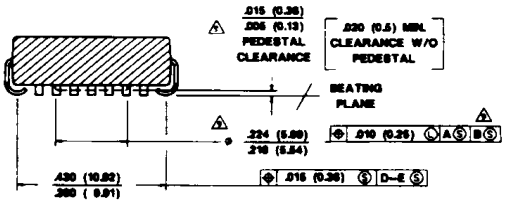
# Programmable logic sequencer (16 × 48 × 8)

PLUS105–45



## 28-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE




AQ1 853-0401 93885

**NOTES:**

1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #28 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

# Programmable logic sequencer (16 × 48 × 8)

PLUS105–45



## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | Full Production | This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product. |



Signetics

a subsidiary of North American Philips Corporation

**Signetics Company**
**811 East Arques Avenue**
**P.O. Box 3409**
**Sunnyvale, California 94088–3409**
**Telephone 408/991–2000**



98–7000–300 1186B/FP/4M/0691