

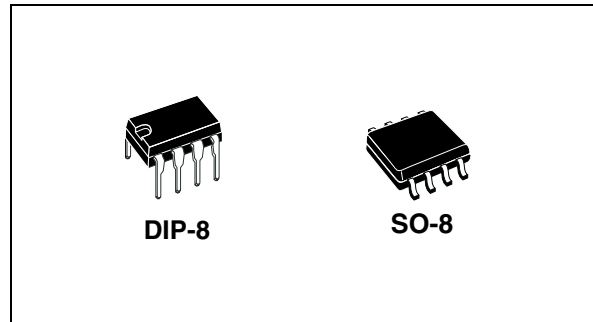
High voltage high and low side driver

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability:
 - 290 mA source,
 - 430 mA sink
- Switching times 75/35 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS input comparators with hysteresis
- Integrated bootstrap diode
- Fixed 320 ns dead-time
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design

Applications

- Motor driver for home appliances, factory automation, industrial drives and fans.



Description

The L6398 is a high-voltage device manufactured with the BCD “OFF-LINE” technology. It is a single chip half-bridge gate driver for N-channel power MOSFET or IGBT.

The high side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing microcontroller/DSP.

Table 1. Device summary

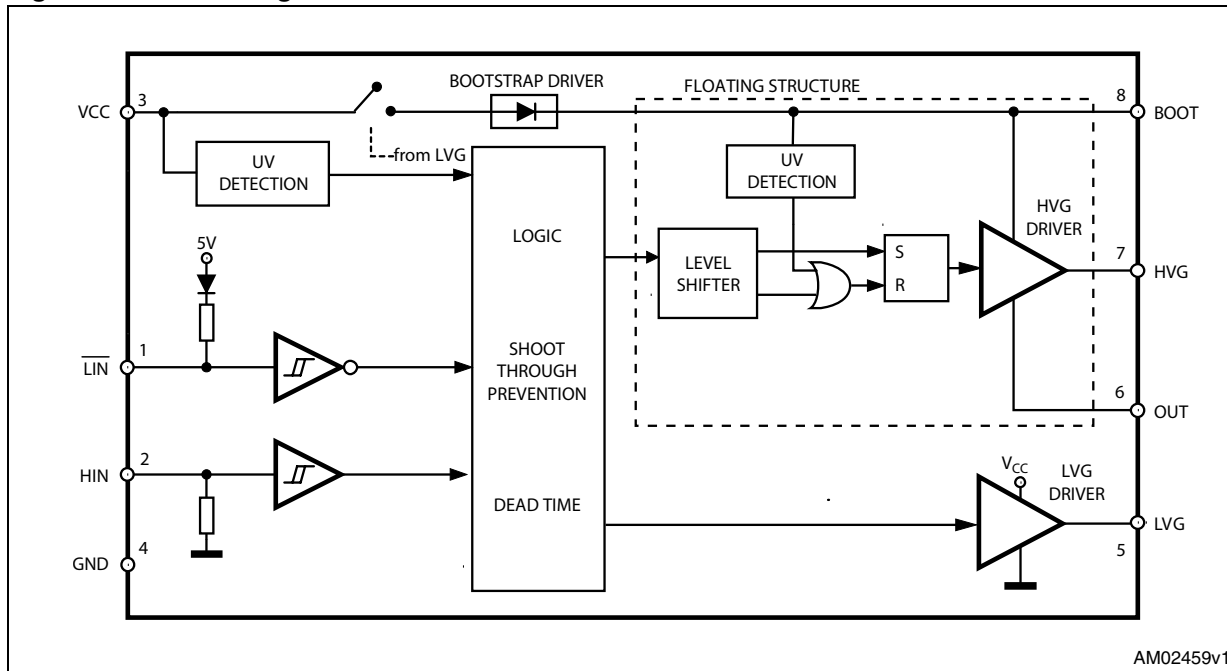
Order codes	Package	Packaging
L6398N	DIP-8	Tube
L6398D	SO-8	Tube
L6398DTR	SO-8	Tape and reel

Contents

1	Block diagram	3
2	Pin connection	4
3	Truth table	5
4	Electrical data	6
	4.1 Absolute maximum ratings	6
	4.2 Thermal data	6
	4.3 Recommended operating conditions	6
5	Electrical characteristics	7
	5.1 AC operation	7
	5.2 DC operation	8
6	Waveforms definitions	9
7	Typical application diagram	10
8	Bootstrap driver	11
	8.1 CBOOT selection and charging	11
9	Package mechanical data	13
10	Revision history	15

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

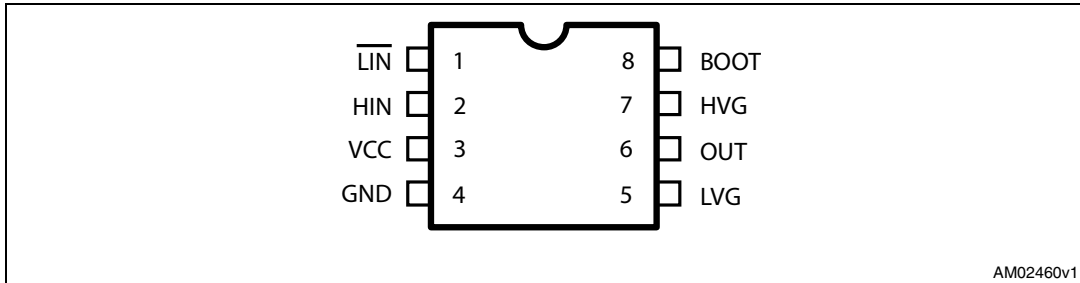


Table 2. Pin description

Pin n #	Pin name	Type	Function
1	$\overline{\text{LIN}}$	I	Low side driver logic input (active low)
2	HIN	I	High side driver logic input (active high)
3	VCC	P	Lower section supply voltage
4	GND	P	Ground
5	LVG ⁽¹⁾	O	Low side driver output
6	OUT	P	High side (floating) common voltage
7	HVG ⁽¹⁾	O	High side driver output
8	BOOT	P	Bootstrapped supply voltage

1. The circuit guarantees less than 1 V on the LVG and HVG pins (@ $I_{\text{sink}} = 10 \text{ mA}$), with $V_{\text{CC}} > 3 \text{ V}$. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

3 Truth table

Table 3. Truth table

Input		Output	
$\overline{\text{LIN}}$	HIN	LVG	HVG
H	L	L	L
L	H	L	L
L	L	H	L
H	H	L	H

4 Electrical data

4.1 Absolute maximum ratings

Table 4. Absolute maximum rating

Symbol	Parameter	Value		Unit
		Min	Max	
V _{cc}	Supply voltage	-0.3	21	V
V _{out}	Output voltage	V _{boot} - 21	V _{boot} + 0.3	V
V _{boot}	Bootstrap voltage	-0.3	620	V
V _{hvg}	High side gate output voltage	V _{out} - 0.3	V _{boot} + 0.3	V
V _{lvg}	Low side gate output voltage	-0.3	V _{cc} + 0.3	V
V _i	Logic input voltage	-0.3	15	V
dV _{out} /dt	Allowed output slew rate		50	V/ns
P _{tot}	Total power dissipation (T _A = 25 °C)		800	mW
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-50	150	°C

Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 1 kV (human body model)

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	SO-8	DIP-8	Unit
R _{th(JA)}	Thermal resistance junction to ambient	150	100	°C/W

4.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min	Max	Unit
V _{cc}	3	Supply voltage		10	20	V
V _{BO} ⁽¹⁾	8-6	Floating supply voltage		9.8	20	V
V _{out}	6	Output voltage		- 11 ⁽²⁾	580	V
f _{sw}		Switching frequency	HVG, LVG load C _L = 1 nF		800	kHz
T _J		Junction temperature		-40	125	°C

- V_{BO} = V_{boot} - V_{out}
- LVG off. V_{cc} = 10 V
Logic is operational if V_{boot} > 5 V

5 Electrical characteristics

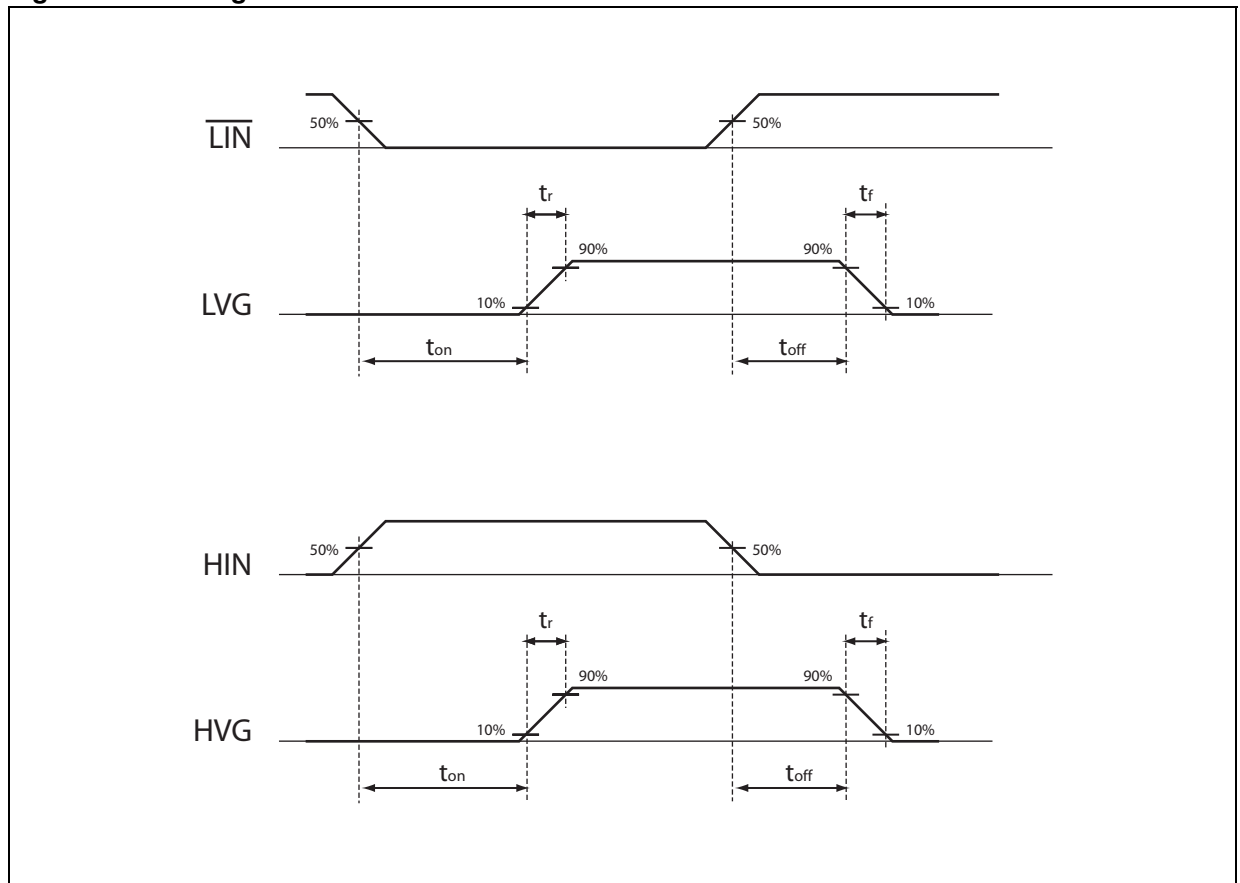
5.1 AC operation

Table 7. AC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ }^\circ\text{C}$)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
t_{on}	1, 2 vs 5, 7	High/low side driver turn-on propagation delay	$V_{out} = 0\text{ V}$ $V_{boot} = V_{CC}$	50	125	200	ns
t_{off}		High/low side driver turn-off propagation delay	$C_L = 1\text{ nF}$ $V_{IN} = 0\text{ to }3.3\text{ V}$ See Figure 3	50	125	200	ns
DT		Dead time ⁽¹⁾	$C_L = 1\text{ nF}$	225	320	415	ns
t_r	5, 7	Rise time	$C_L = 1\text{ nF}$		75	120	ns
t_f		Fall time	$C_L = 1\text{ nF}$		35	70	ns

1. See [Figure 4](#) on page 9.

Figure 3. Timing



5.2 DC operation

Table 8. DC operation electrical characteristics (V_{CC} = 15 V; T_J = + 25 °C)

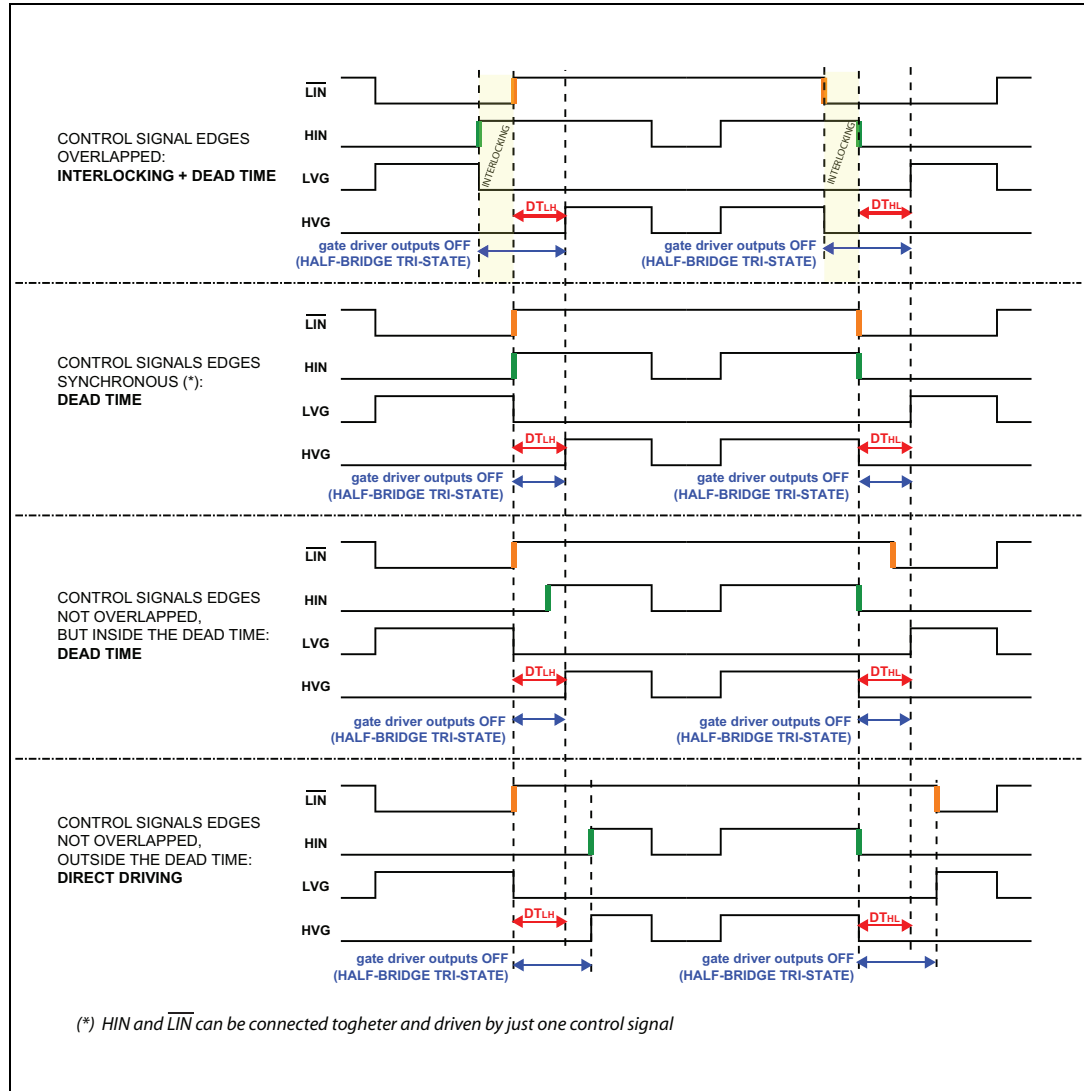
Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
V _{CC_hys}	3	V _{CC} UV hysteresis		1.2	1.5	1.8	V
V _{CC_thON}		V _{CC} UV turn ON threshold		9	9.5	10	V
V _{CC_thOFF}		V _{CC} UV turn OFF threshold		7.6	8	8.4	V
I _{qccu}		Undervoltage quiescent supply current	V _{CC} = 7 V LIN = 5 V; HIN = GND;		90	150	μA
I _{qcc}		Quiescent current	V _{CC} = 15 V LIN = 5 V; HIN = GND;		380	440	μA
Bootstrapped supply voltage section (1)							
V _{BO_hys}	8	V _{BO} UV hysteresis		0.8	1	1.2	V
V _{BO_thON}		V _{BO} UV turn ON threshold		8.2	9	9.8	V
V _{BO_thOFF}		V _{BO} UV turn OFF threshold		7.3	8	8.7	V
I _{QBOU}		Undervoltage V _{BO} quiescent current	V _{BO} = 7 V, LIN = HIN = 5V		30	60	μA
I _{QBO}		V _{BO} quiescent current	V _{BO} = 15 V, LIN = HIN = 5V		190	240	μA
I _{LK}		High voltage leakage current	V _{hvg} = V _{out} = V _{boot} = 600 V			10	μA
R _{DS(on)}		Bootstrap driver on resistance (2)	LVG ON		120		Ω
Driving buffers section							
I _{so}	5, 7	High/low side source short circuit current	V _{IN} = V _{ih} (t _p < 10 μs)	200	290		mA
I _{si}		High/low side sink short circuit current	V _{IN} = V _{il} (t _p < 10 μs)	250	430		mA
Logic inputs							
V _{il}	1, 2	Low logic level voltage				0.8	V
V _{ih}		High logic level voltage		2.25			V
V _{il_S}	1, 2	Single input voltage	LIN and HIN connected together and floating			0.8	V
I _{HINh}	2	HIN logic "1" input bias current	HIN = 15 V	110	175	260	μA
I _{HINl}		HIN logic "0" input bias current	HIN = 0 V			1	μA
I _{LINl}	1	LIN logic "0" input bias current	LIN = 0 V	3	6	20	μA
I _{LINh}		LIN logic "1" input bias current	LIN = 15 V			1	μA

1. V_{BO} = V_{boot} - V_{out}

2. R_{DS(on)} is tested in the following way: R_{DS(on)} = [(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})] / [I₁(V_{CC}, V_{CBOOT1}) - I₂(V_{CC}, V_{CBOOT2})] where I₁ is pin 8 current when V_{CBOOT} = V_{CBOOT1}, I₂ when V_{CBOOT} = V_{CBOOT2}.

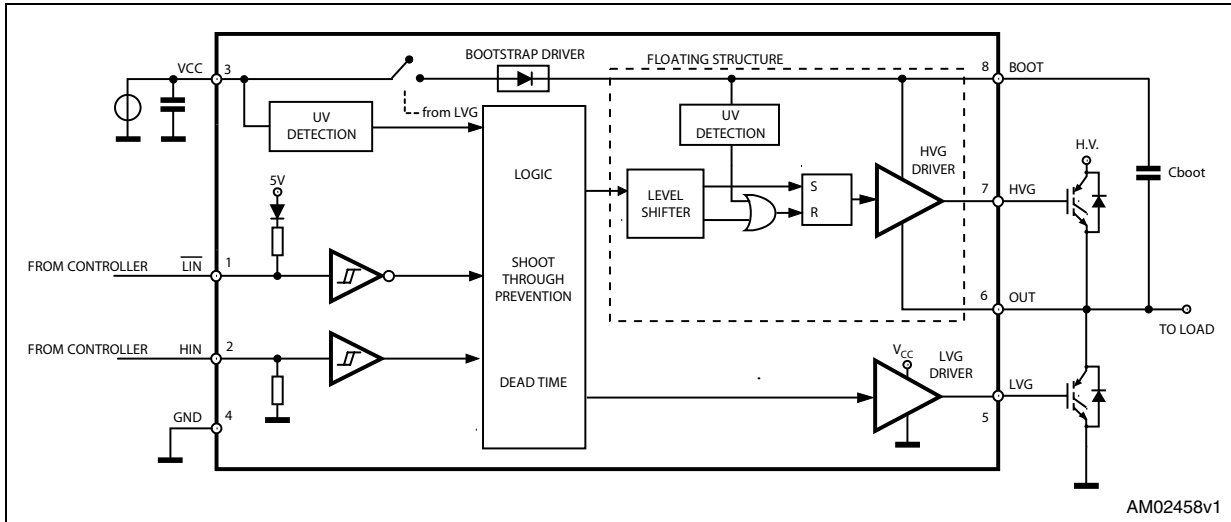
6 Waveforms definitions

Figure 4. Dead time and interlocking waveforms definitions



7 Typical application diagram

Figure 5. Application diagram



8 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 6*). In the L6398 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with diode in series, as shown in *Figure 7*. An internal charge pump (*Figure 7*) provides the DMOS driving voltage.

8.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} \gg \gg C_{EXT}$$

e.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

e.g.: HVG steady state consumption is lower than 190 μA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 μC to C_{EXT}. This charge on a 1 μF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 μ s. In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 120\Omega \sim 0.7V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 6. Bootstrap driver with high voltage fast recovery diode

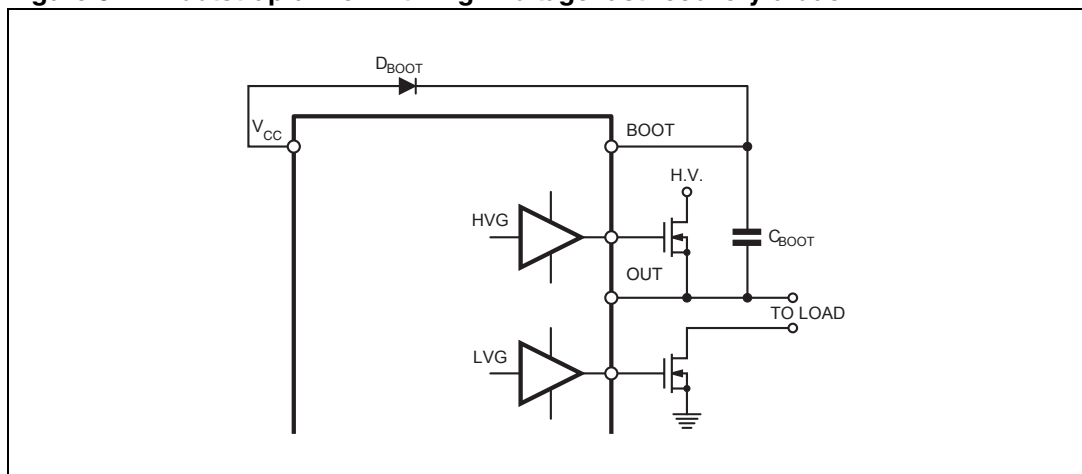
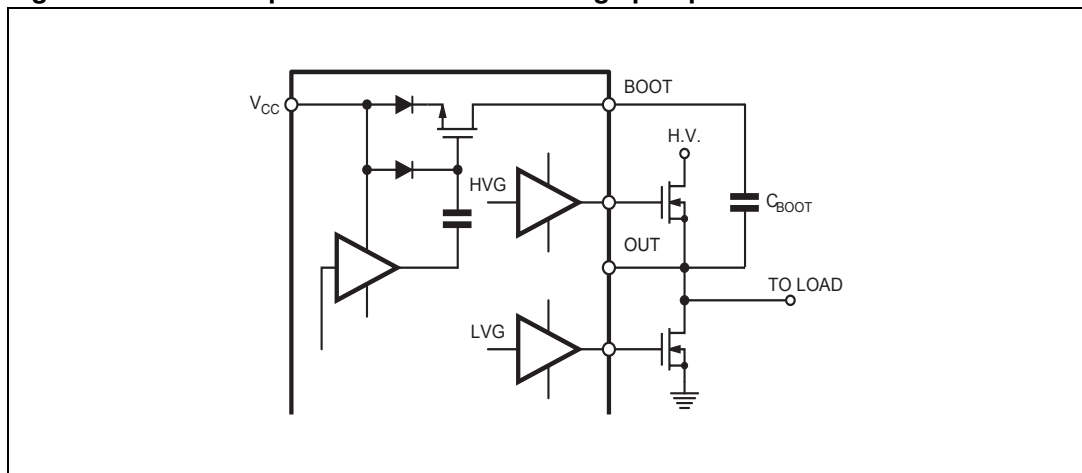


Figure 7. Bootstrap driver with internal charge pump



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. DIP-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

Figure 8. Package dimensions

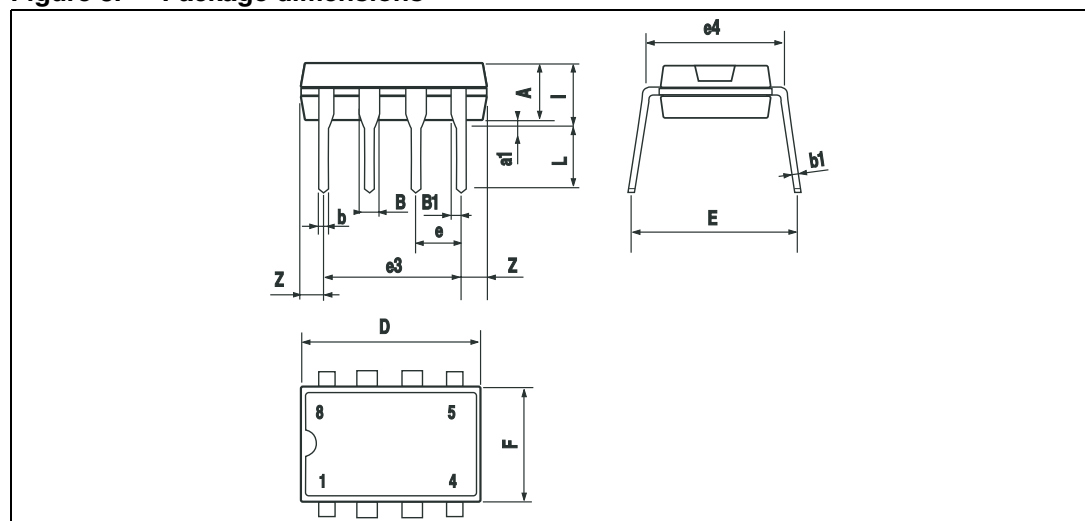
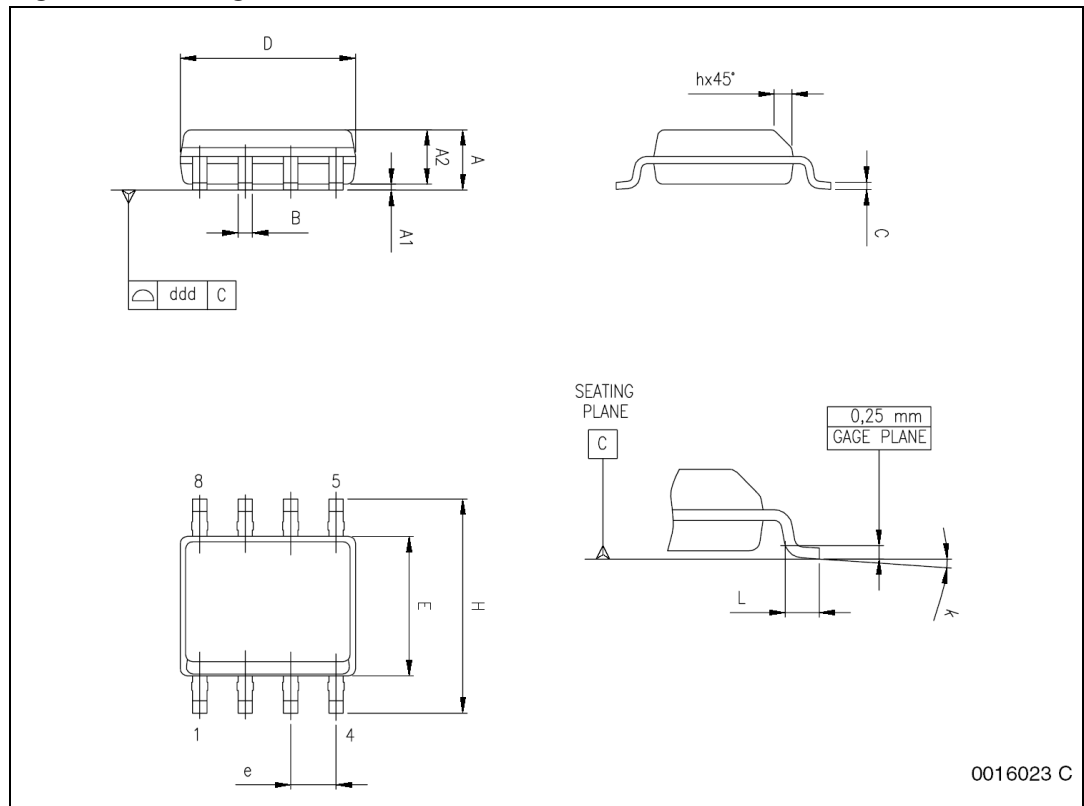


Table 1. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 9. Package dimensions



10 Revision history

Table 10. Document revision history

Date	Revision	Changes
14-Dec-2010	1	First release.
16-Feb-2011	2	Updated Table 8 .
01-Apr-2011	3	Typo in coverpage

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