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ELECTRICAL SPECIFICATIONS (STANDARD)

This section contains the electrical specifications and associated timing information for the standard supply voltage (V_{DD} = 5V ± 10%) MC68HC11P2 variants.

12.1　Maximum ratings

Rating	Symbol	Value	Unit
Supply voltage [1]	V_{DD}	– 0.3 to +7.0	V
Input voltage [1]	V_{in}	– 0.3 to +7.0	V
Operating temperature range – MC68HC11P2, *MC68HC711P2*	T_A	T_L to T_H –40 to +85	°C
Storage temperature range	T_{stg}	– 55 to +150	°C
Current drain per pin [2] – not VDD, VSS, VDD AD, VSS AD, VRH or VRL	I_D	25	mA

(1) All voltages are with respect to V_{SS}.

(2) Maximum current drain per pin is for one pin at a time, observing maximum power dissipation limits.

Note:　This device contains circuitry designed to protect against damage due to high electrostatic voltages or electric fields. However, it is recommended that normal precautions be taken to avoid the application of any voltages higher than those given in the maximum ratings table to this high impedance circuit. For maximum reliability all unused inputs should be tied to either V_{SS} or V_{DD}.

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12.2   Thermal characteristics and power considerations

The average chip junction temperature, T_J, in degrees Celsius can be obtained from the following equation:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$ [1]

where:

T_A = Ambient temperature (°C)

θ_{JA} = Package thermal resistance, junction-to-ambient (°C/W)

P_D = Total power dissipation = $P_{INT} + P_{I/O}$ (W)

P_{INT} = Internal chip power = $I_{DD} \bullet V_{DD}$ (W)

$P_{I/O}$ = Power dissipation on input and output pins (User determined)

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{T_J + 273}$$ [2]
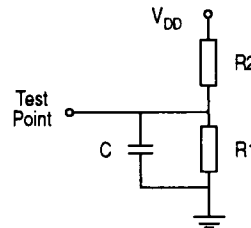
Solving equations [1] and [2] for K gives:

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$$ [3]

where K is a constant for a particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained for any value of T_A, by solving the above equations. The package thermal characteristics are shown below:
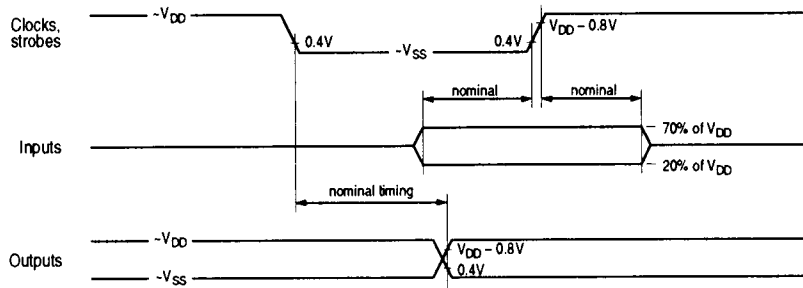
Characteristics	Symbol	Value	Unit
Thermal resistance	θ_{JA}		°C/W
– 84-pin PLCC package		50	
– 84-pin CERQUAD package (EPROM)		50	
– 88-pin QFP package		TBD	

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12.3   Test methods

Pins	R1	R2	C
PA[7:0], PB[7:0], PC[7:0], PD5, PD0, E, R/$\overline{W}$, AS	3.26kΩ	2.38kΩ	90pF
PD[4:1]	3.26kΩ	2.38kΩ	200pF

(a) Equivalent test loads

(b) DC testing

(c) AC testing

Notes:

(1) Full test loads are applied during all DC electrical tests and AC timing measurements.

(2) During AC timing measurements, inputs are driven to 0.4 V and V_{DD} – 0.8 V; timing measurements are taken at the 20% and 70% of V_{DD} points.

Figure 12-1   Test methods

12.4 DC electrical characteristics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
Output voltage[1] (I_{LOAD} = ± 10 μA):				
All outputs except XTAL	V_{OL}	—	0.1	V
All outputs except XTAL, RESET & MODA	V_{OH}	V_{DD} – 0.1	—	V
Output high voltage[1] (I_{LOAD} = –0.8 mA, V_{DD} =4.5 V):				
All outputs except XTAL, RESET & MODA	V_{OH}	V_{DD} – 0.8	—	V
Output low voltage (I_{LOAD} = +1.6 mA):				
All outputs except XTAL	V_{OL}	—	0.4	V
Input high voltage:	V_{IH}			V
All inputs except RESET		$0.7 V_{DD}$	V_{DD} + 0.3	
RESET		$0.8 V_{DD}$	V_{DD} + 0.3	
Input low voltage – all inputs	V_{IL}	V_{SS} – 0.3	$0.2 V_{DD}$	V
I/O ports tristate leakage (v_{IN} = V_{IH} or V_{IL}):				
Ports A, B, C, D, F, G, H, MODA/LIR, RESET	I_{OZ}	—	±10	μA
Input leakage[2] (v_{IN} = V_{DD} or V_{SS}):	I_{IN}			μA
IRQ, XIRQ (ROM parts)		—	±1	
MODB/VSTBY, XIRQ (EPROM parts)		—	±10	
Input current with pull-up resistors (v_{IN} = V_{IL}):				
Ports B, F, G, H	I_{IPR}	100	500	μA
RAM stand-by voltage (power down)	V_{SB}	2.0	V_{DD}	V
RAM stand-by current (power down)	I_{SB}	—	10	μA
Input capacitance:	C_{IN}			pF
Port E, IRQ, XIRQ, EXTAL		—	8	
Ports A, B, C, D, F, G, H, MODA/LIR, RESET		—	12	
Output load capacitance:	C_L			pF
All outputs except PD[4:1], XTAL, MODA/LIR		—	90	
PD[4:1]		—	200	

(1) V_{OH} specification for RESET and MODA is not applicable as they are open-drain pins.
    V_{OH} specification is not applicable to ports C and D in wired-OR mode.

(2) Refer to A/D specification for the leakage current value for port E.

Characteristic	Symbol	2 MHz	3 MHz	4 MHz	Unit
Maximum total supply current (including PLL)[1]:	I_{DD}				
RUN: Single chip mode		27	32	40	mA
RUN: Expanded mode		35	42	50	mA
WAIT: Single chip mode[2]		10	15	20	mA
WAIT: Expanded mode[2]		12	17	22	mA
STOP: Single chip mode		50	50	50	μA
Power dissipation: Single chip mode	P_D	149	176	220	mW
Power dissipation: Expanded mode		193	231	275	

(1) All current measurements taken with suitable decoupling capacitors across the power supply to suppress the transient switching currents inherent in CMOS designs.
    EXTAL is driven with a square wave, with t_{CYC} = 500/333/250 ns for 2/3/4 MHz devices.
    VIL ≤ 0.2 V; VIH ≥ VDD – 0.2 V; no DC loads
    WAIT: all peripheral functions shut down   STOP: all clocks stopped
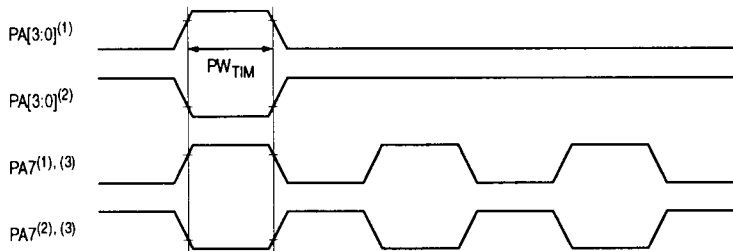
(2) If the PLL low-power WAIT mode is selected (WEN = 1) then, with an external clock of 614 kHz, the supply current will not exceed 1 mA in single chip mode, or 2 mA in expanded mode.

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12.5 Control timing

$(V_{DD} = 5.0\ Vdc \pm 10\%, V_{SS} = 0\ Vdc, T_A = T_L\ to\ T_H)$

Characteristic [1]	Symbol	2.0 MHz Min.	2.0 MHz Max.	3.0 MHz Min.	3.0 MHz Max.	4.0 MHz Min.	4.0 MHz Max.	Unit
Frequency of operation	f_{OP}	0	2.0	0	3.0	0	4.0	MHz
E clock period	t_{CYC}	500	—	333	—	250	—	ns
Crystal frequency	f_{XTAL}	—	8.0	—	12.0	—	16.0	MHz
External oscillator frequency	$4f_{OP}$	0	8.0	0	12.0	0	16.0	MHz
Processor control set-up time $(t_{PCSU} = t_{CYC}/4 + 50ns)$	t_{PCSU}	175	—	133	—	112	—	ns
Reset input pulse width [2]	PW_{RSTL}[3] PW_{RSTL}[4]	8 1	— —	8 1	— —	8 1	— —	t_{CYC}
Mode programming set-up time	t_{MPS}	2	—	2	—	2	—	t_{CYC}
Mode programming hold time	t_{MPH}	10	—	10	—	10	—	ns
Interrupt pulse width (IRQ edge sensitive mode)	PW_{IRQ}	t_{CYC} +20	—	t_{CYC} +20	—	t_{CYC} +20	—	ns
Timer pulse width (Input capture and pulse accumulator inputs)	PW_{TIM}	t_{CYC} +20	—	t_{CYC} +20	—	t_{CYC} +20	—	ns
WAIT recovery start-up time	t_{WRS}	—	4	—	4	—	4	t_{CYC}
Clock monitor reset	f_{CMON}	10	200	10	200	10	200	kHz
PLL crystal frequency	f_{XTAL}	—	2.0	—	2.0	—	2.0	MHz
PLL stabilization time	t_{PLLS}	—	TBD	—	TBD	—	TBD	ms

(1) All timing is given with respect to 20% and 70% of V_{DD}, unless otherwise noted.

(2) Reset is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin and samples the pin level two cycles later to determine the source of the interrupt. (See Section 10.)

(3) To guarantee an external reset vector.

(4) This is the minimum input time; it can be pre-empted by an internal reset.

Figure 12-2 Timer inputs

Notes
(1) Rising edge sensitive input.
(2) Falling edge sensitive input.
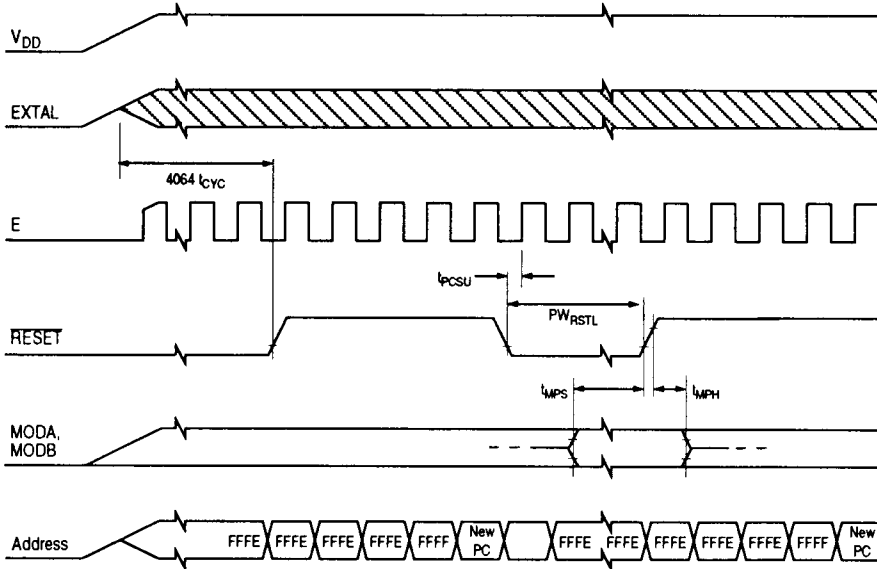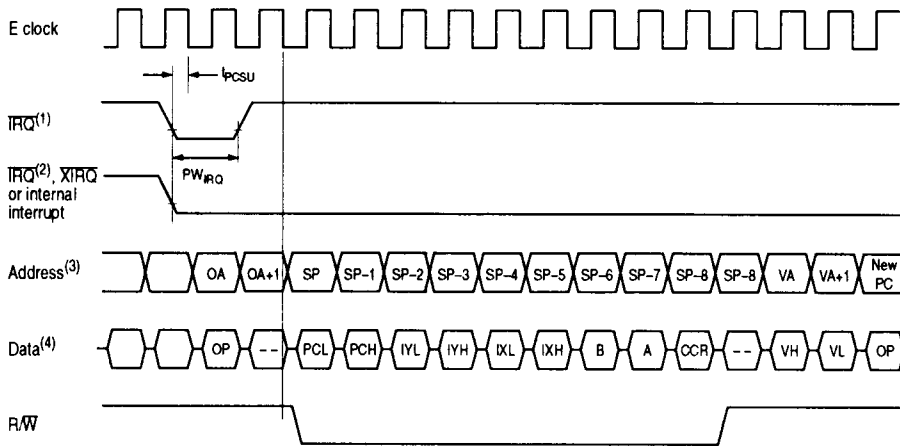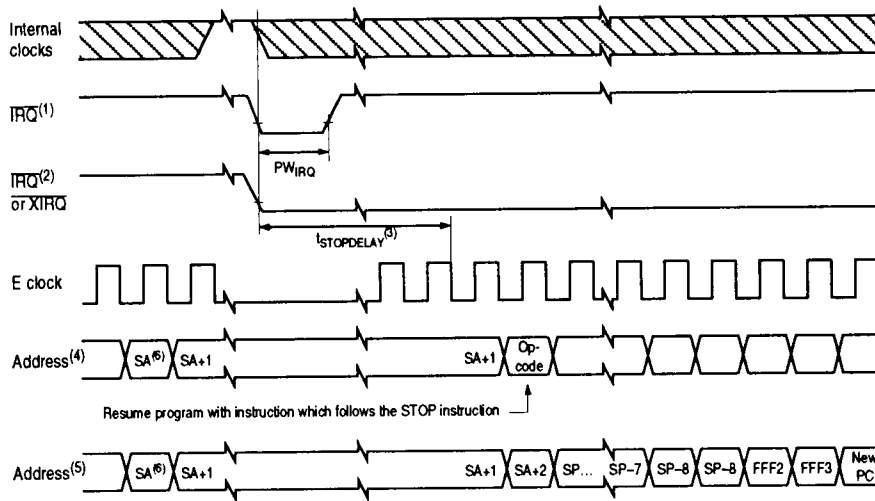(3) Maximum pulse accumulator clocking rate is E clock frequency divided by two (E/2).

Figure 12-3 Reset timing

Notes:
(1) Edge sensitive $\overline{IRQ}$ pin (IRQE = 1).
(2) Level sensitive $\overline{IRQ}$ pin (IRQE = 0).
(3) Where OA = Opcode address and VA = Vector address.
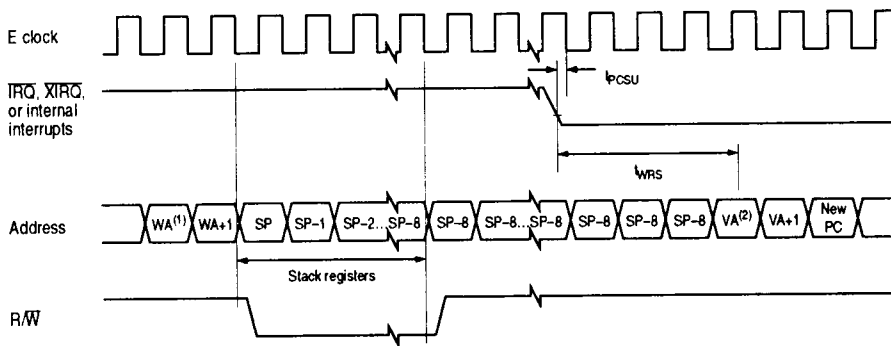(4) Where OP = Opcode, VH = Vector (MSB) and VL = Vector (LSB).

Figure 12-4 Interrupt timing

Notes:

(1) Edge sensitive $\overline{IRQ}$ pin (IRQE = 1).
(2) Level sensitive $\overline{IRQ}$ pin (IRQE = 0).
(3) $t_{STOPDELAY} = 4064\ t_{CYC}$ (DLY = 1) or $4\ t_{CYC}$ (DLY = 0).
(4) $\overline{XIRQ}$ with X-bit in CCR = 1.
(5) $\overline{IRQ}$ (or $\overline{XIRQ}$, with X-bit = 0; in this case vector fetch will be $FFF4/5).
(6) SA = STOP address.

Figure 12-5 STOP recovery timing

Notes:

$\overline{RESET}$ also causes recovery from WAIT.

(1) WA = WAIT address.

(2) VA = Vector address.

Figure 12-6 WAIT recovery timing

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12.5.1 Peripheral port timing

Characteristic [1]	Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Frequency of operation (E clock frequency)	f_{OP}	0	2.0	0	3.0	0	4.0	MHz
E clock period	t_{CYC}	500	—	333	—	250	—	ns
Peripheral data set-up time, all ports [2]	t_{PDSU}	100	—	100	—	100	—	ns
Peripheral data hold time, all ports [2]	t_{PDH}	50	—	50	—	50	—	ns
Delay time, peripheral data write	t_{PWD}							ns
MCU write to port A, B, G or H		—	200	—	200	—	200	
MCU write to port C, D or F		—	225	—	183	—	162	

(1) All timing is given with respect to 20% and 70% of V_{DD}, unless otherwise noted.

(2) Port C and D timing is valid for active drive (CWOM and DWOM bits clear in OPT2 and SPCR registers, respectively).
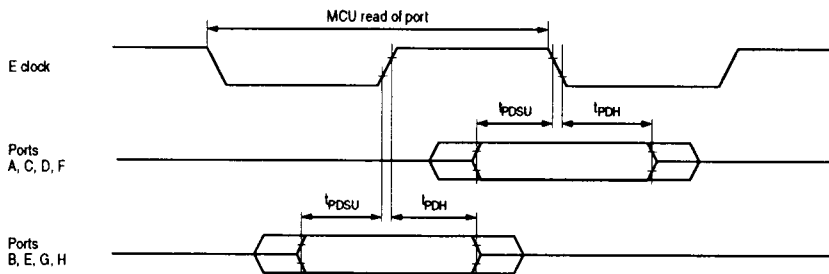

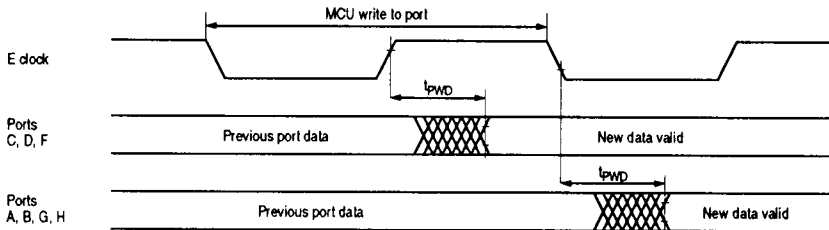**Figure 12-7**   Port read timing diagram

Figure 12-8   Port write timing diagram

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12.5.2 Analog-to-digital converter characteristics

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, 750 kHz ≤ E ≤ 4 MHz, unless otherwise noted)

Characteristic	Parameter	Min.	Absolute	2 MHz[1] Max.	3 MHz[1] Max.	4 MHz[1] Max.	Unit
Resolution	Number of bits resolved by ADC	—	8	—	—	—	bits
Non-linearity	Maximum deviation from the ideal ADC transfer characteristics	—	—	±0.5	±1	±1	LSB
Zero error	Difference from the output of an ideal ADC for zero input voltage	—	—	±0.5	±1	±1	LSB
Full-scale error	Difference from the output of an ideal ADC for full-scale input voltage	—	—	±0.5	±1	±1	LSB
Total unadjusted error	Maximum sum of non-linearity, zero and full-scale errors	—	—	±0.5	±1.5	±1.5	LSB
Quantization error	Uncertainty due to converter resolution	—	—	±0.5	±0.5	±0.5	LSB
Absolute accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, including all error sources	—	—	±1	±2	±2	LSB
Conversion range	Analog input voltage range	V_{RL}	—	V_{RH}	V_{RH}	V_{RH}	V
V_{RH}	Analog reference voltage (high) [2]	V_{RL}	—	V_{DD}+0.1	V_{DD}+0.1	V_{DD}+0.1	V
V_{RL}	Analog reference voltage (low) [2]	V_{SS}−0.1	—	V_{RH}	V_{RH}	V_{RH}	V
ΔV_R	Minimum difference between V_{RH} and V_{RL} [2]	3	—	—	—	—	V
Conversion time	Total time to perform a single A/D conversion: E clock / Internal RC oscillator	— / —	32 / —	— / t_{CYC}+32	— / t_{CYC}+32	— / t_{CYC}+32	t_{CYC} / µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	Guaranteed					
Zero input reading	Conversion result when V_{IN} = V_{RL}	$00	—	—	—	—	Hex
Full-scale reading	Conversion result when V_{IN} = V_{RH}	—	—	$FF	$FF	$FF	Hex
Sample acquisition time	Analogue input acquisition sampling time: E clock / Internal RC oscillator	— / —	12 / —	— / 12	— / 12	— / 12	t_{CYC} / µs
Sample/hold capacitance	Input capacitance (PE[0:7]) during sample	—	20 (typ)	—	—	—	pF
Input leakage	Input leakage on A/D pins: PE[0:7] / V_{RL}, V_{RH}	— / —	— / —	400 / 1.0	400 / 1.0	400 / 1.0	nA / µA

(1) For f_{OP} < 2 MHz, source impedances should be approximately 10 kΩ. For f_{OP} ≥ 2 MHz, source impedances should be in the range 5–10 kΩ. Source impedances greater than 10 kΩ have an adverse affect on A/D accuracy, because of input leakage.

(2) Performance verified down to ΔV_R = 2.5 V, however accuracy is tested and guaranteed at ΔV_R = 5 V ± 10%.

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12.5.3　Serial peripheral interface timing

$(V_{DD} = 5.0 \text{ Vdc} \pm 10\%, V_{SS} = 0 \text{ Vdc}, T_A = T_L \text{ to } T_H)$

Num	Characteristic [1]		Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
	Operating frequency	Master	$f_{OP(M)}$	0	0.5	0	0.5	0	0.5	f_{OP}
		Slave	$f_{OP(S)}$	0	2.0	0	3.0	0	4.0	MHz
1	Cycle time	Master	$t_{CYC(M)}$	2.0	—	2.0	—	2.0	—	t_{CYC}
		Slave	$t_{CYC(S)}$	500	—	333	—	250	—	ns
2	Enable lead time [2]	Master	$t_{LEAD(M)}$	—	—	—	—	—	—	ns
		Slave	$t_{LEAD(S)}$	250	—	240	—	200	—	
3	Enable lag time [2]	Master	$t_{LAG(M)}$	—	—	—	—	—	—	ns
		Slave	$t_{LAG(S)}$	250	—	240	—	200	—	
4	Clock (SCK) high time	Master	$t_{W(SCKH)M}$	340	—	227	—	130	—	ns
		Slave	$t_{W(SCKH)S}$	190	—	127	—	85	—	
5	Clock (SCK) low time	Master	$t_{W(SCKL)M}$	340	—	227	—	130	—	ns
		Slave	$t_{W(SCKL)S}$	190	—	127	—	85	—	
6	Input data set-up time	Master	$t_{SU(M)}$	100	—	100	—	100	—	ns
		Slave	$t_{SU(S)}$	100	—	100	—	100	—	
7	Input data hold time	Master	$t_{H(M)}$	100	—	100	—	100	—	ns
		Slave	$t_{H(S)}$	100	—	100	—	100	—	
8	Access time (from high-z to data active)	Slave	t_A	0	120	0	120	0	120	ns
9	Disable time (hold time to high-z state)	Slave	t_{DIS}	—	240	—	167	—	125	ns
10	Data valid (after enable edge) [3]		$t_{V(S)}$	—	240	—	167	—	125	ns
11	Output data hold time (after enable edge)		t_{HO}	0	—	0	—	0	—	ns
12	Rise time [3]									
	SPI outputs (SCK, MOSI and MISO)		t_{RM}	—	100	—	100	—	100	ns
	SPI inputs (SCK, MOSI, MISO and $\overline{SS}$)		t_{RS}	—	2.0	—	2.0	—	2.0	µs
13	Fall time [3]									
	SPI outputs (SCK, MOSI and MISO)		t_{FM}	—	100	—	100	—	100	ns
	SPI inputs (SCK, MOSI, MISO and $\overline{SS}$)		t_{FS}	—	2.0	—	2.0	—	2.0	µs

(1) All timing is given with respect to 20% and 70% of V_{DD}, unless otherwise noted.

(2) Signal production depends on software.
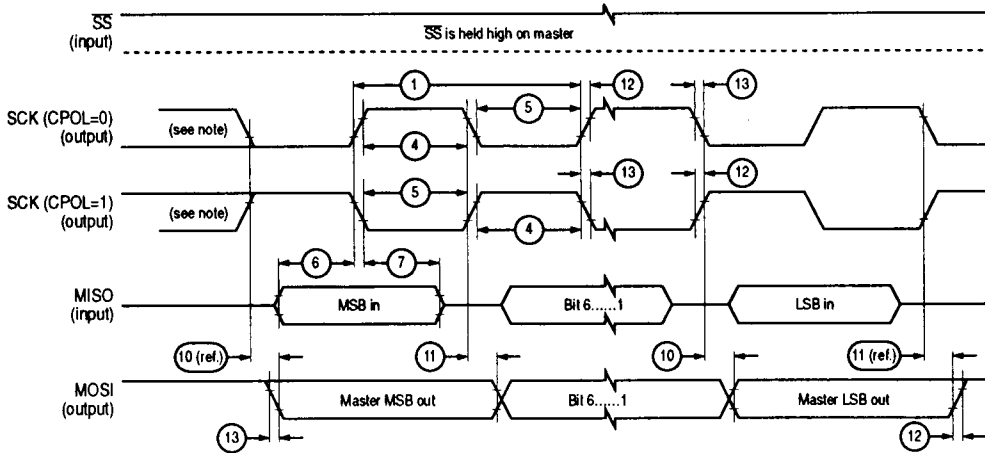
(3) Assumes 200 pF load on all SPI pins.

Note: This first clock edge is generated internally, but is not seen at the SCK pin.

Figure 12-9 SPI master timing (CPHA = 0)

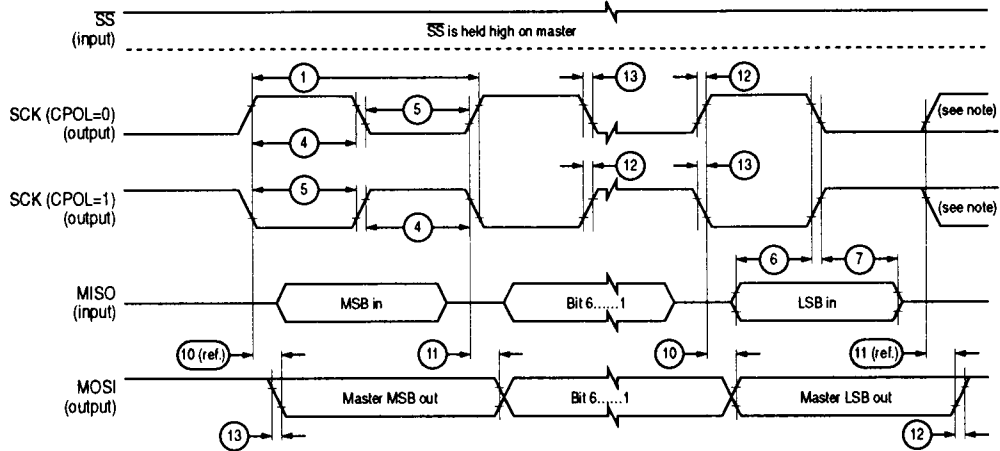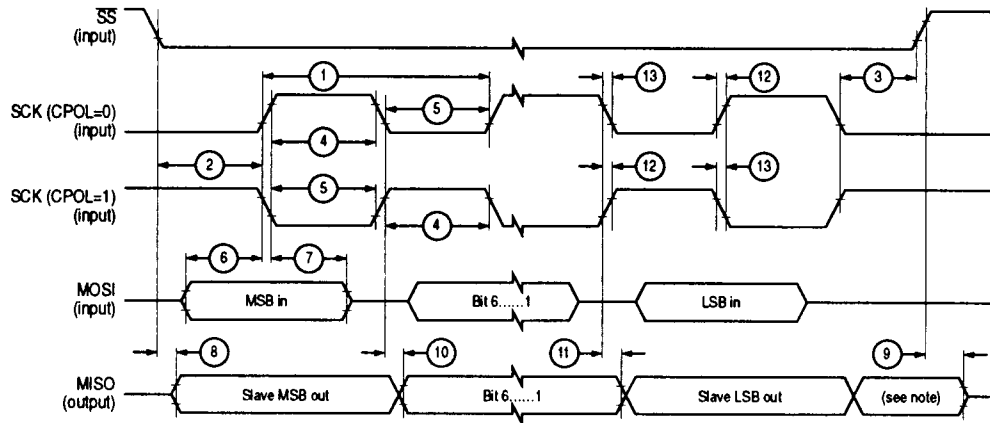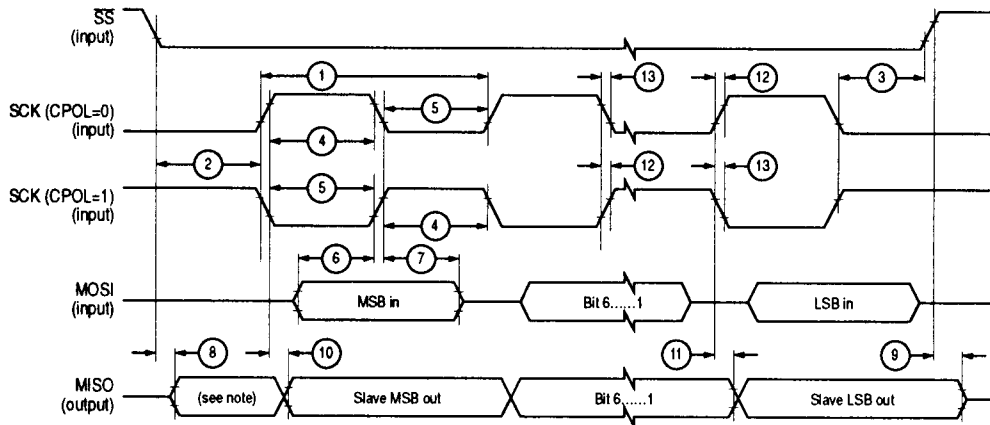Note: This last clock edge is generated internally, but is not seen at the SCK pin.

Figure 12-10 SPI master timing (CPHA = 1)

Note: Not defined, but normally the MSB of character just received.

Figure 12-11 SPI slave timing (CPHA = 0)

Note: Not defined, but normally the LSB of character last transmitted.

Figure 12-12 SPI slave timing (CPHA = 1)

12.5.4 Nonmultiplexed expansion bus timing

$(V_{DD} = 5.0\ Vdc \pm 10\%,\ V_{SS} = 0\ Vdc,\ T_A = T_L\ to\ T_H)$

Num	Characteristic [1]		Symbol	2.0 MHz		3.0 MHz		4.0 MHz		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
	Frequency of operation (E clock frequency)		f_{OP}	0	2.0	0	3.0	0	4.0	MHz
1	E clock period		t_{CYC}	500	—	333	—	250	—	ns
2	Pulse width, E low [2], [3]		PW_{EL}	230	—	147	—	105	—	ns
3	Pulse width, E high [2], [3]		PW_{EH}	225	—	142	—	100	—	ns
4A	E clock	rise time	t_r	—	20	—	20	—	20	ns
4B		fall time	t_f	—	20	—	18	—	15	
9	Address hold time [3]		t_{AH}	53	—	32	—	21	—	ns
11	Address delay time [3]		t_{AD}	—	103	—	82	—	71	ns
12	Address valid to E rise time [3]		t_{AV}	127	—	65	—	34	—	ns
17	Read data set-up time		t_{DSR}	30	—	30	—	20	—	ns
18	Read data hold time		t_{DHR}	0	—	0	—	0	—	ns
19	Write data delay time		t_{DDW}	—	40	—	40	—	40	ns
21	Write data hold time [3]		t_{DHW}	63	—	42	—	31	—	ns
29	MPU address access time [3]		t_{ACCA}	347	—	203	—	144	—	ns
39	Write data set-up time [3]		t_{DSW}	185	—	102	—	60	—	ns
57	Address valid to data tristate time		t_{AVDZ}	—	10	—	10	—	10	ns

(1) All timing is given with respect to 20% and 70% of V_{DD}, unless otherwise noted.

(2) Input clock duty cycles other than 50% will affect the bus performance.

(3) For $f_{OP} \leq 2\,MHz$ the following formulae may be used to calculate parameter values:

$PW_{EL} = t_{CYC}/2 - 20\,ns$ $PW_{EH} = t_{CYC}/2 - 25\,ns$

$t_{AH} = t_{CYC}/8 - 10\,ns$ $t_{AD} = t_{CYC}/8 + 40\,ns$

$t_{AV} = PW_{EL} - t_{AD}$ $t_{DHW} = t_{CYC}/8$

$t_{ACCA} = t_{CYC} - t_f - t_{DSR} - t_{AD}$ $t_{DSW} = PW_{EH} - t_{DDW}$

$t_{ECSA} = PW_{EH} - t_{ECSD} - t_{DSR}$ $t_{ACSD} = t_{CYC}/4 + 40\,ns$
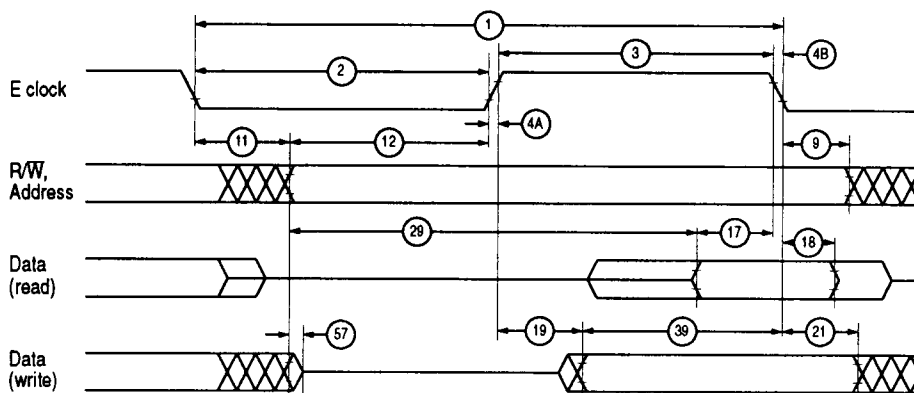
$t_{ACSA} = t_{CYC} - t_f - t_{DSR} - t_{ACSD}$

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Figure 12-13 Expansion bus timing

12.5.5 EEPROM characteristics

Characteristic	Temperature range			Unit
	–40 to +85°C	–40 to +105°C	–40 to +125°C	
Programming time [1]				
< 1 MHz, RCO enabled	10	15	20	
1–2 MHz, RCO disabled	20	must use RCO	must use RCO	ms
≥2 MHz & whenever RCO enabled	10	15	20	
Erase time: byte, row and bulk [1]	10	10	10	ms
Write/erase endurance [2]	10 000	10 000	10 000	cycles
Data retention [2]	10	10	10	years

(1) The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E clock frequency is less than 1.0 MHz.

(2) Refer to the current issue of Motorola's quarterly *Reliability Monitor Report* for the latest failure rate information.

12.5.6 *EPROM characteristics*

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted)

Characteristic	Symbol	Typ.	Unit
Programming voltage	V_{PPE}	12.25	V
Programming time	t_{EPROG}	4	ms