PCA9670

Remote 8-bit I/O expander for Fm+ I²C-bus with reset

1. General description

The PCA9670 provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus) and is a part of the Fast-mode Plus family.

The PCA9670 is a drop-in upgrade for the PCF8574 providing higher Fast-mode Plus (Fm+) I²C-bus speeds (1 MHz versus 400 kHz) so that the output can support PWM dimming of LEDs, higher I²C-bus drive (30 mA versus 3 mA) so that many more devices can be on the bus without the need for bus buffers, higher total package sink capacity (200 mA versus 100 mA) that supports having all 25 mA LEDs on at the same time and more device addresses (64 versus 8) are available to allow many more devices on the bus without address conflicts.

The difference between the PCA9670 and the PCF8574 is that the interrupt output on the PCF8574 is replaced by a $\overline{RESET}$ input on the PCA9670.

The devices consist of an 8-bit quasi-bidirectional port and an I²C-bus interface. The PCA9670 have low current consumption and include latched outputs with 25 mA high current drive capability for directly driving LEDs.

The internal Power-On Reset (POR), hardware reset pin ($\overline{RESET}$), or software reset sequence initializes the I/Os as inputs.

2. Features

- 1 MHz I²C-bus interface
- Compliant with the I²C-bus Fast and Standard modes
- SDA with 30 mA sink capability for 4000 pF buses
- 2.3 V to 5.5 V operation with 5.5 V tolerant I/Os
- 8-bit remote I/O pins that default to inputs at power-up
- Latched outputs with 25 mA sink capability for directly driving LEDs
- Total package sink capability of 200 mA
- Active LOW reset input
- 64 programmable slave addresses using 3 address pins
- Readable device ID (manufacturer, device type, and revision)
- Low standby current
- −40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA
- Packages offered: SO16, TSSOP16, HVQFN16

PHILIPS

3. Applications

- ■ LED signs and displays
- ■ Servers
- ■ Industrial control
- ■ Medical equipment
- ■ PLCs
- ■ Cellular telephones
- ■ Gaming machines
- ■ Instrumentation and test measurement

4. Ordering information

Table 1. Ordering information

| Type number	Topside mark	Package		Version
		Name	**Description**	
PCA9670BS	9670	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9670D	PCA9670D	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9670PW	9670	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Block diagram
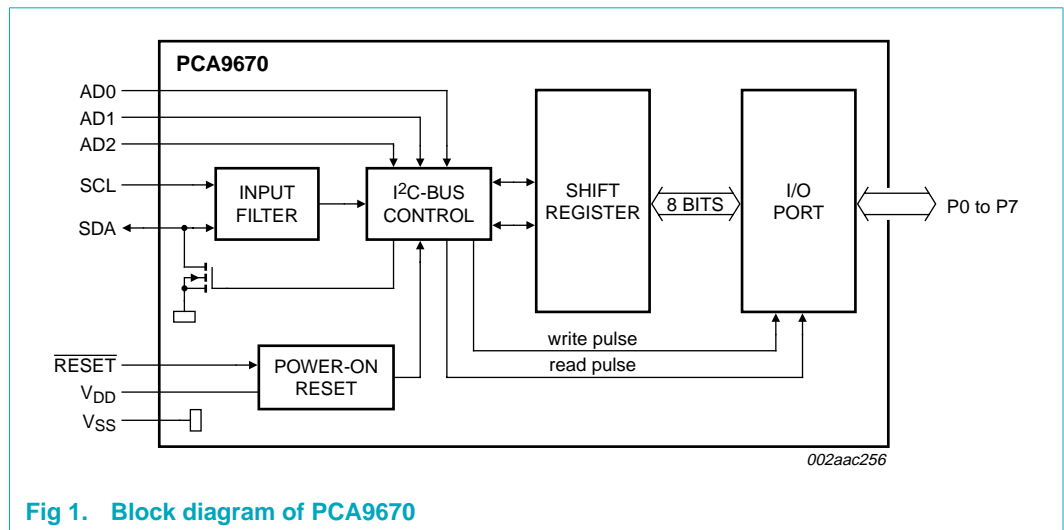
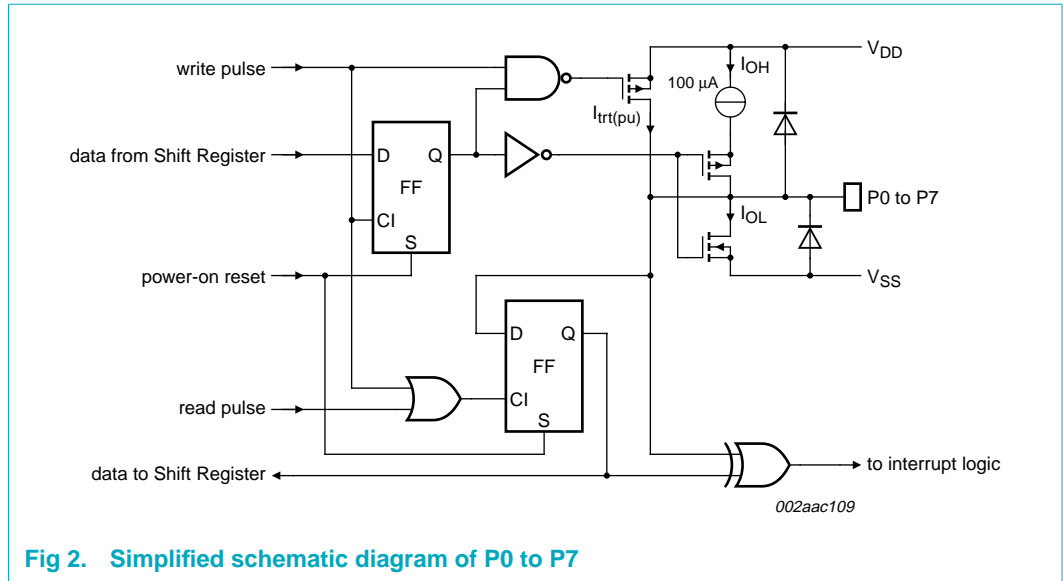

Fig 1. Block diagram of PCA9670

Fig 2. Simplified schematic diagram of P0 to P7

6. Pinning information

6.1 Pinning

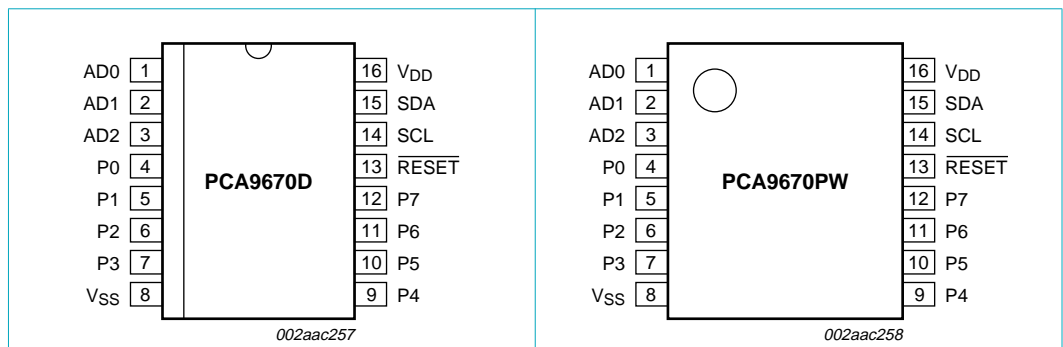

Fig 3. Pin configuration for SO16
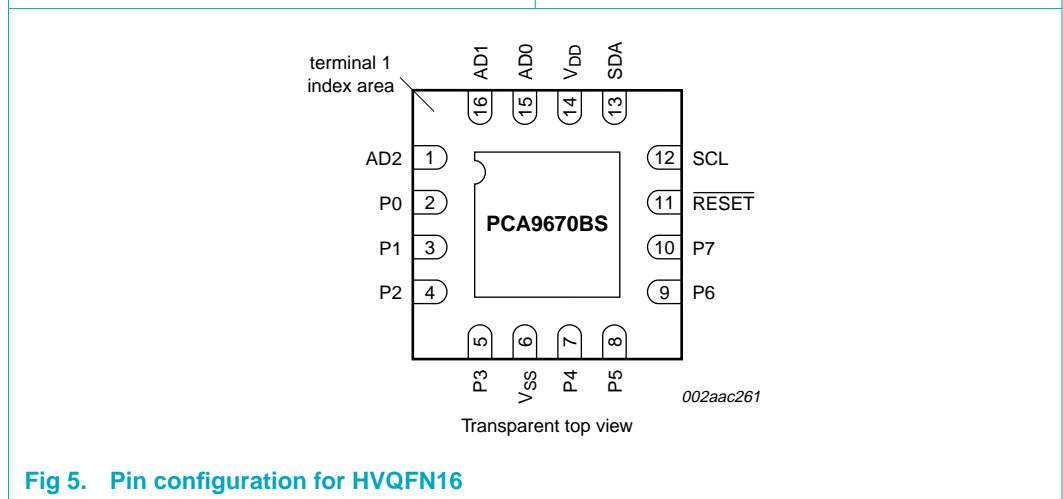

Fig 4. Pin configuration for TSSOP16

Transparent top view

Fig 5. Pin configuration for HVQFN16

6.2 Pin description

Table 2. **Pin description**

Symbol	Pin		Description
	SO16, TSSOP16	**HVQFN16**	
AD0	1	15	address input 0
AD1	2	16	address input 1
AD2	3	1	address input 2
P0	4	2	quasi-bidirectional I/O 0
P1	5	3	quasi-bidirectional I/O 1
P2	6	4	quasi-bidirectional I/O 2
P3	7	5	quasi-bidirectional I/O 3
V_{SS}	8	6[1]	supply ground
P4	9	7	quasi-bidirectional I/O 4
P5	10	8	quasi-bidirectional I/O 5
P6	11	9	quasi-bidirectional I/O 6
P7	12	10	quasi-bidirectional I/O 7
$\overline{RESET}$	13	11	reset input (active LOW)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V_{DD}	16	14	supply voltage

[1] HVQFN package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to Figure 1 "Block diagram of PCA9670".

7.1 Device address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9670 is shown in Figure 6. Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1, and AD0. Address values depending on AD2, AD1, and AD0 can be found in Table 3 "PCA9670 address map".

Remark: When using the PCA9670, reserved I²C-bus addresses must be used with caution since they can interfere with:

- "reserved for future use" I²C-bus addresses (0000 011, 1111 101, 1111 110, 1111 111)
- slave devices that use the 10-bit addressing scheme (1111 0xx)
- High speed mode (Hs-mode) master code (0000 1xx)

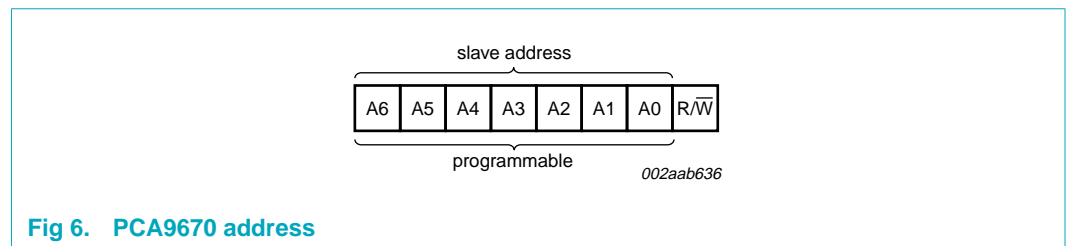| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ |

slave address

programmable

002aab636

Fig 6. PCA9670 address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

When AD2, AD1 and AD0 are held to V_{DD} or V_{SS}, the same address as the PCF8574 is applied.

7.1.1 Address maps

Table 3.   PCA9670 address map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
V_{SS}	SCL	V_{SS}	0	0	1	0	0	0	0	20h
V_{SS}	SCL	V_{DD}	0	0	1	0	0	0	1	22h
V_{SS}	SDA	V_{SS}	0	0	1	0	0	1	0	24h
V_{SS}	SDA	V_{DD}	0	0	1	0	0	1	1	26h
V_{DD}	SCL	V_{SS}	0	0	1	0	1	0	0	28h
V_{DD}	SCL	V_{DD}	0	0	1	0	1	0	1	2Ah
V_{DD}	SDA	V_{SS}	0	0	1	0	1	1	0	2Ch
V_{DD}	SDA	V_{DD}	0	0	1	0	1	1	1	2Eh
V_{SS}	SCL	SCL	0	0	1	1	0	0	0	30h
V_{SS}	SCL	SDA	0	0	1	1	0	0	1	32h
V_{SS}	SDA	SCL	0	0	1	1	0	1	0	34h
V_{SS}	SDA	SDA	0	0	1	1	0	1	1	36h
V_{DD}	SCL	SCL	0	0	1	1	1	0	0	38h
V_{DD}	SCL	SDA	0	0	1	1	1	0	1	3Ah
V_{DD}	SDA	SCL	0	0	1	1	1	1	0	3Ch
V_{DD}	SDA	SDA	0	0	1	1	1	1	1	3Eh
V_{SS}	V_{SS}	V_{SS}	0	1	0	0	0	0	0	40h
V_{SS}	V_{SS}	V_{DD}	0	1	0	0	0	0	1	42h
V_{SS}	V_{DD}	V_{SS}	0	1	0	0	0	1	0	44h
V_{SS}	V_{DD}	V_{DD}	0	1	0	0	0	1	1	46h
V_{DD}	V_{SS}	V_{SS}	0	1	0	0	1	0	0	48h
V_{DD}	V_{SS}	V_{DD}	0	1	0	0	1	0	1	4Ah
V_{DD}	V_{DD}	V_{SS}	0	1	0	0	1	1	0	4Ch
V_{DD}	V_{DD}	V_{DD}	0	1	0	0	1	1	1	4Eh
V_{SS}	V_{SS}	SCL	0	1	0	1	0	0	0	50h
V_{SS}	V_{SS}	SDA	0	1	0	1	0	0	1	52h
V_{SS}	V_{DD}	SCL	0	1	0	1	0	1	0	54h
V_{SS}	V_{DD}	SDA	0	1	0	1	0	1	1	56h
V_{DD}	V_{SS}	SCL	0	1	0	1	1	0	0	58h
V_{DD}	V_{SS}	SDA	0	1	0	1	1	0	1	5Ah
V_{DD}	V_{DD}	SCL	0	1	0	1	1	1	0	5Ch
V_{DD}	V_{DD}	SDA	0	1	0	1	1	1	1	5Eh

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Table 3. **PCA9670 address map** …*continued*

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
SCL	SCL	V_{SS}	1	0	1	0	0	0	0	A0h
SCL	SCL	V_{DD}	1	0	1	0	0	0	1	A2h
SCL	SDA	V_{SS}	1	0	1	0	0	1	0	A4h
SCL	SDA	V_{DD}	1	0	1	0	0	1	1	A6h
SDA	SCL	V_{SS}	1	0	1	0	1	0	0	A8h
SDA	SCL	V_{DD}	1	0	1	0	1	0	1	AAh
SDA	SDA	V_{SS}	1	0	1	0	1	1	0	ACh
SDA	SDA	V_{DD}	1	0	1	0	1	1	1	AEh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh
SCL	V_{SS}	V_{SS}	1	1	0	0	0	0	0	C0h
SCL	V_{SS}	V_{DD}	1	1	0	0	0	0	1	C2h
SCL	V_{DD}	V_{SS}	1	1	0	0	0	1	0	C4h
SCL	V_{DD}	V_{DD}	1	1	0	0	0	1	1	C6h
SDA	V_{SS}	V_{SS}	1	1	0	0	1	0	0	C8h
SDA	V_{SS}	V_{DD}	1	1	0	0	1	0	1	CAh
SDA	V_{DD}	V_{SS}	1	1	0	0	1	1	0	CCh
SDA	V_{DD}	V_{DD}	1	1	0	0	1	1	1	CEh
SCL	V_{SS}	SCL	1	1	1	0	0	0	0	E0h
SCL	V_{SS}	SDA	1	1	1	0	0	0	1	E2h
SCL	V_{DD}	SCL	1	1	1	0	0	1	0	E4h
SCL	V_{DD}	SDA	1	1	1	0	0	1	1	E6h
SDA	V_{SS}	SCL	1	1	1	0	1	0	0	E8h
SDA	V_{SS}	SDA	1	1	1	0	1	0	1	EAh
SDA	V_{DD}	SCL	1	1	1	0	1	1	0	ECh
SDA	V_{DD}	SDA	1	1	1	0	1	1	1	EEh

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7.2 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the PCA9670.

- General Call address: allows to reset the PCA9670 through the I²C-bus upon reception of the right I²C-bus sequence. See Section 7.2.1 "Software Reset" for more information.

- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See Section 7.2.2 "Device ID (PCA9670 ID field)" for more information.
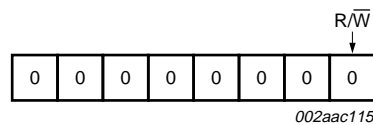
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	R/$\overline{W}$
0 0 0 0 0 0 0 0	

002aac115

Fig 7. General Call address

1 1 1 1 1 0 0 R/$\overline{W}$

002aac116
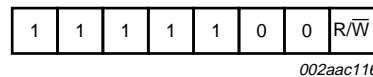
Fig 8. Device ID address

7.2.1 Software Reset

The Software Reset Call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I²C-bus master.

2. The reserved General Call I²C-bus address '0000 000' with the R/$\overline{W}$ bit set to 0 (write) is sent by the I²C-bus master.

3. The PCA9670 device(s) acknowledge(s) after seeing the General Call address '0000 0000' (00h) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I²C-bus master.

4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.

   a. The PCA9670 acknowledges this value only. If the byte is not equal to 06h, the PCA9670 does not acknowledge it.

   If more than 1 byte of data is sent, the PCA9670 does not acknowledge any more.

5. Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the PCA9670 then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I^{2}C-bus master must interpret a non-acknowledge from the PCA9670 (at any time) as a 'Software Reset Abort'. The PCA9670 does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in Figure 9.

Fig 9.   Software Reset sequence
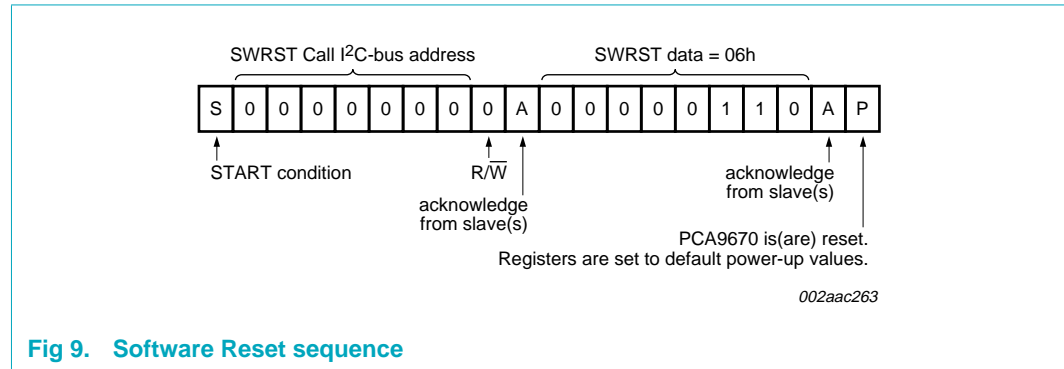
7.2.2 Device ID (PCA9670 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 8 bits with the manufacturer name, unique per manufacturer (for example, Philips).

- 13 bits with the part identification, assigned by manufacturer, the 7 MSBs with the category ID and the 6 LSBs with the feature ID (for example, for example PCA9670 16-bit quasi-output I/O expander).

- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command

2. The master sends the Reserved Device ID I^{2}C-bus address '1111 100' with the R/$\overline{\text{W}}$ bit set to 0 (write).

3. The master sends the I^{2}C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I^{2}C-bus slave address).

4. The master sends a Re-START command.

   Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed.

   Remark: A STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID read cannot be performed.

5. The master sends the Reserved Device ID I^{2}C-bus address '1111 100' with the R/$\overline{\text{W}}$ bit set to 1 (read).

6. The device ID read can be done, starting with the 8 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 13 part identification bits and then the 3 die revision bits (3 LSB of the third byte).

7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

   Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

Remark: If the master continues to ACK the bytes after the third byte, the PCA9670 rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

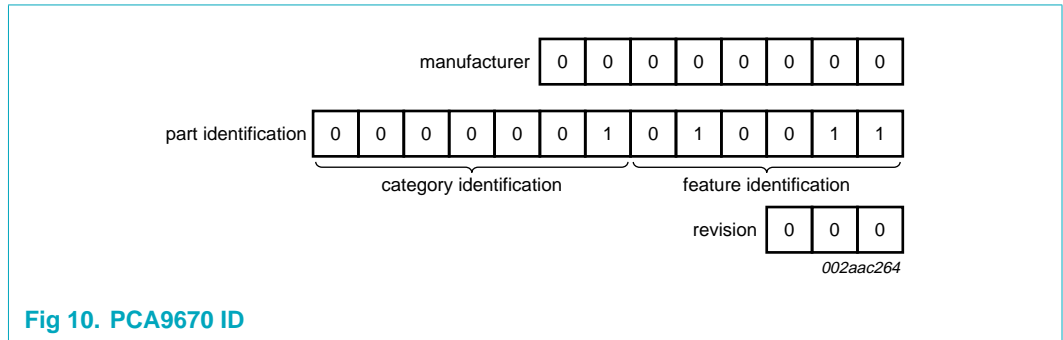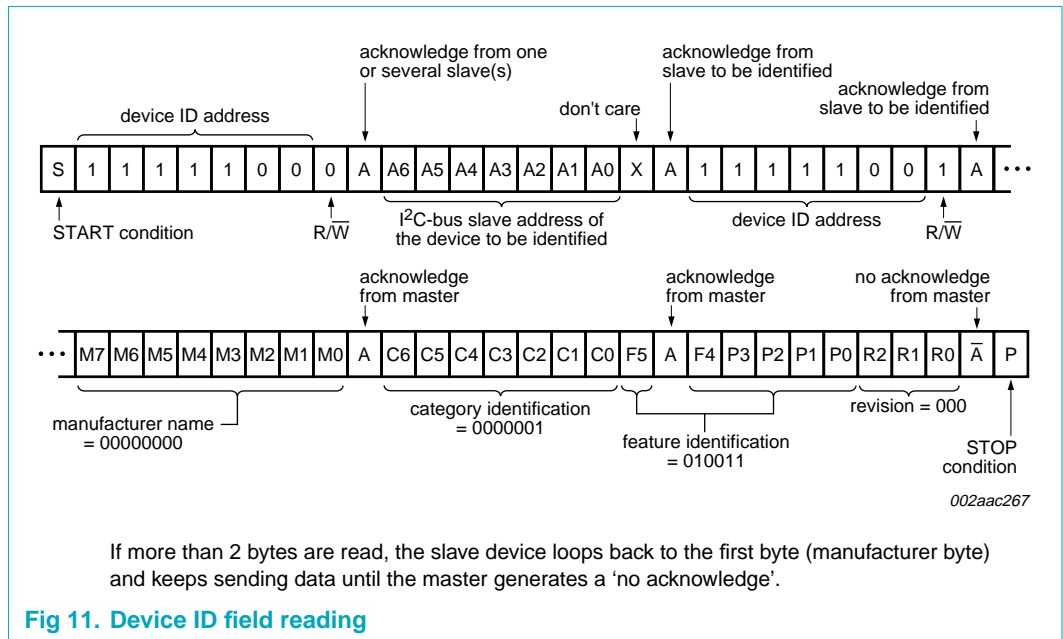For the PCA9670, the Device ID is as shown in Figure 10.

Fig 10. PCA9670 ID

If more than 2 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 11. Device ID field reading

8. I/O programming

8.1 Quasi-bidirectional I/O architecture

The PCA9670's 8 ports (see Figure 2) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the Read mode (see Figure 13). Output data is transmitted to the ports in the Write mode (see Figure 12).

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data directions. At power-on the I/Os are HIGH. In this mode only a current source (I_{OH}) to V_{DD} is active. An additional strong pull-up to V_{DD} ($I_{trt(pu)}$) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on, as all the I/Os are set HIGH, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode.

Remark: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current (I_{OL}) will flow to V_{SS}.

8.2 Writing to the port (Output mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the write mode is entered. The PCA9670 acknowledges and the master sends the data byte for P7 to P0 and is acknowledged by the PCA9670. The 8-bit data is presented on the port lines after it has been acknowledged by the PCA9670.

The number of data bytes that can be sent successively is not limited. The previous data is overwritten every time a data byte has been sent.
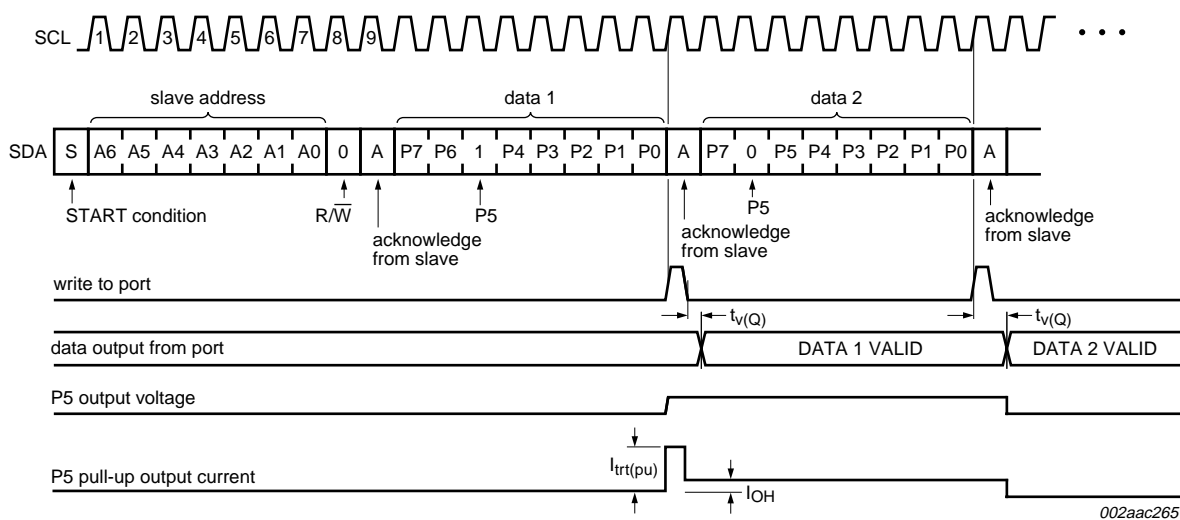

Fig 12. Write mode (output)

8.3 Reading from a port (Input mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the Read mode is entered. The data bytes that follow on the SDA are the values on the ports.

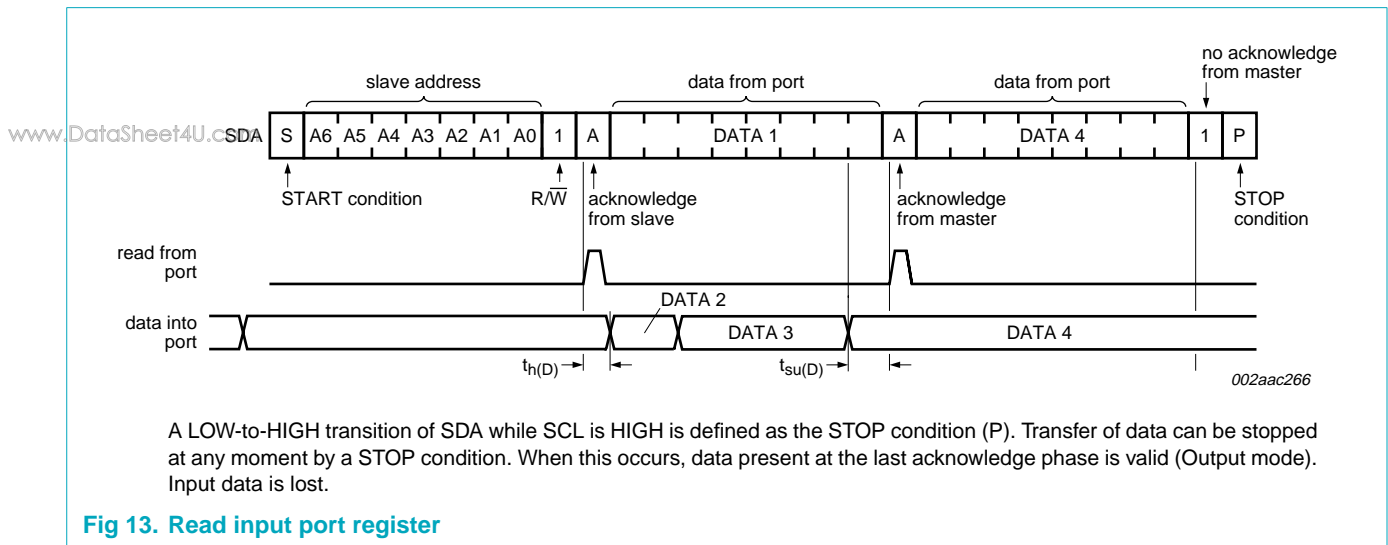If the data on the input port changes faster than the master can read, this data may be lost.

A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the last acknowledge phase is valid (Output mode). Input data is lost.

Fig 13. Read input port register

8.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9670 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9670 registers and I²C-bus/SMBus state machine will initialize to their default states. Thereafter V_{DD} must be lowered below 0.2 V to reset the device.

8.5 $\overline{RESET}$ input

A reset can be accomplished by holding the $\overline{RESET}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA9670 registers and I²C-bus state machine will be held in their default state until the $\overline{RESET}$ input is once again HIGH.

9. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 14).

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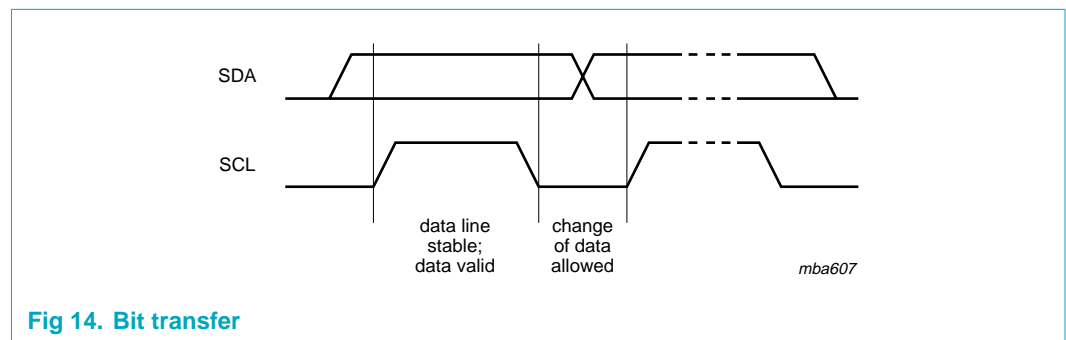
Fig 14. Bit transfer

9.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 15.)
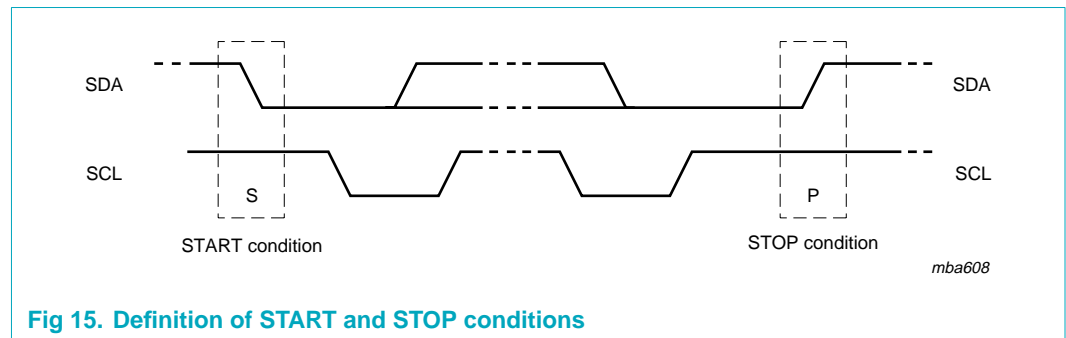

Fig 15. Definition of START and STOP conditions

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9.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 16).
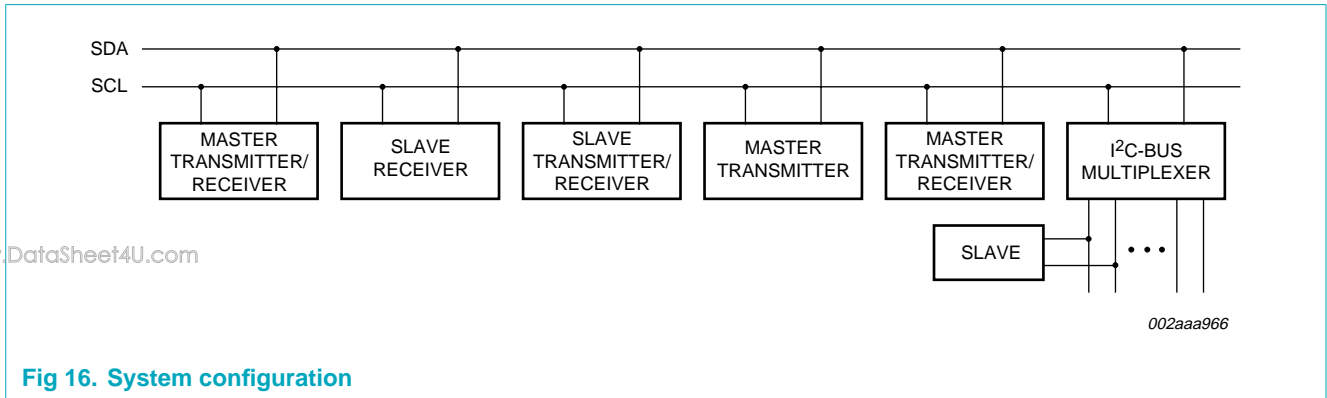
Fig 16. System configuration

9.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.
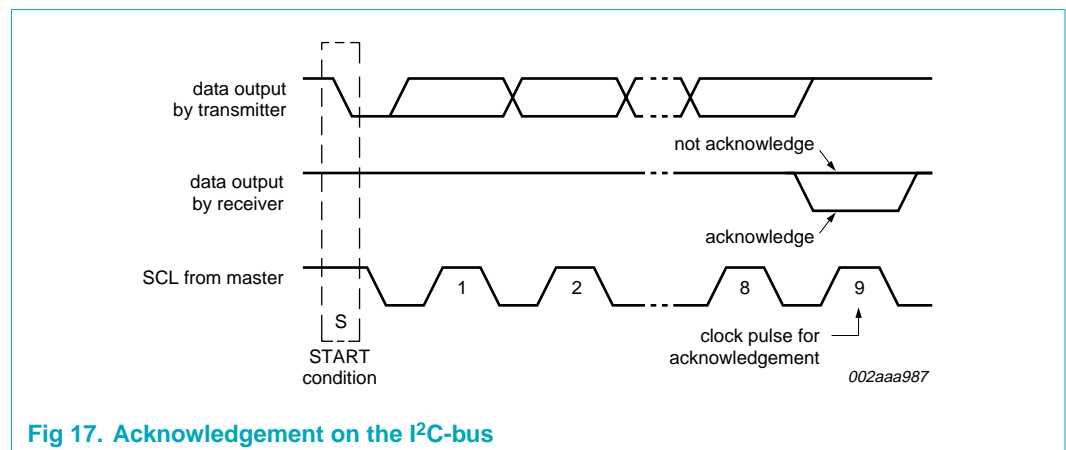
Fig 17. Acknowledgement on the I^{2}C-bus

10. Application design-in information

10.1 Bidirectional I/O expander applications

In the 8-bit I/O expander application shown in Figure 18, P0 and P1 are inputs, and P2 to P7 are outputs. When used in this configuration, during a write, the input (P0 and P1) must be written as HIGH so the external devices fully control the input ports. The desired HIGH or LOW logic levels may be written to the I/Os used as outputs (P2 to P7). During a read, the logic levels of the external devices driving the input ports (P0 and P1) and the previous written logic level to the output ports (P2 to P7) will be read.

The GPIO also has a reset line ($\overline{\text{RESET}}$) that can be connected to an output pin of the microprocessor. Since the device does not have an interrupt output, changes of the I/Os can be monitored by reading the input register. If both a $\overline{\text{RESET}}$ and $\overline{\text{INT}}$ are needed, use the PCA9671.
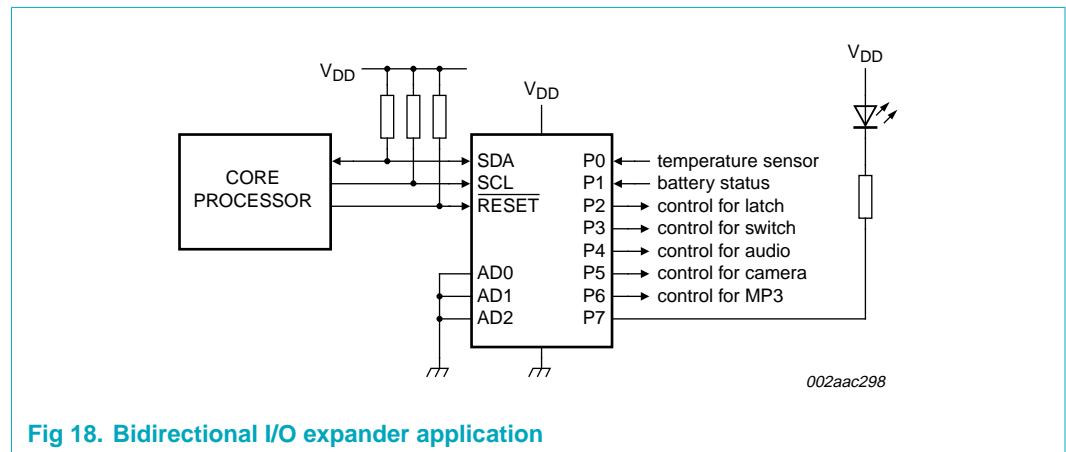
Fig 18. Bidirectional I/O expander application

10.2 High current-drive load applications

The GPIO has a maximum sinking current of 25 mA per bit. In applications requiring additional drive, two port pins in the same octal may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together. Up to 8 pins (one octal) can be connected together to drive 200 mA.
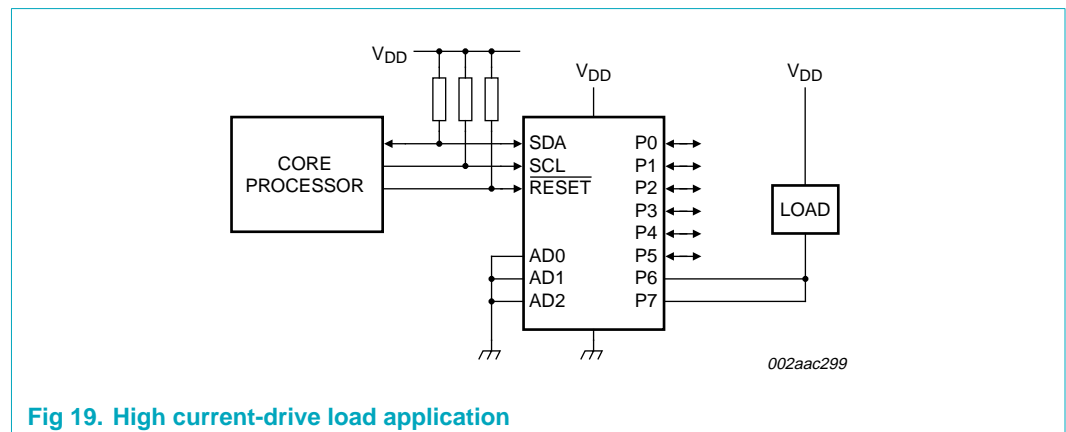

Fig 19. High current-drive load application

11. Limiting values

Table 4. **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6	V
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±400	mA
V_I	input voltage		$V_{SS} - 0.5$	5.5	V
I_I	input current		-	±20	mA
I_O	output current	[1]	-	±50	mA
P_{tot}	total power dissipation		-	400	mW
P/out	power dissipation per output		-	100	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C

[1] Total package (maximum) output current is 400 mA.

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12. Static characteristics

Table 5. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	Operating mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 1 MHz; AD0, AD1, AD2 = static H or L		-	100	200	µA
I_{stb}	standby current	Standby mode; no load; $V_I = V_{DD}$ or V_{SS}; f_{SCL} = 0 kHz		-	2.5	10	µA
V_{POR}	power-on reset voltage		[1]	-	1.8	2.0	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 2.3 V		20	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 3.0 V		25	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 4.5 V		30	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	5	10	pF
I/Os; P0 to P7							
I_{OL}	LOW-level output current[2]	V_{OL} = 0.5 V; V_{DD} = 2.3 V		12	\<tbd>	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V		17	\<tbd>	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V		25	\<tbd>	-	mA
$I_{OL(tot)}$	total LOW-level output current[2]	V_{OL} = 0.5 V; V_{DD} = 4.5 V		-	-	200	mA
I_{OH}	HIGH-level output current	$V_{OH} = V_{SS}$		−30	\<tbd>	−300	µA
$I_{trt(pu)}$	transient boosted pull-up current	$V_{OH} = V_{SS}$; see Figure 12		−0.5	−1.0	-	mA
C_i	input capacitance		[3]	-	\<tbd>	10	pF
C_o	output capacitance		[3]	-	\<tbd>	10	pF
Input RESET							
V_{IL}	LOW-level input voltage			−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA
I_{OH}	HIGH-level output current			−1	-	+1	µA
C_i	input capacitance			-	3	5	pF
Inputs AD0, AD1, AD2							
V_{IL}	LOW-level input voltage			−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current			−1	-	+1	µA
C_i	input capacitance			-	3.5	5	pF

[1] The power-on reset circuit resets the I^{2}C-bus logic with $V_{DD} < V_{POR}$ and set all I/Os to logic 1 (with current source to V_{DD}).

[2] Each bit must be limited to a maximum of 25 mA and the total package limited to 200 mA due to internal busing limits.

[3] The value is not tested, but verified on sampling basis.

13. Dynamic characteristics

Table 6.　　**Dynamic characteristics**

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Standard mode I2C-bus		Fast mode I2C-bus		Fast-mode Plus I2C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time[1]		0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time[2]		300	-	50	-	<tbd>	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[4][5]	-	300	20 + 0.1C_b[3]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	20 + 0.1C_b[3]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter[6]		-	50	-	50	-	<tbd>	ns
Port timing; C_L ≤ 100 pF (see Figure 13 and Figure 12)									
$t_{v(Q)}$	data output valid time		-	4	-	4	-	4	µs
$t_{su(D)}$	data input setup time		0	-	0	-	0	-	µs
$t_{h(D)}$	data input hold time		4	-	4	-	4	-	µs
Reset timing (see Figure 21)									
$t_{w(rst)}$	reset pulse width		4	-	4	-	4	-	µs
$t_{rec(rst)}$	reset recovery time		0	-	0	-	0	-	µs
t_{rst}	reset time		100	-	100	-	100	-	µs

[1]　$t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2]　$t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3]　C_b = total capacitance of one bus line in pF.

[4]　A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region SCL's falling edge.

[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

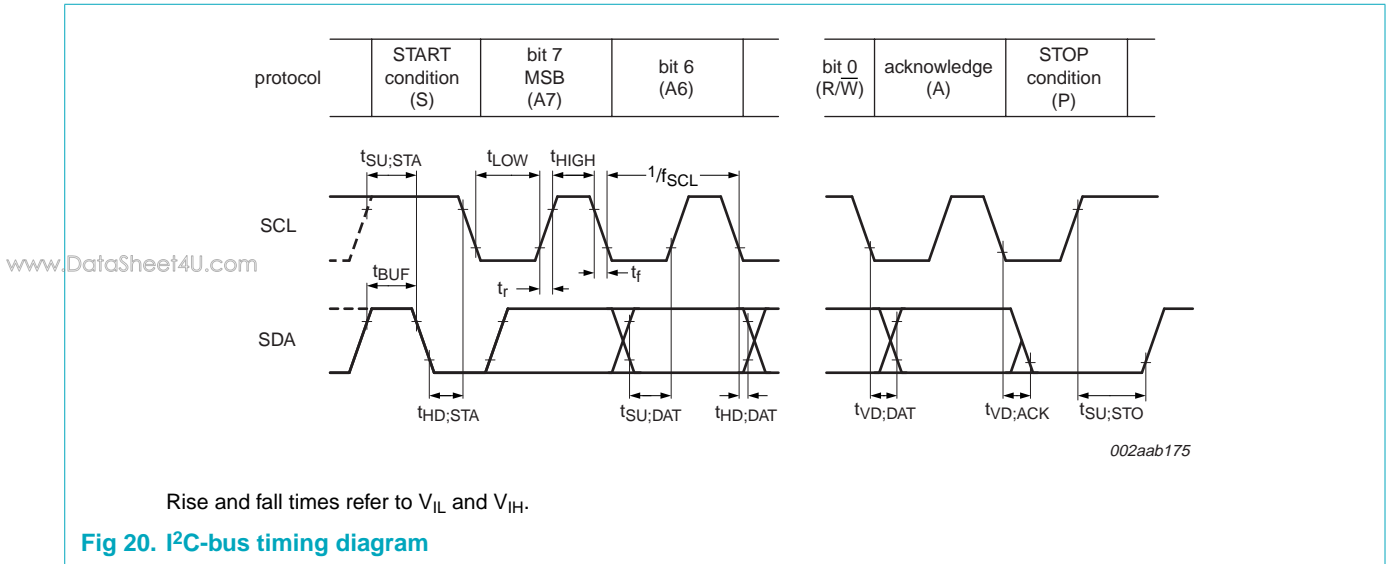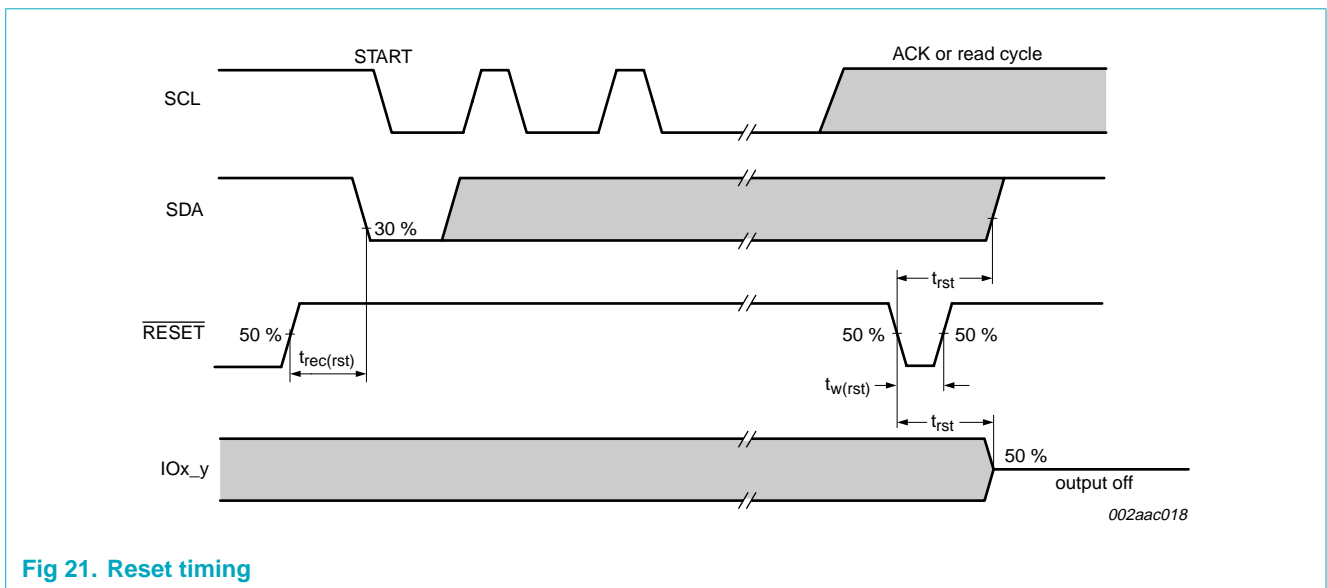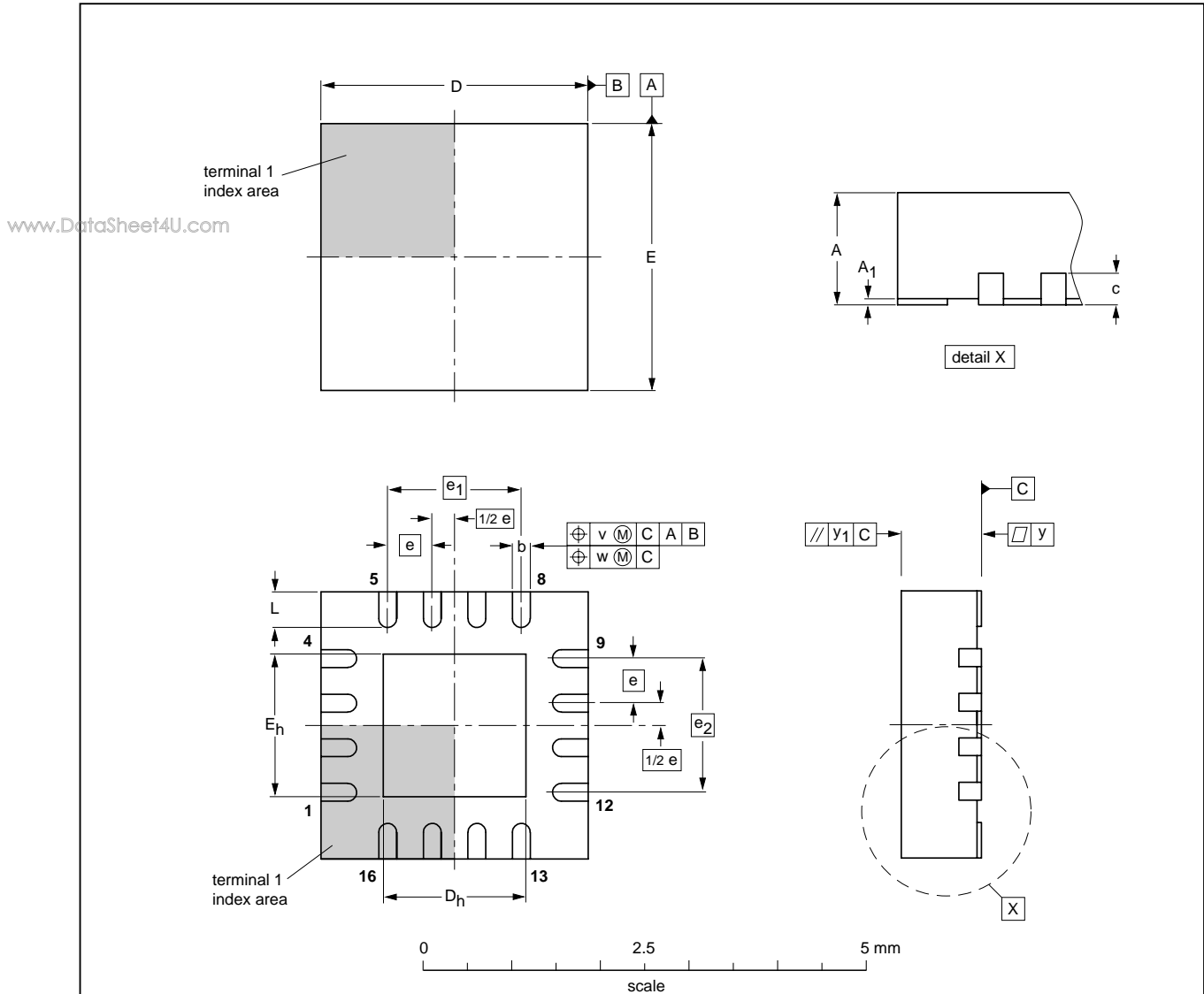[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

Rise and fall times refer to V_{IL} and V_{IH}.

Fig 20. I²C-bus timing diagram

Fig 21. Reset timing

14. Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads;
16 terminals; body 3 x 3 x 0.85 mm

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DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A₁	b	c	D(1)	Dₕ	E(1)	Eₕ	e	e₁	e₂	L	v	w	y	y₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			02-03-25 02-10-21

Fig 22. Package outline SOT758-1 (HVQFN16)

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SO16: plastic small outline package; 16 leads; body width 7.5 mm SOT162-1
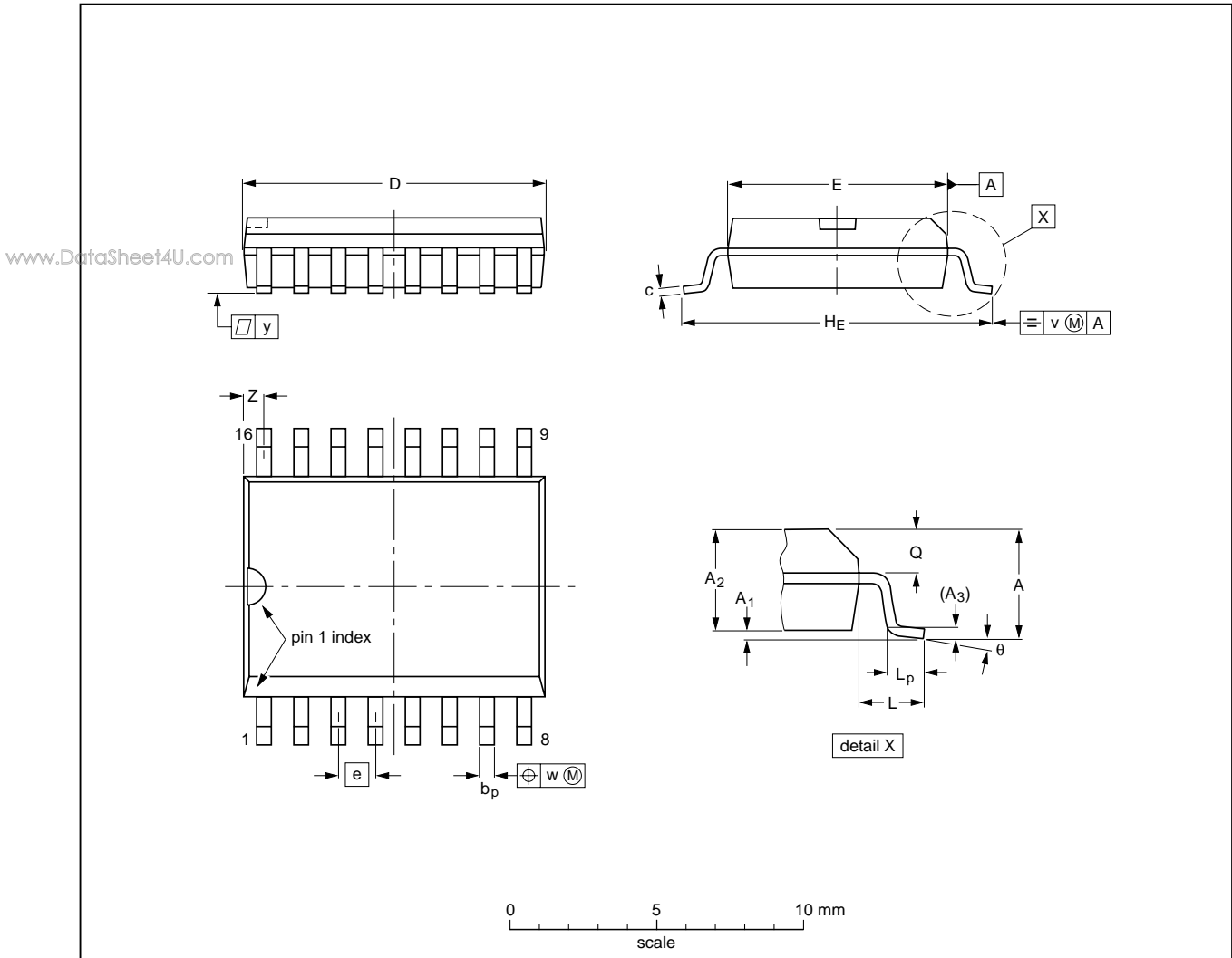
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

Fig 23. Package outline SOT162-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm   **SOT403-1**

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0   2.5   5 mm
scale
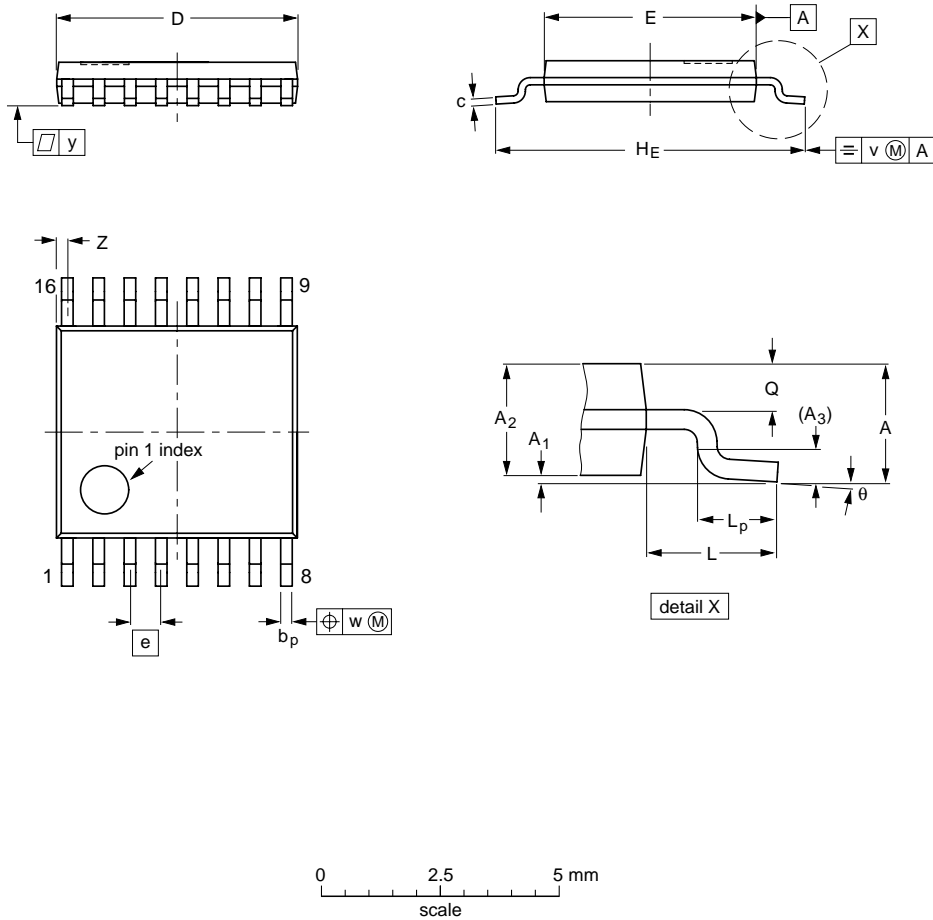
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D (1)	E (2)	e	HE	L	Lₚ	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 24. Package outline SOT403-1 (TSSOP16)

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15. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

16. Soldering

16.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 7.   SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 8.   Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

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To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

16.5 Package related soldering information

Table 9.   Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	**Reflow**[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

17. Abbreviations

Table 10.   Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
LED	Light Emitting Diode
IC	Integrated Circuit
I²C-bus	Inter IC bus
ID	Identification
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PLC	Programmable Logic Controller
RAID	Redundant Array of Independent Disks

18. Revision history

Table 11.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9670_1	20060620	Objective data sheet	-	-

PCA9670_1

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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21. Contents

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Date of release: 20 June 2006

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