

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# 2SJ549(L), 2SJ549(S)

Silicon P Channel MOS FET  
High Speed Power Switching

**RENESAS**

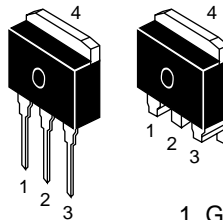
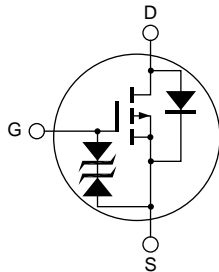
ADE-208-644A (Z)  
2nd. Edition  
Jul. 1998

## Features

- Low on-resistance  
 $R_{DS(on)} = 0.11 \Omega$  typ.
- Low drive current
- 4 V gate drive devices
- High speed switching

## Outline

LDBPAK



1. Gate
2. Drain
3. Source
4. Drain

## 2SJ549(L),2SJ549(S)

### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	-12	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-48	A
Body-drain diode reverse drain current	$I_{DR}$	-12	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	-12	A
Avalanche energy	$E_{AR}$ <sup>Note3</sup>	12	mJ
Channel dissipation	$Pch$ <sup>Note2</sup>	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

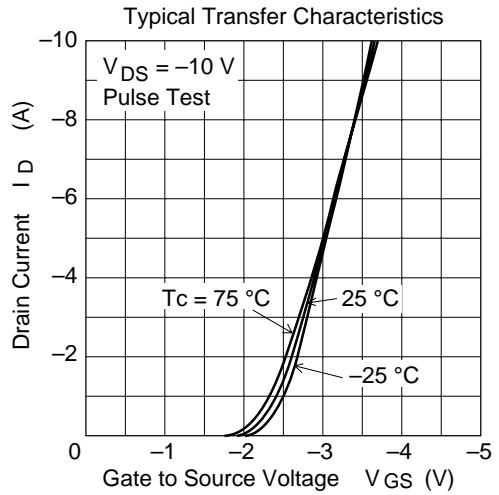
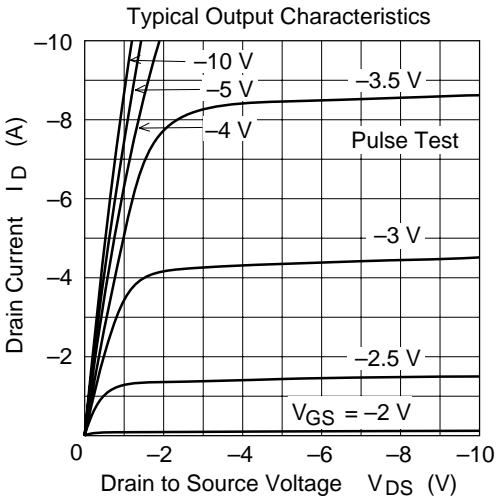
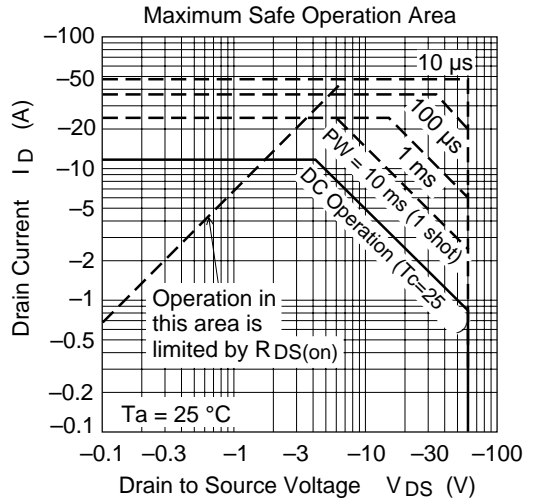
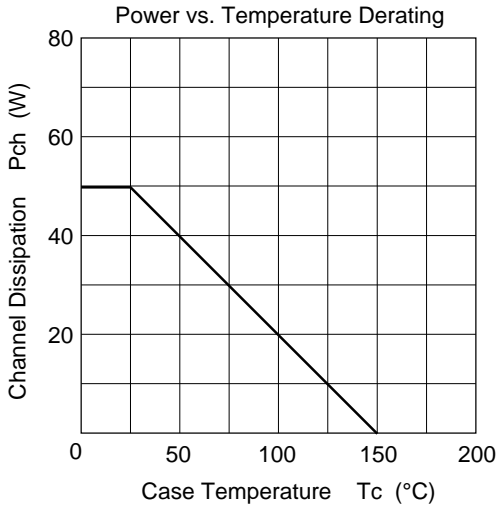
- Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$   
2. Value at  $T_c = 25^\circ C$   
3. Value at  $Tch = 25^\circ C$ ,  $R_g \geq 50 \Omega$

## Electrical Characteristics (Ta = 25°C)

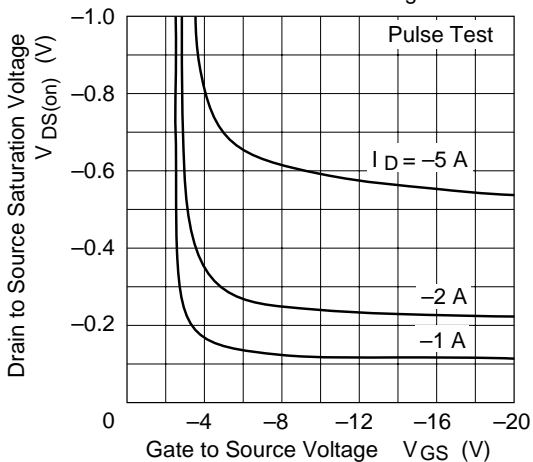
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100\mu\text{A}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-10	$\mu\text{A}$	$V_{DS} = -60\text{V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16\text{V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$ , $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.11	0.15	$\Omega$	$I_D = -6\text{A}$ , $V_{GS} = -10\text{V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.16	0.23	$\Omega$	$I_D = -6\text{A}$ , $V_{GS} = -4\text{V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	5	8	—	S	$I_D = -6\text{A}$ , $V_{DS} = -10\text{V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	580	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	$C_{oss}$	—	300	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	85	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$V_{GS} = -10\text{V}$ , $I_D = -6\text{A}$
Rise time	$t_r$	—	55	—	ns	$R_L = 6\Omega$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	$t_f$	—	60	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-1.2	—	V	$I_D = -12\text{A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = -12\text{A}$ , $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

Note: 4. Pulse test

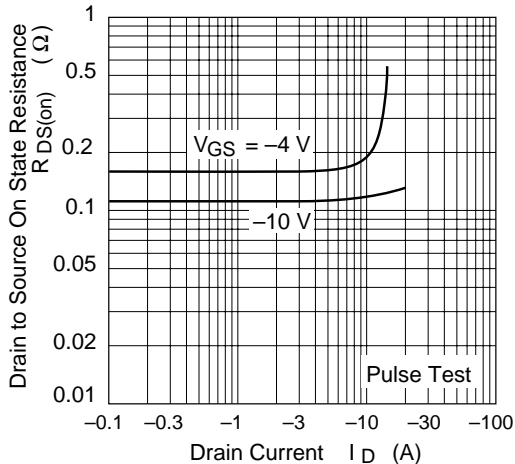
Main Characteristics



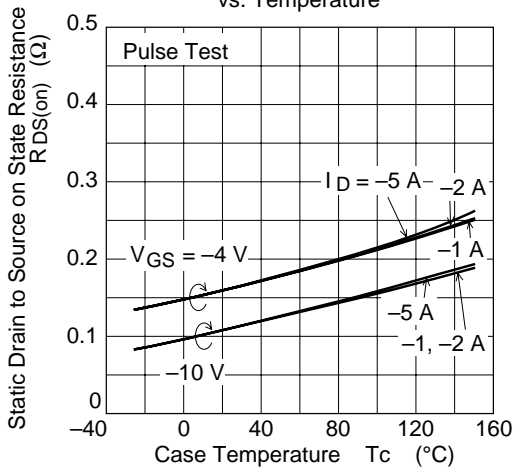
Drain to Source Saturation Voltage vs. Gate to Source Voltage



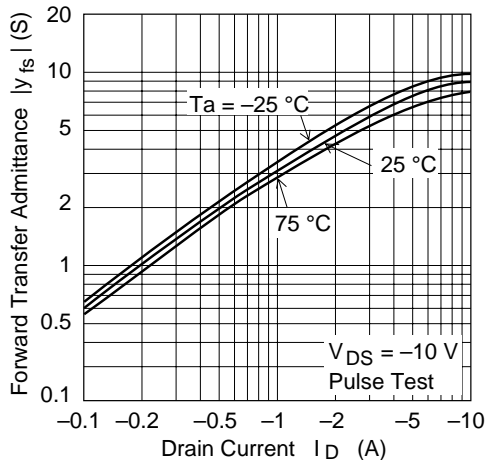
Static Drain to Source on State Resistance vs. Drain Current

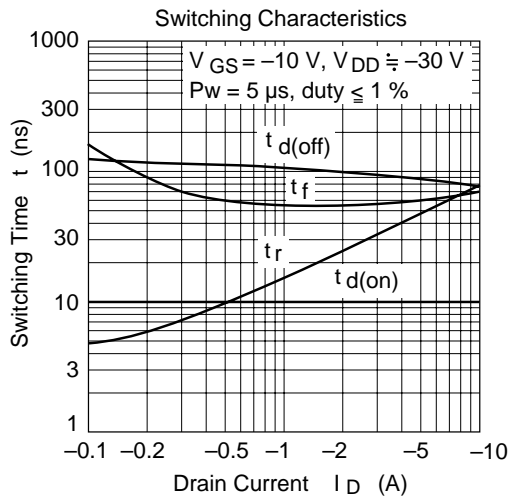
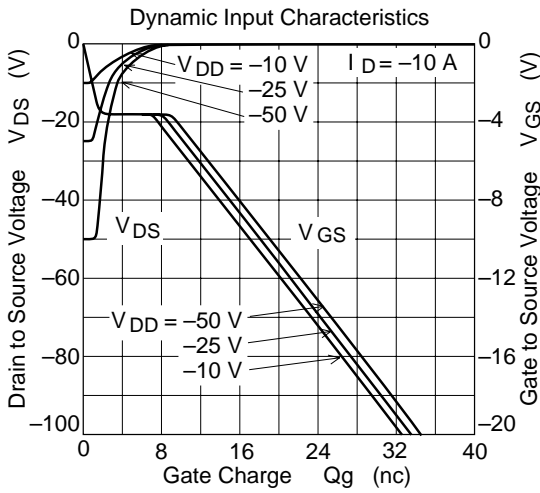
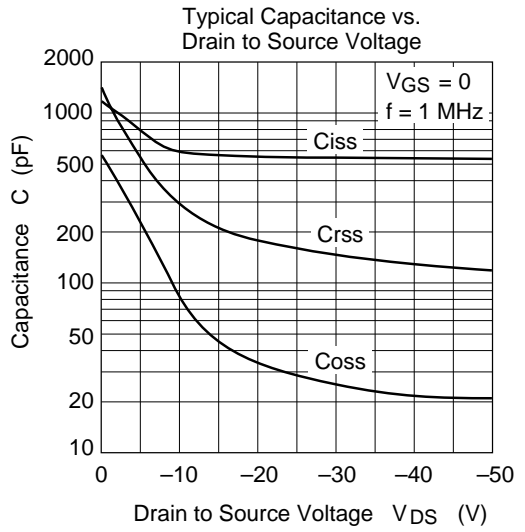
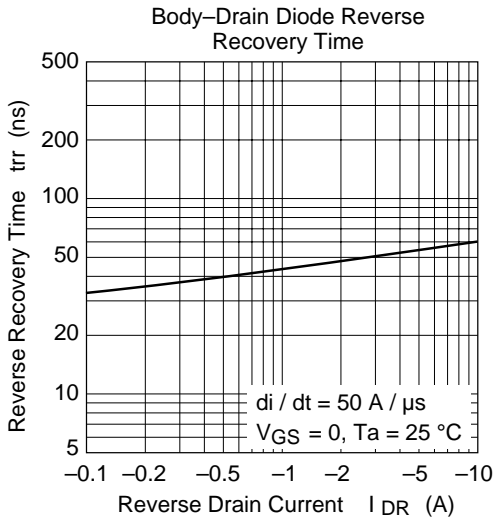


Static Drain to Source on State Resistance vs. Temperature



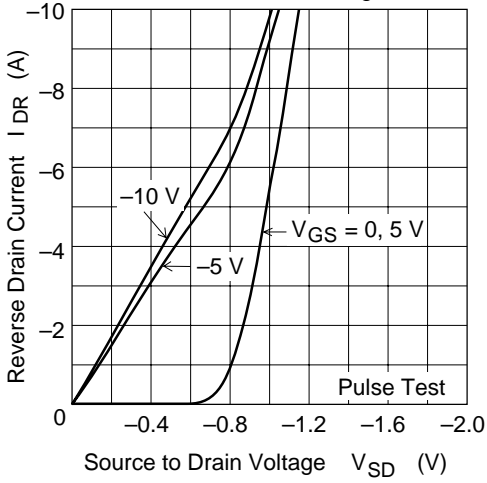
Forward Transfer Admittance vs. Drain Current



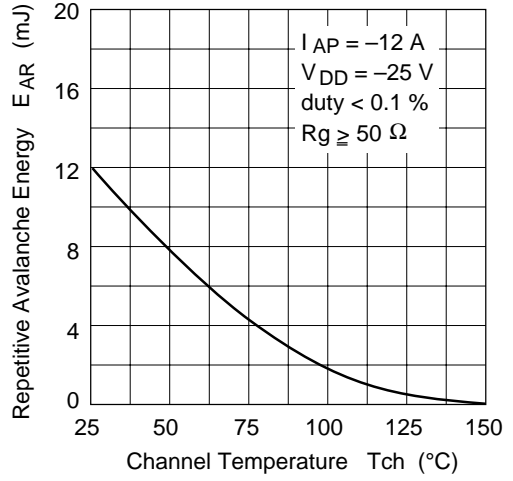




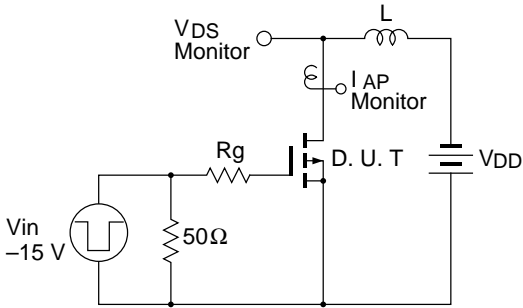
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

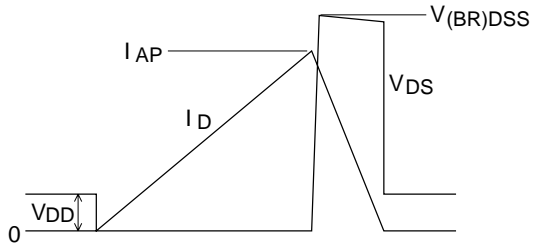


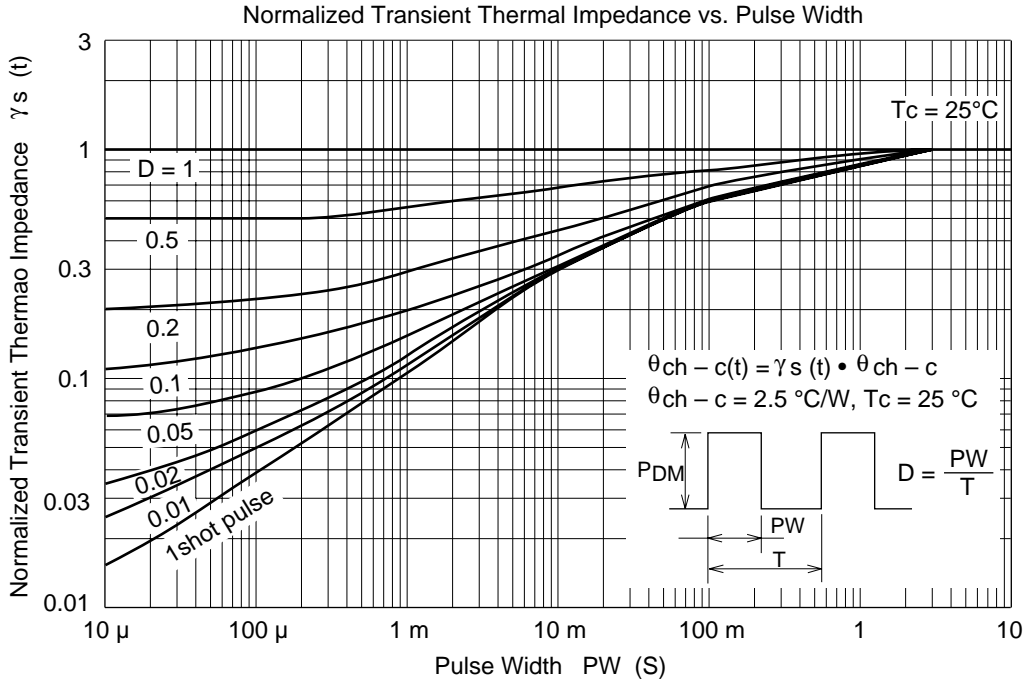
Avalanche Test Circuit



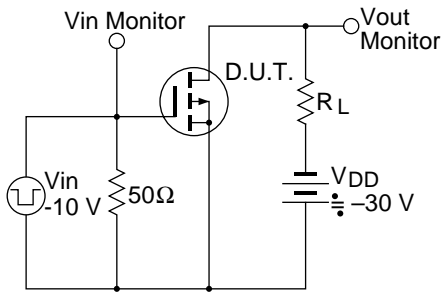
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

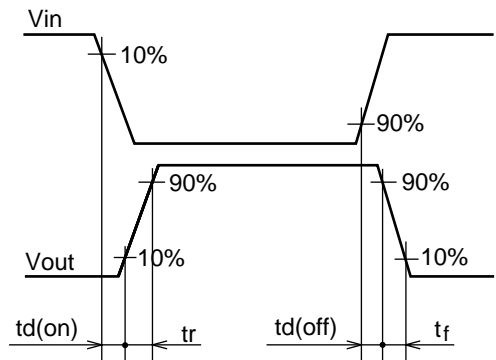




Switching Time Test Circuit

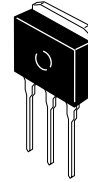
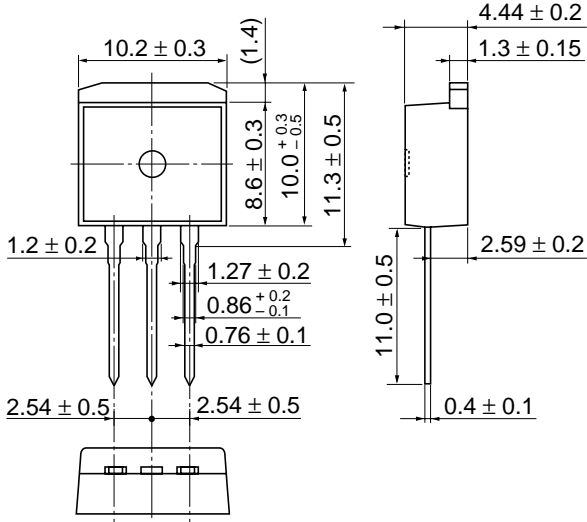


Waveform



Package Dimensions

As of January, 2001  
Unit: mm

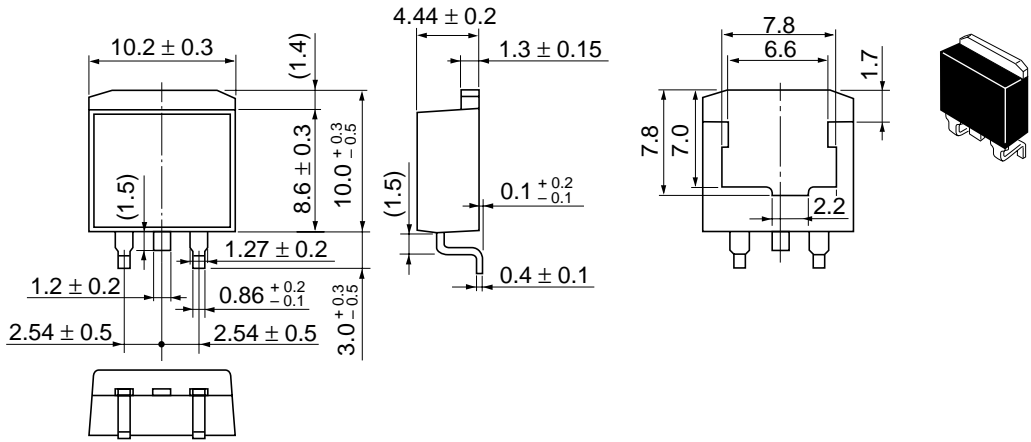


Hitachi Code	LDBAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

# 2SJ549(L),2SJ549(S)

As of January, 2001

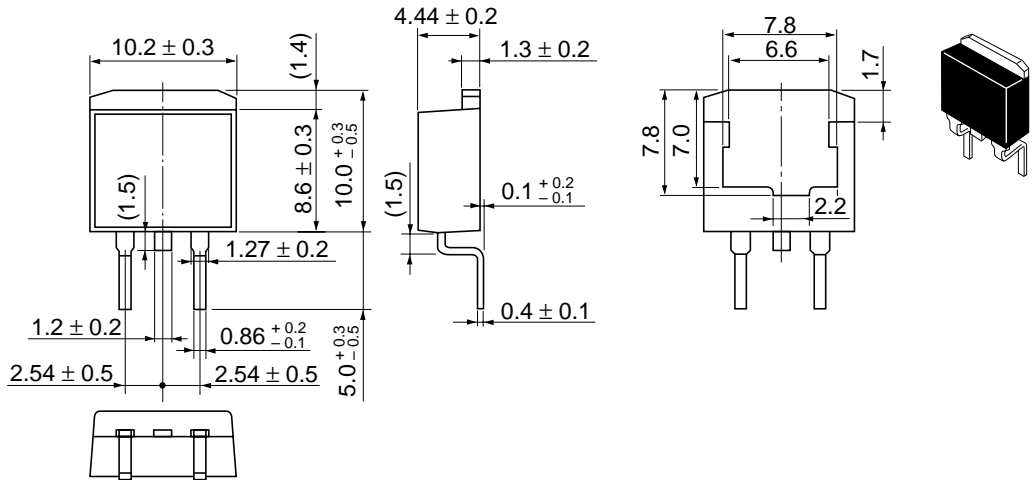
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

As of January, 2001

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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