

DATA SHEET

PDTC143X series

NPN resistor-equipped transistors;

R1 = 4.7 k Ω , R2 = 10 k Ω

Product specification
Supersedes data of 2004 Mar 23

2004 Aug 06

NPN resistor-equipped transistors; R1 = 4.7 k Ω , R2 = 10 k Ω

PDTC143X series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
R1	bias resistor	4.7	–	k Ω
R2	bias resistor	10	–	k Ω

DESCRIPTION

NPN resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC143XE	SOT416	SC-75	34	PDTA143XE
PDTC143XEF	SOT490	SC-89	54	PDTA143XEF
PDTC143XK	SOT346	SC-59	26	PDTA143XK
PDTC143XM	SOT883	SC-101	E2	PDTA143XM
PDTC143XS	SOT54 (TO-92)	SC-43	TC143X	PDTA143XS
PDTC143XT	SOT23	–	*32 ⁽¹⁾	PDTA143XT
PDTC143XU	SOT323	SC-70	*53 ⁽¹⁾	PDTA143XU

Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC143XS		1 2 3	base collector emitter
PDTC143XE PDTC143XEF PDTC143XK PDTC143XT PDTC143XU		1 2 3	base emitter collector
PDTC143XM		1 2 3	base emitter collector

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTC143XE	–	plastic surface mounted package; 3 leads	SOT416
PDTC143XEF	–	plastic surface mounted package; 3 leads	SOT490
PDTC143XK	–	plastic surface mounted package; 3 leads	SOT346
PDTC143XM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTC143XS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTC143XT	–	plastic surface mounted package; 3 leads	SOT23
PDTC143XU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	10	V
V_I	input voltage				
	positive		–	+20	V
	negative		–	–7	V
I_O	output current (DC)		–	100	mA
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT883	notes 2 and 3	–	250	mW
SOT490	notes 1 and 2	–	250	mW	
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$
T_{amb}	operating ambient temperature		–65	+150	$^\circ\text{C}$

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μm copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT883	notes 2 and 3	500	K/W
SOT490	notes 1 and 2	500	K/W	

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A	–	–	1	μ A
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C	–	–	50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A	–	–	600	μ A
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 10 mA	50	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA	–	–	100	mV
V _{i(off)}	input-off voltage	I _C = 100 μ A; V _{CE} = 5 V	–	–	0.3	V
V _{i(on)}	input-on voltage	I _C = 20 mA; V _{CE} = 0.3 V	2.5	–	–	V
R1	input resistor		3.3	4.7	6.1	k Ω
$\frac{R2}{R1}$	resistor ratio		1.7	2.1	2.6	
C _c	collector capacitance	I _E = i _e = 0 A; V _{CB} = 10 V; f = 1 MHz	–	–	2.5	pF

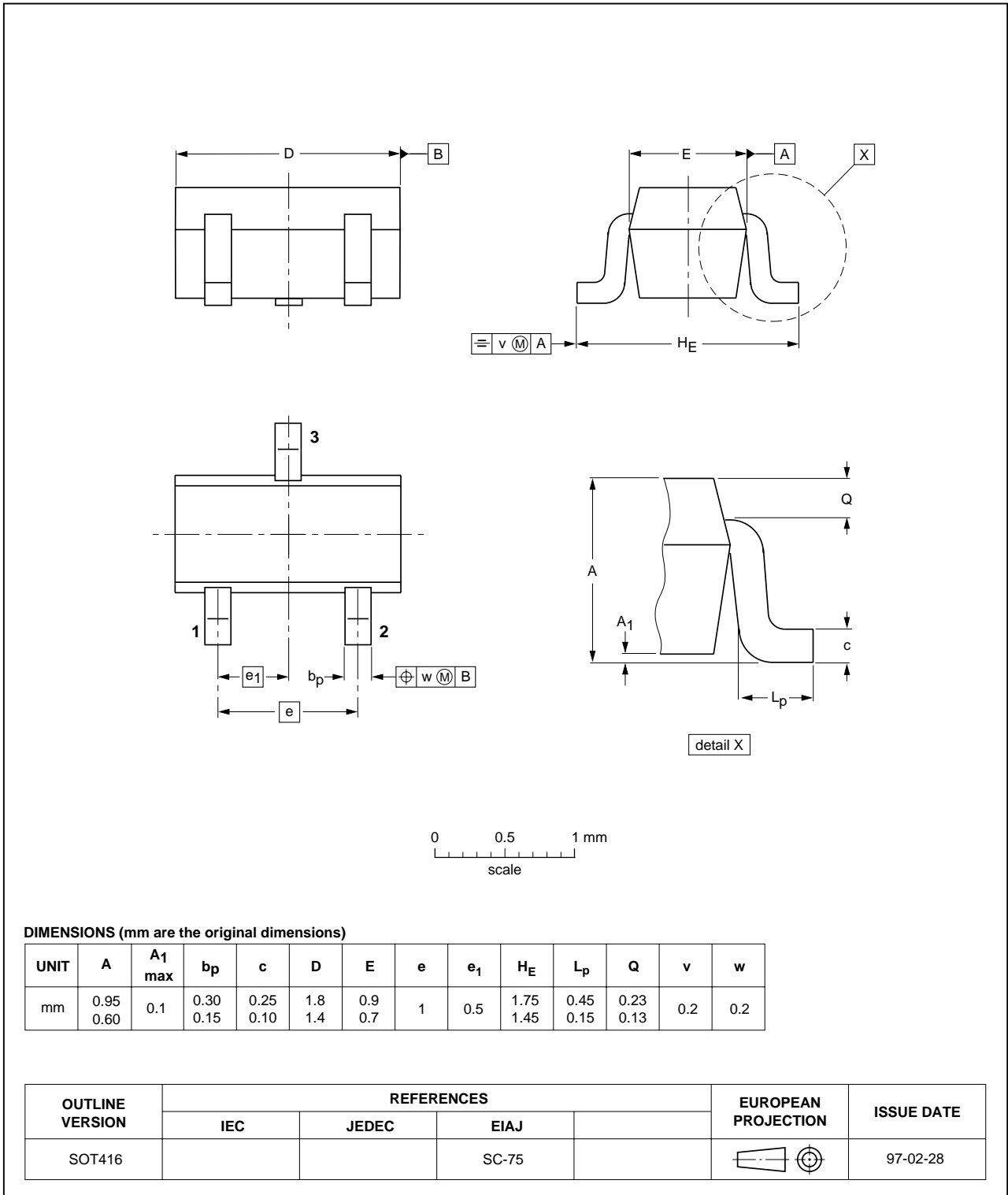
NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 10 kΩ

PDTC143X series

PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT416

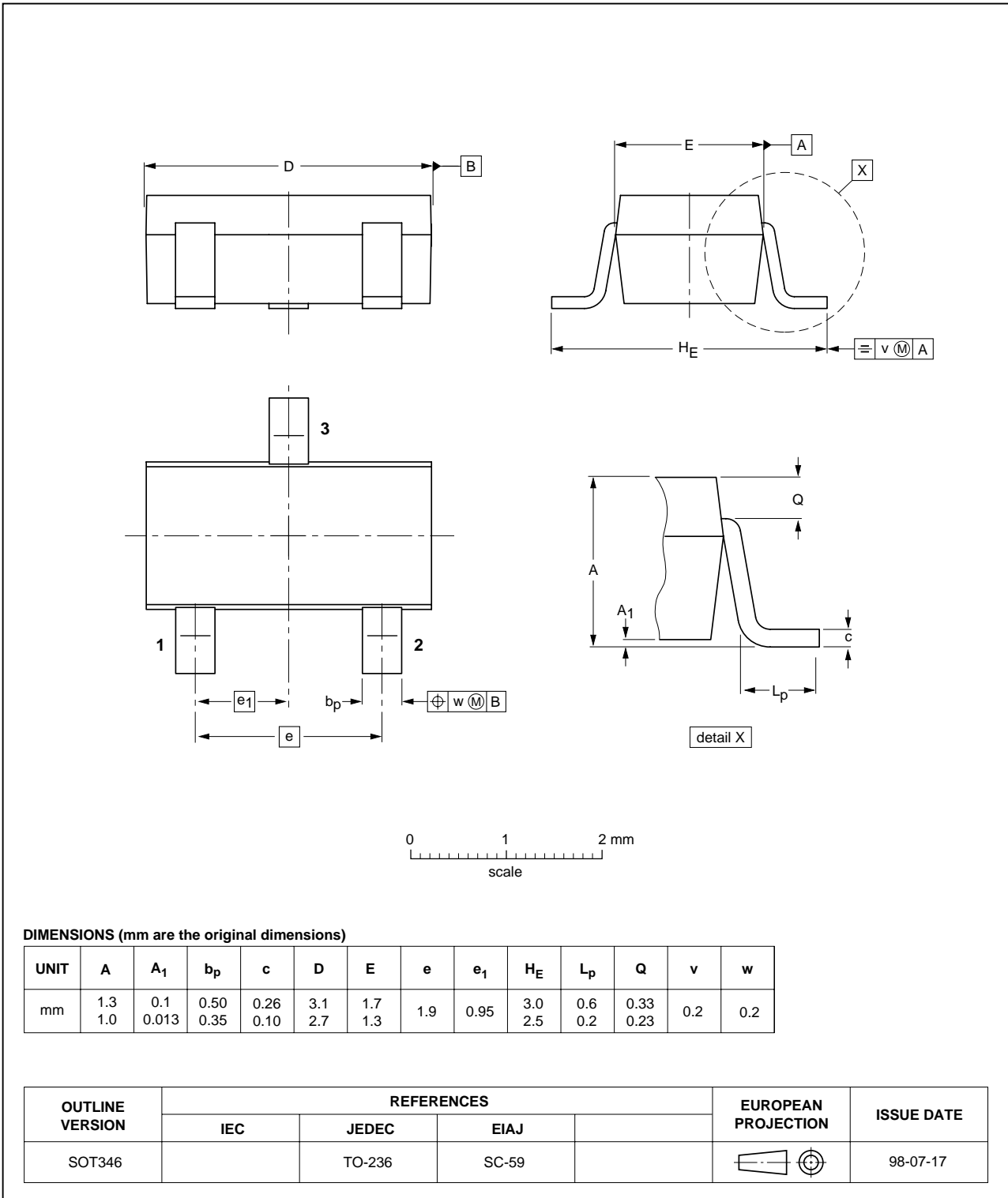


NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 10 kΩ

PDTC143X series

Plastic surface mounted package; 3 leads

SOT346

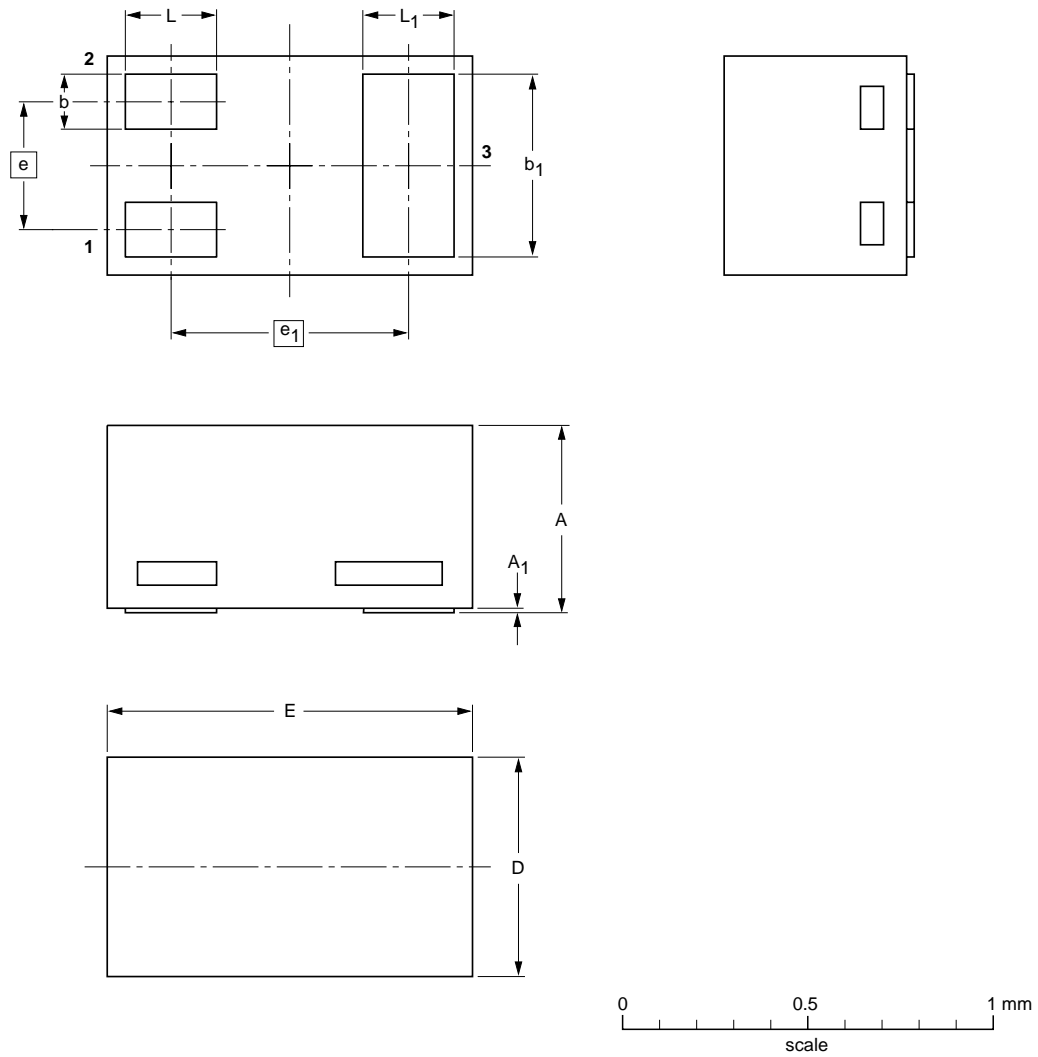


NPN resistor-equipped transistors;
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PDTC143X series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

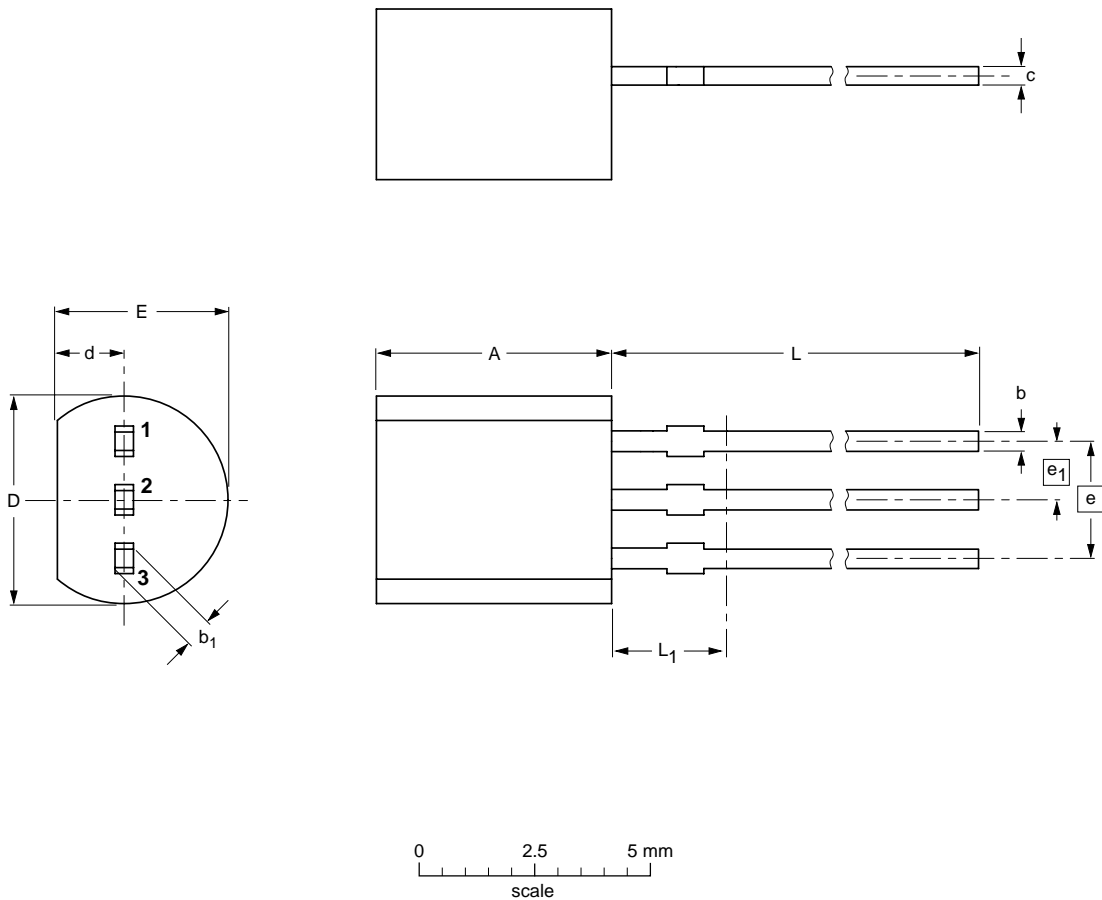
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT883			SC-101		03-02-05 03-04-03

NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 10 kΩ

PDTC143X series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

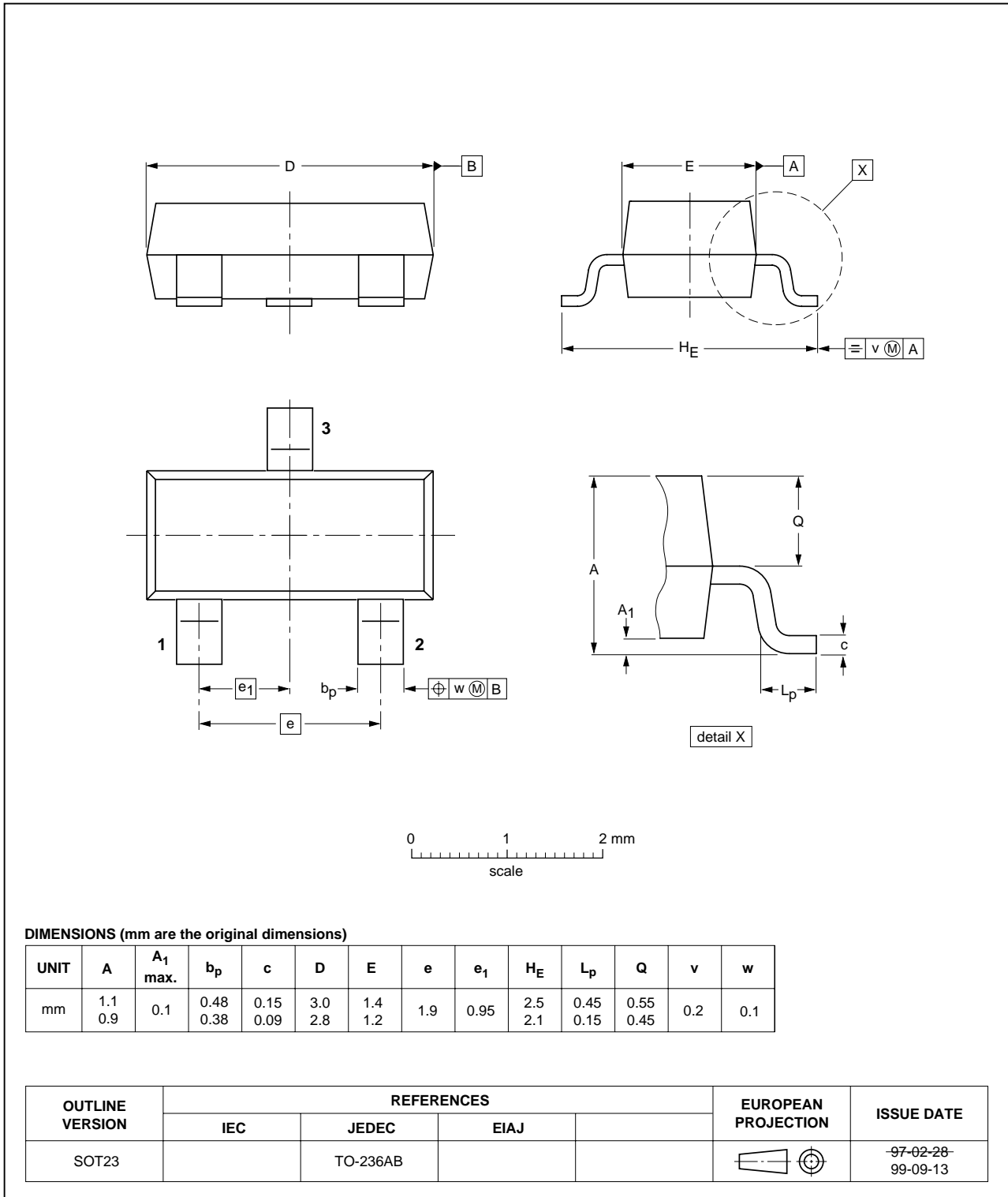
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

NPN resistor-equipped transistors;
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PDTC143X series

Plastic surface mounted package; 3 leads

SOT23

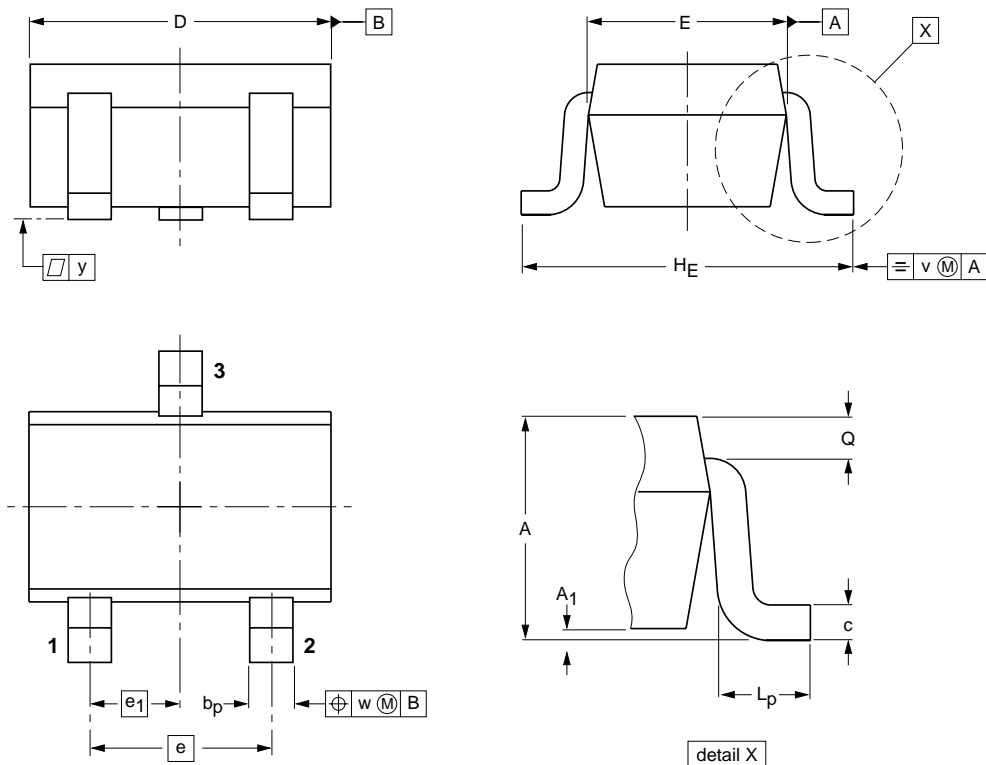


NPN resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = 10 kΩ

PDTC143X series

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

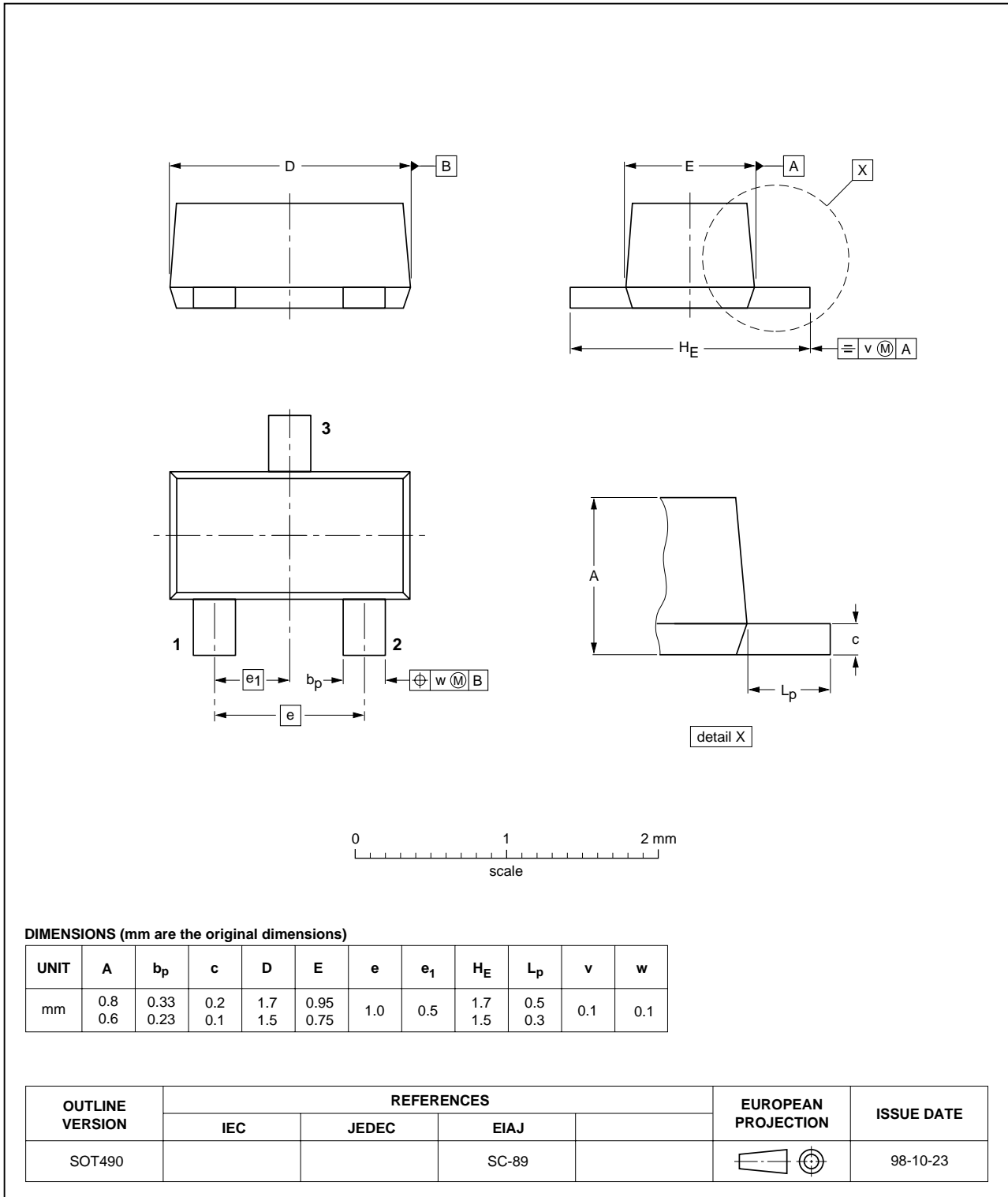
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

NPN resistor-equipped transistors;
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PDTC143X series

Plastic surface mounted package; 3 leads

SOT490



NPN resistor-equipped transistors;
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PDTC143X series

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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