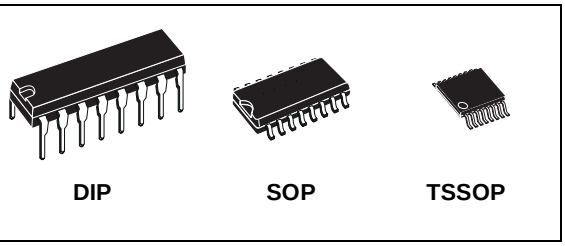
M74HC194

4 BIT PIPO SHIFT REGISTER

- HIGH SPEED :
  t_{PD} = 13 ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} =4μA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 194



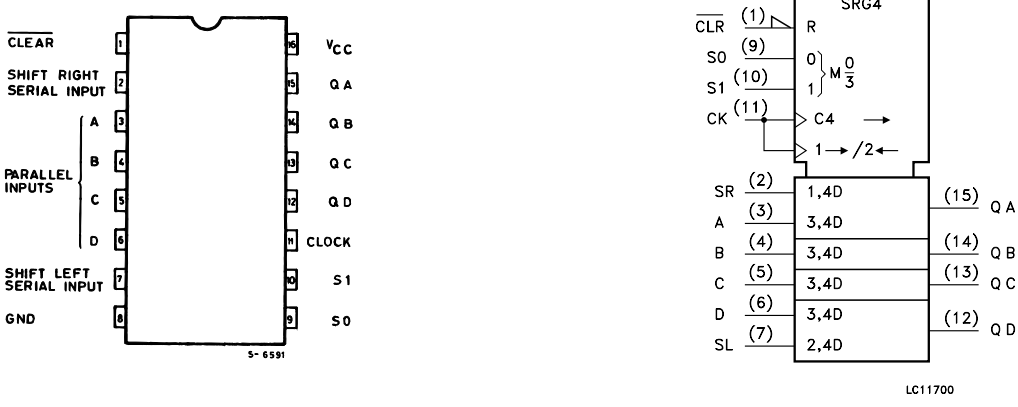
ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC194B1R	
SOP	M74HC194M1R	M74HC194RM13TR
TSSOP		M74HC194TTR

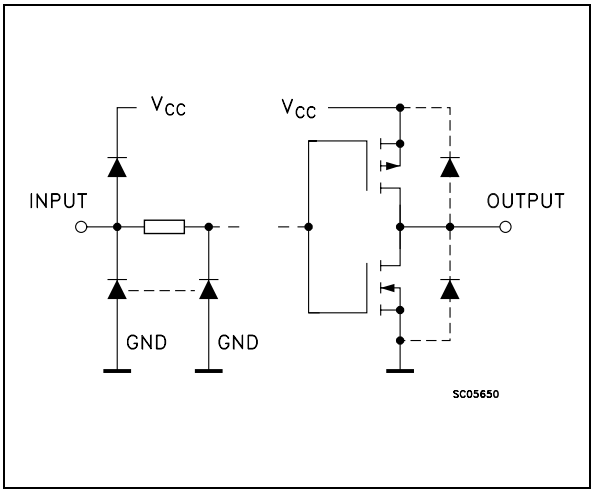
DESCRIPTION

The M74HC194 is an high speed CMOS 8 BIT PIPO SHIFT REGISTER fabricated with silicon gate C^2MOS technology. This SHIFT REGISTER is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, clear line. The register has four distinct modes of operation : PARALLEL (Broadside) LOAD ; SHIFT RIGHT(SR) (in the direction Q_A Q_D); SHIFT LEFT(SL); INHIBIT CLOCK (do nothing). Synchronous parallel loading is accomplished by applying the four data bits and taking both mode control inputs, S0 and S1 high. The data are loaded into their respective flip-flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shift left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

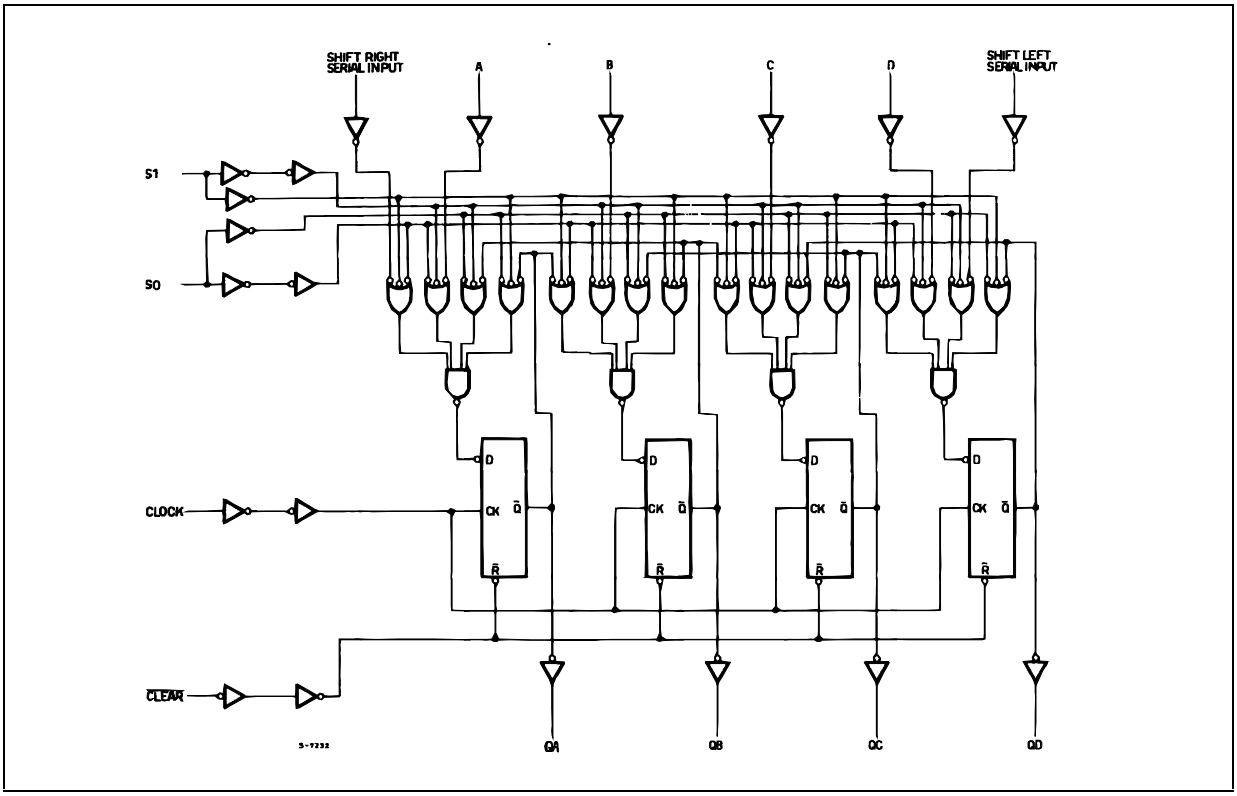
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Reset Input (Active LOW)
2	SR	Serial Data Input (Shift Right)
3, 4, 5, 6	A to D	Parallel Data Inputs
7	SL	Serial Data Input (Shift Left)
9, 10	S0, S1	Mode Control Inputs
11	CLOCK	Clock Input (LOW to HIGH Edge-triggered)
15, 14, 13, 12	QA to QD	Parallel Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS										OUTPUTS			
$\overline{\text{CLEAR}}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	⊓	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	⊔	X	X	a	b	c	d	a	b	c	d
H	L	H	⊔	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	⊔	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	⊔	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	⊔	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

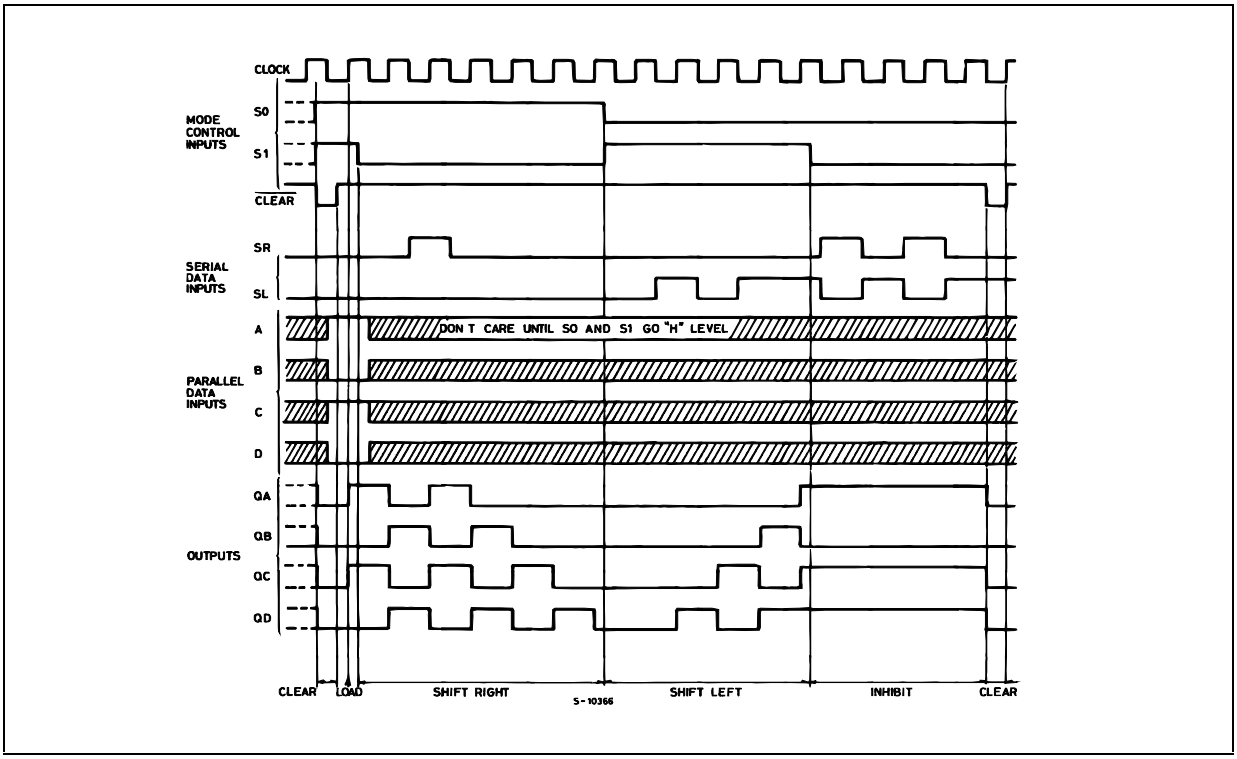
X : Don't Care
a ~ d : The level of steady state input voltage at input A ~ D
QA0 ~ QD0 : No Change
QAn ~ QDn : The level of QA, QB, QC, respectively, before the most recent positive transition of the clock.

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

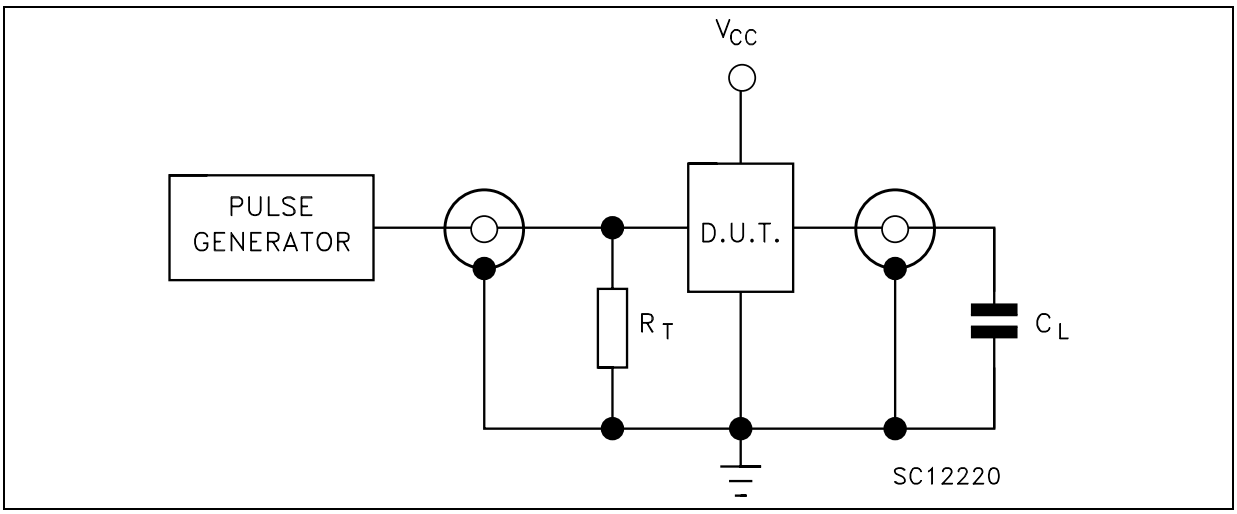
Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		115	ns
		4.5			8	15		19		23	
		6.0			7	13		16		20	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			48	115		145		175	ns
		4.5			15	23		29		35	
		6.0			13	20		25		30	
t_{PHL}	Propagation Delay Time ($\overline{CLEAR}$ - Q)	2.0			52	125		155		190	ns
		4.5			17	25		31		38	
		6.0			15	21		26		32	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	13		5.0		4.2		MHz
		4.5		31	50		25		21		
		6.0		37	59		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLEAR}$)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t_s	Minimum Set-up Time (SI, PI - CLOCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_s	Minimum Set-up Time (S0, S1 - CLOCK)	2.0			28	75		95		110	ns
		4.5			7	15		19		23	
		6.0			6	13		16		20	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			85						pF

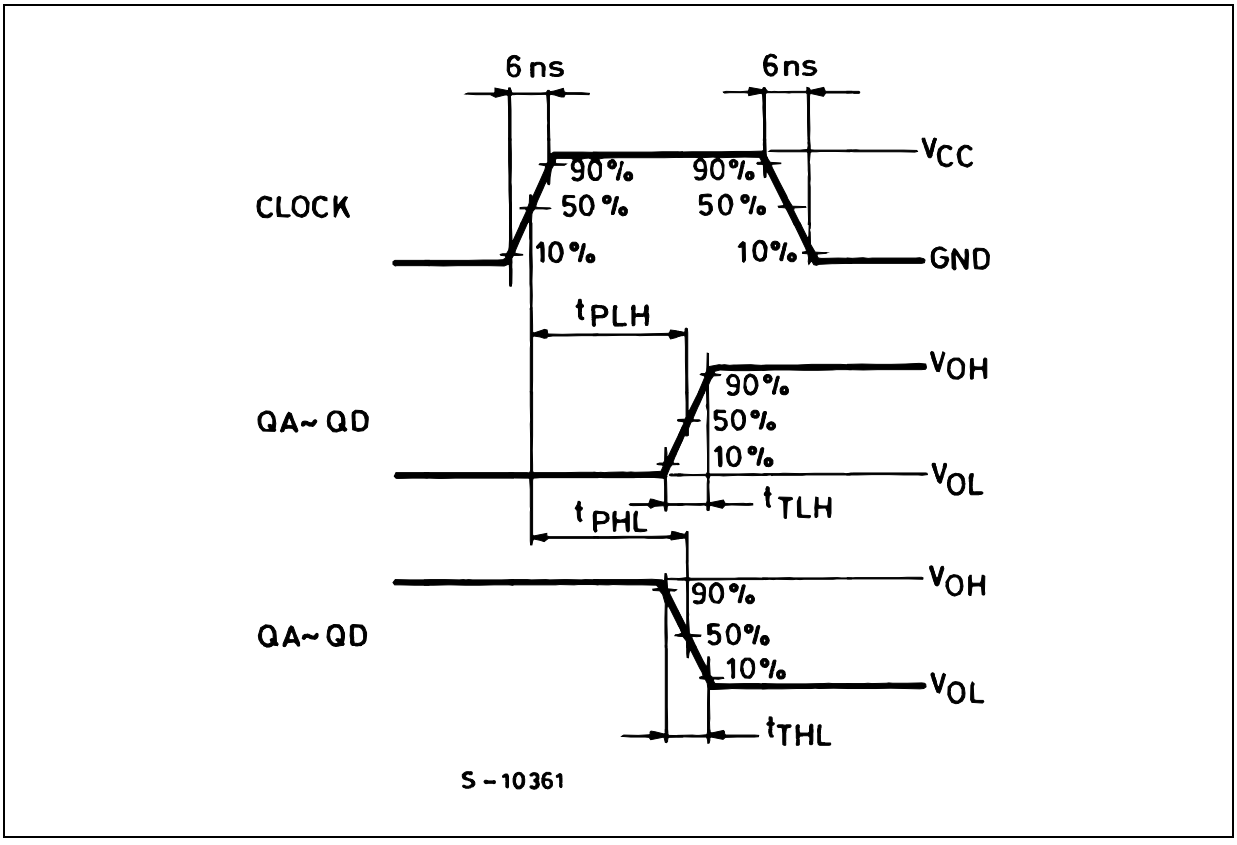
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT

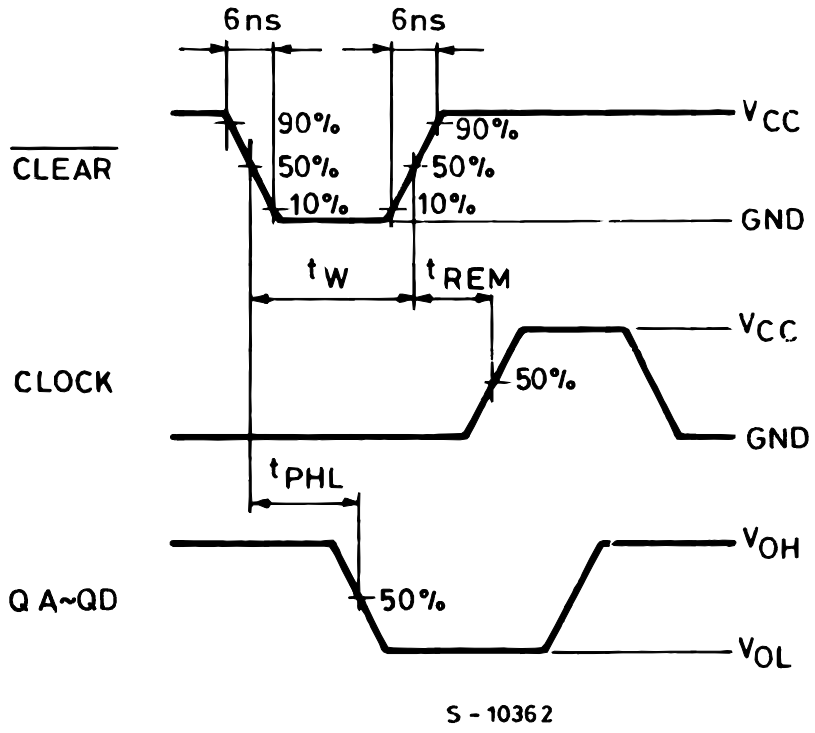


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_T = Z_{OUT} of pulse generator (typically 50Ω)

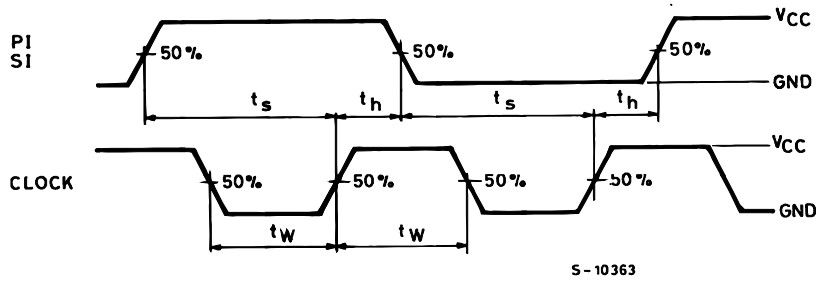
WAVEFORM 1 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



WAVEFORM 2 : MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)

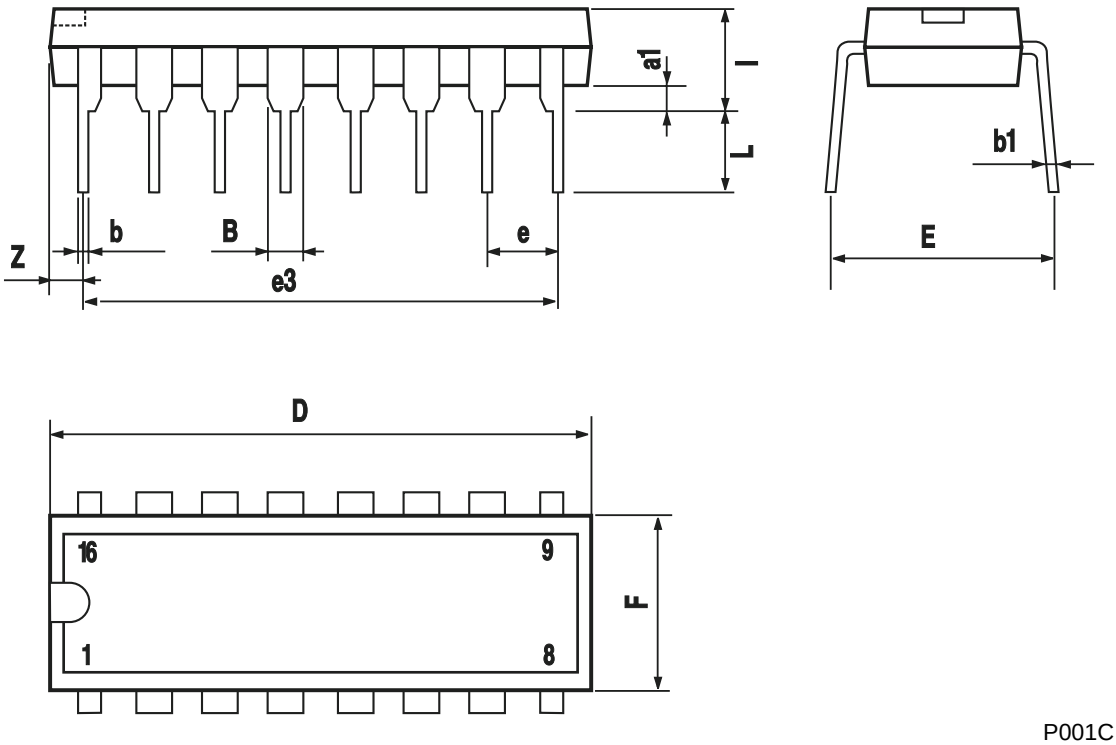


WAVEFORM 3 : MINIMUM PULSE WIDTH, SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

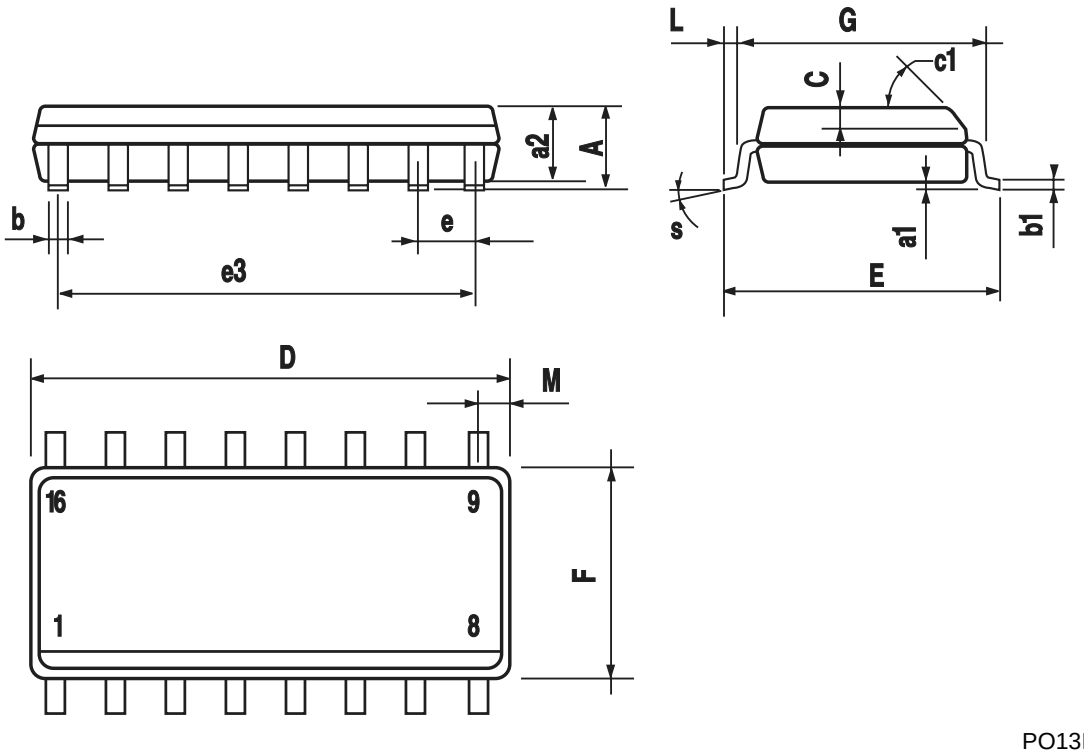
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030