MC100E256

5V ECL 3-Bit 4:1 Mux-Latch

The MC100E256 contains three 4:1 multiplexers followed by transparent latches with differential outputs. Separate Select controls are provided for the leading 2:1 mux pairs (see logic symbol).

When the Latch Enable (LEN) is LOW, the latch is transparent, and output data is controlled by the multiplexer select controls. A logic HIGH on LEN latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

The 100 Series contains temperature compensation.

- 950 ps Max. D to Output
- 850 ps Max. LEN to Output
- Split Select
- Differential Outputs
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 code V–0 @ 1/8″,
  Oxygen Index 28 to 34
- Transistor Count = 280 devices

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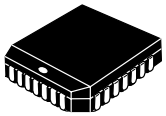
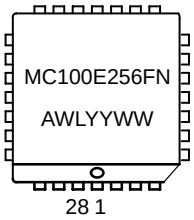
MARKING DIAGRAM



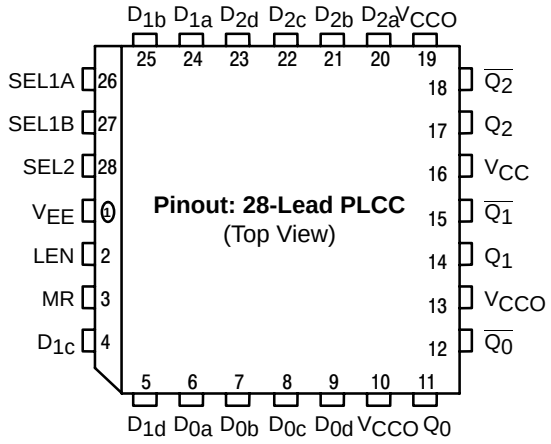


PLCC–28
FN SUFFIX
CASE 776

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100E256FN	PLCC–28	37 Units/Rail
MC100E256FNR2	PLCC–28	500 Units/Reel



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pin Assignment

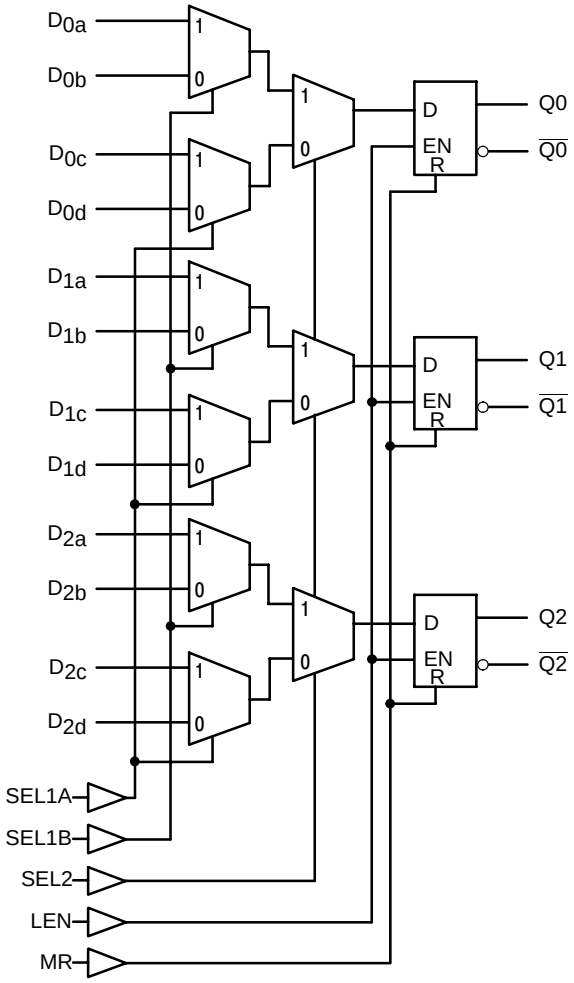


Figure 2. Logic Diagram

PIN DESCRIPTION

PIN	FUNCTION
$D_{0x} - D_{2x}$	ECL Data Inputs
SEL1A, SEL1B	ECL First-stage Select Inputs
SEL2	ECL Second-stage Select Input
LEN	ECL Latch Enable
MR	ECL Master Reset
Q_0, $\overline{Q_0} - Q_2$, $\overline{Q_2}$	ECL Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

Pin	State	Operation
SEL2	H	Output c/d Data
SEL1A	H	Input d Data
SEL1B	H	Input b Data

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 2)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		69	83		69	83		79	96	mA
V_{OH}	Output HIGH Voltage (Note 3)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 3)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.

100E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 4)

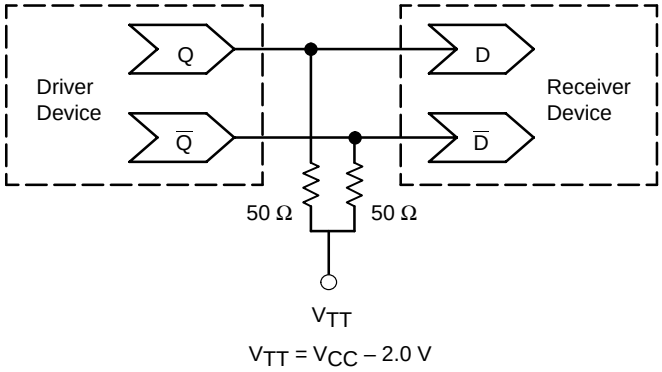
		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		69	83		69	83		79	96	mA
V_{OH}	Output HIGH Voltage (Note 5)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 5)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
5. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.

AC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = –5.0 V (Note 6)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	D	400	600	900	400	600	900	400	600	900	
	SEL1	550	775	1050	550	775	1050	550	775	1050	
	SEL2	450	650	900	450	650	900	450	650	900	
	LEN	350	500	800	350	500	800	350	500	800	
	MR	350	600	825	350	600	825	350	600	825	
t_S	Setup Time										ps
	D	400	275		400	275		400	275		
	SEL1	600	300		600	300		600	300		
	SEL2	500	250		500	250		500	250		
t_h	Hold Time										ps
	D	300	–275		300	–275		300	–275		
	SEL1	100	–300		100	–300		100	–300		
	SEL2	200	–250		200	–250		200	–250		
t_{RR}	Reset Recovery Time	700	600		700	600		700	600		ps
t_{PW}	Minimum Pulse Width										ps
	MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 7)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20 - 80%)	275	475	700	275	475	700	275	475	700	ps

6. 100 Series: V_{EE} can vary +0.46 V / –0.8 V.
7. Within-device skew is defined as identical transitions on similar paths through a device.



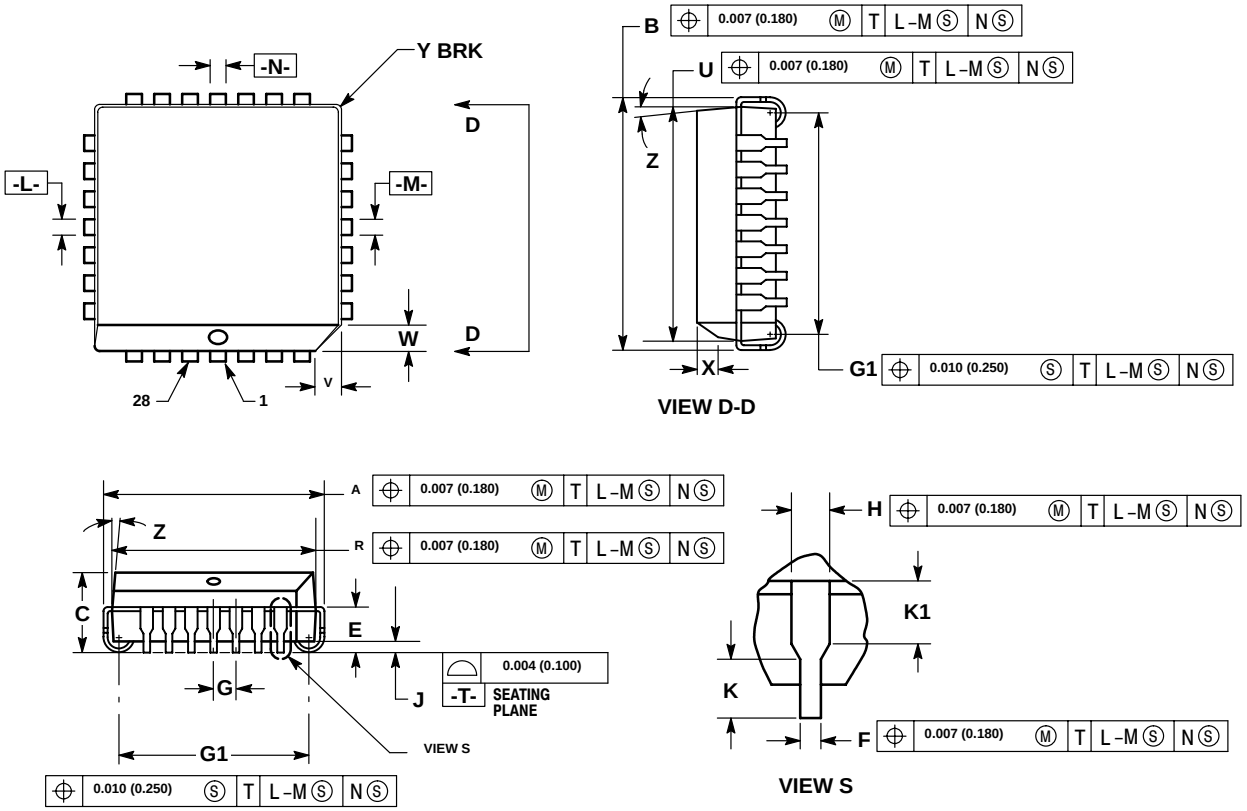
Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

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