# D68000

## 16/32-bit Microprocessor

## ver 1.15

### OVERVIEW

D68000 soft core is binary-compatible with the industry standard 68000 32-bit microcontroller. D68000 has a 16-bit data bus and 24-bit address data bus. It is code compatible with the MC68008 and is upward code compatible with the MC68010 virtual extensions and the MC68020 32-bit implementation of the architecture. D68000 has improved instructions set allows execution of a program with higher performance than standard 68000 core.

D68000 is delivered with **fully automated testbench** and **complete set of tests** allowing easy package validation at each stage of SoC design flow.

### KEY FEATURES

- Software compatible with industry standard 68000
- **MULS, MULU** take **28 clock periods**
- **DIVS, DIVU** take **28 clock periods**
- Optimized shifts and rotations
- Idle cycles removed to improve performance
- Shorter effective address calculation time
- Bus cycle timings **identical** to 68000
- 32 bit data and address registers
- 14 addressing modes:
  - *Direct:*
    - *Data register direct*
    - *Address register direct*
  - *Indirect:*
    - *Register indirect*
    - *Postincrement register indirect*
    - *Predecrement register indirect*
    - *Register indirect with offset*
    - *Indexed register indirect with offset*
  - *PC relative:*
    - *Relative with offset*
    - *Relative with index and offset*
  - *Absolute data:*
    - *Absolute short*
    - *Absolute long*
  - *Immediate data:*
    - *Immediate*
    - *Quick immediate*
  - *Implied*
- 5 data types supported:
  - *bits*
  - *BCD*
  - *bytes, words and long words*
- Arithmetic Logic Unit includes:
  - *8,16,32-bit arithmetic & logical operations*
  - *16x16 bit signed and unsigned multiplication*
  - *32/16 bit signed and unsigned division*
  - *Boolean operations*
- Interrupt controller:



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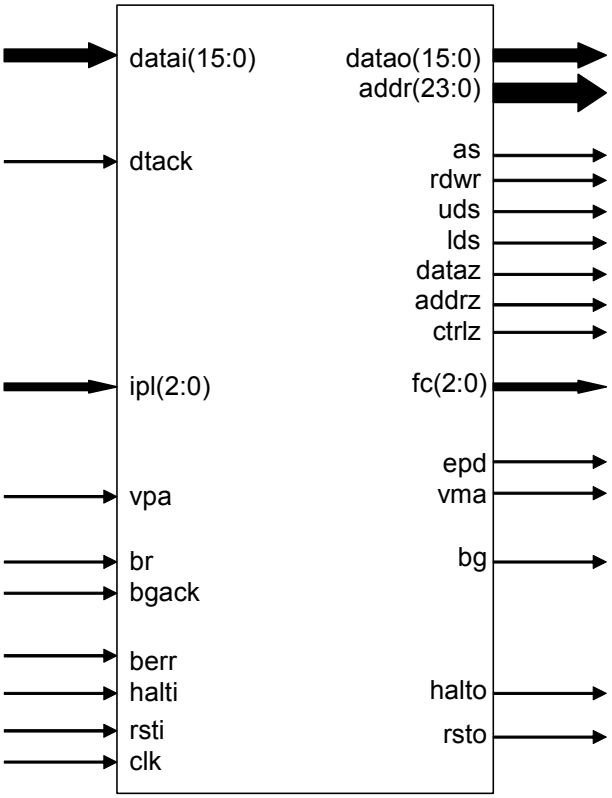
- *7 priority levels interrupt controller*
- *Unlimited number of virtual interrupt sources*
- *Vectored and auto-vectored modes*

- Memory interface includes:
  - *Up to 4 GB of address space*
  - *16-bit data bus*
  - *Asynchronous bus control*
- M6800 family synchronous interface
- 3- and 2- wire bus arbitration
- Supervisor and user modes
- Fully synthesizable, static synchronous design with no internal tri-states

## SYMBOL




## PINS DESCRIPTION

| PIN | TYPE | ACTIVE | DESCRIPTION |
|---|---|---|---|
| clk | input | High | Global clock |
| rsti | input | Low | Global reset input |
| halti | input | Low | Halt input |
| berr | input | Low | Bus error |
| vpa | input | Low | Valid peripheral address |
| ipl(2:0) | input | Low | Interrupt control |
| dtack | input | Low | Data transfer acknowledge |
| br | input | Low | Bus request |
| bgack | input | Low | Bus grant acknowledge |
| datai[15:0] | input | - | Data bus input |
| datao[15:0] | output | - | Data bus output |
| addr[23:0] | output | - | Address data bus |
| bg | output | Low | Bus grant |
| as | output | Low | Address strobe |
| rdwr | output | High/Low | Read write signal |
| uds | output | Low | Upper data byte strobe |
| lds | output | Low | Lower data byte strobe |
| addrz | output | High | Turns Address bus into 'Z' state |
| dataz | output | High | Turns Data bus into 'Z' state |
| ctrlz | output | High | Turns as, rdwr, uds, lds, vma, fc(2:0) signals into 'Z' state |
| fc(2:0) | output | High | Processor function code |
| epd | output | High | Enable peripheral device |
| vma | output | Low | Valid memory address |
| halto | output | Low | Halt output |
| rsto | output | Low | Reset output |

## DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance



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- Delivery the IP Core updates, minor and major versions changes
- Delivery the documentation updates
- Phone & email support

## LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

*Single Design* license allows use IP Core in single FPGA bitstream and ASIC implementation.

*Unlimited Designs*, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

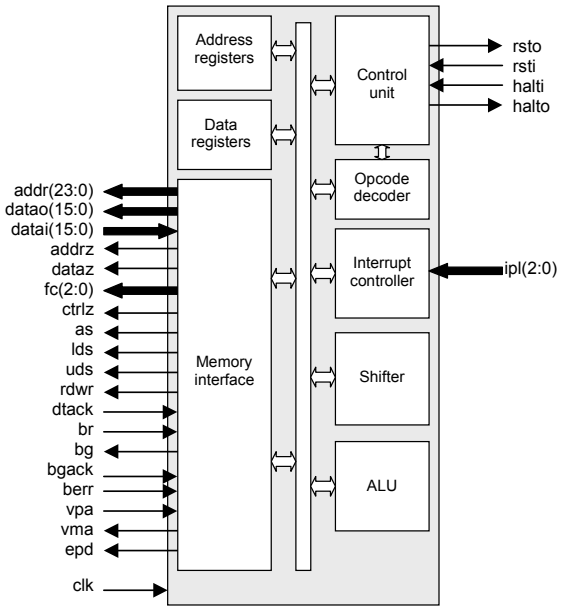
In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

## BLOCK DIAGRAM

**ALU** – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator and related logic such as arithmetic unit, logic unit, multiplier and divider. BCD operation are executed in this unit and condition code flags (N-negative, Z-zero, C-carry V-overflow) for most instructions.

**Shifter** – Performs shifting operations for the appropriate instructions, mainly for rotation, shift and bit operations.




**Control Unit** – Performs the core synchronization and data flow control. This module manages execution of all instructions. Contains SR (status register is consisted of two portions supervisor byte and user byte) and its related logic.

**Opcode Decoder** – Performs an instruction opcode decoding and the control functions for all other blocks.

**Memory Interface** – Contains memory access related registers It performs the memory addressing instructions code fetching and data transfers. It is responsible for all external bus cycle actions such as: read & write, repeated read & write, halt and resume of bus cycles, bus arbitration provided by 3- and 2- wire system, correct bus and address errors handling, wait states cycle insertion and M6800 synchronous cycle generation.

**Interrupt Controller** – Interrupt Control module is responsible for the interrupt manage system for the external & internal interrupts and exceptions processing. It manages auto-vectored interrupt cycles, priority resolving and correct vector numbers creation.

**Address registers** – Contains 32-bit A0 to A6 address registers, two stack pointers USP (user SP) and SSP (Supervisor SP), 32-bit Program counter and related logic to perform word and long address operations. An effective address operation are executed in this unit.

**Data registers** – Contains 32-bit data registers D0 to D7 and related logic to perform byte, word and long data operations.

## PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

| Device | Speed grade | Logic Cells | $F_{max}$ |
|---|---|---|---|
| APEX20K | -1 | 6332 | 30 MHz |
| APEX20KE | -1 | 6332 | 32 MHz |
| APEX20KC | -7 | 6332 | 37 MHz |
| APEX-II | -7 | 6657 | 40 MHz |
| MERCURY | -5 | 7086 | 45 MHz |
| STRATIX | -5 | 6862 | 49 MHz |
| CYCLONE | -6 | 6604 | 44 MHz |

*Core performance in ALTERA® devices*

## CONTACTS

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