

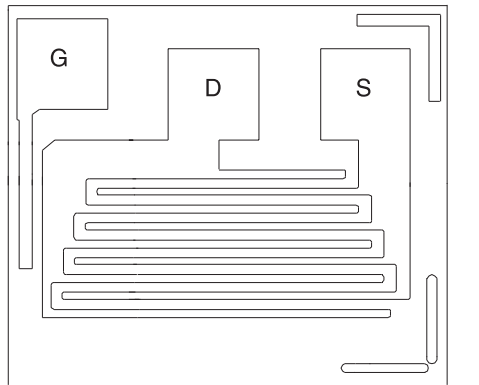
PROCESS CP206
Small Signal Transistors
N - Channel Switch/Chopper J FET Chip

CentralTM
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	21 x 18 MILS
Die Thickness	8.0 MILS
Drain Bonding Pad Area	3.8 X 3.8 MILS
Source Bonding Pad Area	3.8 X 3.8 MILS
Gate Bonding Pad Area	3.8 X 3.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 6,000Å

GEOMETRY



BACKSIDE GATE

GROSS DIE PER 4 INCH WAFER

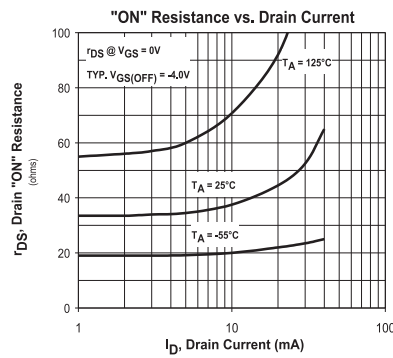
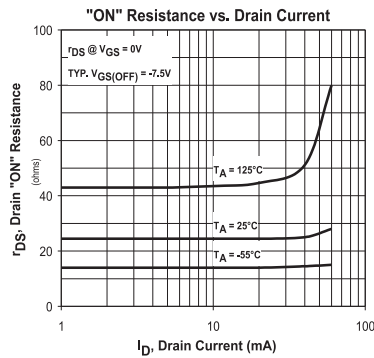
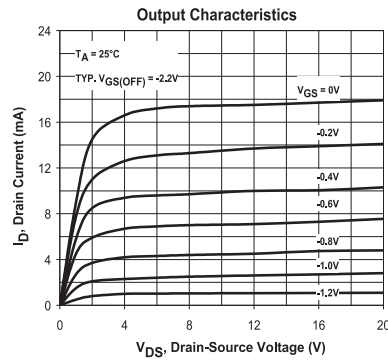
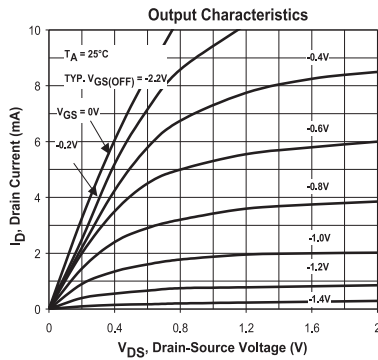
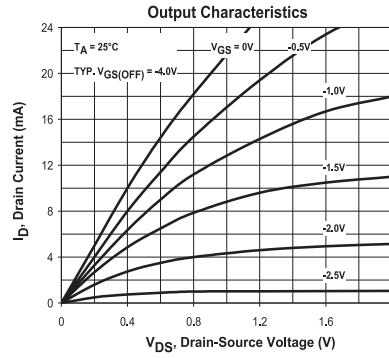
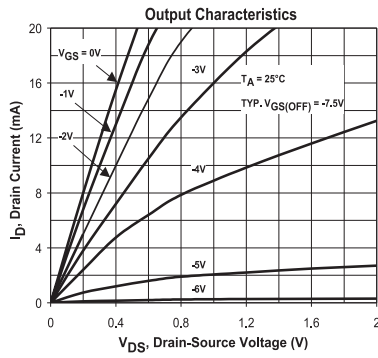
30,950

PRINCIPAL DEVICE TYPES

2N4391
 2N4392
 2N4393
 CMPF4391
 CMPF4392
 CMPF4393

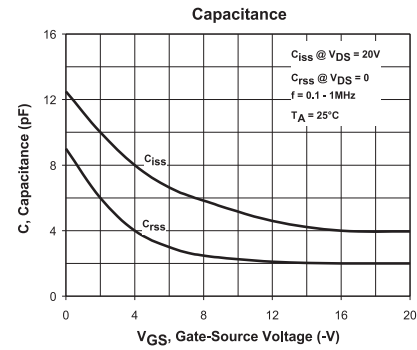
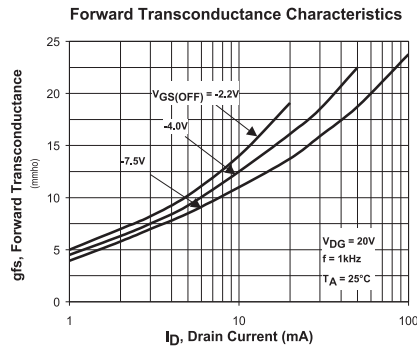
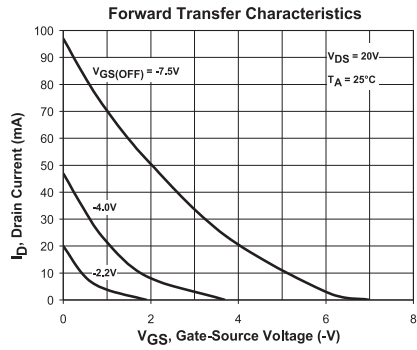
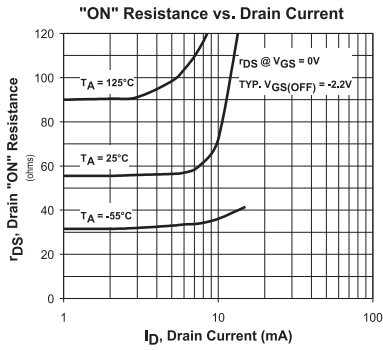
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R3 (9 -September 2003)



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