



LNBK20D2

LNB SUPPLY AND CONTROL VOLTAGE REGULATOR (PARALLEL INTERFACE)

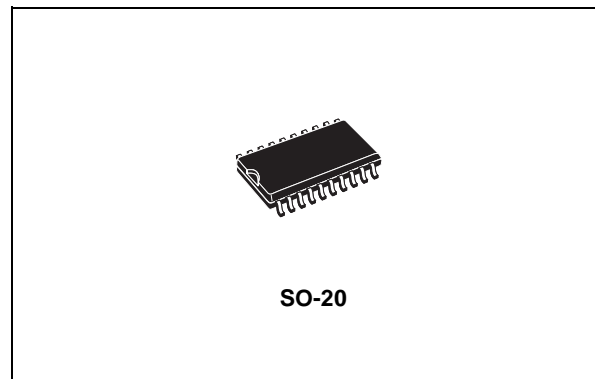
- COMPLETE INTERFACE FOR TWO LNBs REMOTE SUPPLY AND CONTROL
- GUARANTEED 400mA OUTPUT CURRENT
- LNB SELECTION AND STAND-BY FUNCTION
- BUILT-IN TONE OSCILLATOR FACTORY TRIMMED AT 22KHz
- FAST OSCILLATOR START-UP FACILITATES DiSEqC™ ENCODING
- TWO SUPPLY INPUTS FOR LOWEST DISSIPATION
- BYPASS FUNCTION FOR SLAVE OPERATION
- LNB SHORT CIRCUIT PROTECTION AND DIAGNOSTIC
- AUXILIARY MODULATION INPUT EXTENDS FLEXIBILITY
- CABLE LENGTH COMPENSATION
- INTERNAL OVER TEMPERATURE PROTECTION
- BACKWARD CURRENT PROTECTION
- COST-EFFECTIVE VERSION OF LNBP SERIES

DESCRIPTION

Intended for analog and digital satellite receivers, the LNBK20D2 is a monolithic linear voltage regulator, assembled in SO-20, specifically designed to provide the powering voltages and the interfacing signals to the LNB downconverter situated in the antenna via the coaxial cable. It has the same functionality of the LNBP1X and LNBP20 series, at a reduced output current capability. Since most satellite receivers have two antenna ports, the output voltage of the regulator is available at one of two logic-selectable output pins (LNBA, LNBB). When the IC is powered and put in Stand-by (EN pin LOW), both regulator outputs are disabled to allow the antenna downconverters to be supplied/controlled by others satellite receivers sharing the same coaxial lines. In this occurrence the device will limit at 3 mA (max) the backward current that could flow from LNBA and LNBB output pins to GND.

For slave operation in single dish, dual receiver systems, the bypass function is implemented by an electronic switch between the Master Input pin

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(MI) and the LNBA pin, thus leaving all LNB powering and control functions to the Master Receiver. This electronic switch is closed when the device is powered and EN pin is LOW.

The regulator outputs can be logic controlled to be 13 or 18 V (typ.) by mean of the VSEL pin for remote controlling of LNBs. Additionally, it is possible to increment by 1V (typ.) the selected voltage value to compensate the excess voltage drop along the coaxial cable (LLC pin HIGH).

In order to reduce the power dissipation of the device when the lowest output voltage is selected, the regulator has two Supply Input pins V_{CC1} and V_{CC2} . They must be powered respectively at 16V (min) and 23V (min), and an internal switch automatically will select the suitable supply pin according to the selected output voltage. If adequate heatsink is provided and higher power losses are acceptable, both supply pins can be powered by the same 23V source without affecting any other circuit performance.

The ENT (Tone Enable) pin activates the internal oscillator so that the DC output is modulated by a ± 0.3 V, 22KHz (typ.) square wave. This internal oscillator is factory trimmed within a tolerance of ± 2 KHz, thus no further adjustments neither external components are required.

A burst coding of the 22KHz tone can be accomplished thanks to the fast response of the ENT input and the prompt oscillator start-up. This helps designers who want to implement the DiSEqC™ protocols (*).

In order to improve design flexibility and to allow implementation of newcoming LNB remote control standards, an analogic modulation input pin is

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available (EXTM). An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. When external modulation is not used, the relevant pin can be left open.

Two pins are dedicated to the overcurrent protection/monitoring: CEXT and OLF. The overcurrent protection circuit works dynamically: as soon as an overload is detected in either LNB output, the output is shut-down for a time T_{off} determined by the capacitor connected between CEXT and GND. Simultaneously the OLF pin, that is an open collector diagnostic output flag, from HIGH IMPEDANCE state goes LOW.

After the time has elapsed, the output is resumed for a time $t_{on}=1/15t_{off}$ (typ.) and OLF goes in HIGH

IMPEDANCE. If the overload is still present, the protection circuit will cycle again through t_{off} and t_{on} until the overload is removed. Typical $t_{on}+t_{off}$ value is 1200ms when a $4.7\mu F$ external capacitor is used.

This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up even with highly capacitive loads on LNB outputs.

The device is packaged in Multiwatt15 for thru-holes mounting and in PowerSO-20 for surface mounting. When a limited functionality in a smaller package matches design needs, a range of cost-effective PowerSO-10 solutions is also offered. All versions have built-in thermal protection against overheating damage.

(*): External components are needed to comply to level 2.x and above (bidirectiona) DiSEqC™ bus hardware requirements. DiSEqC™ is a trademark or EUTELSAT.

PIN CONFIGURATION (top view)

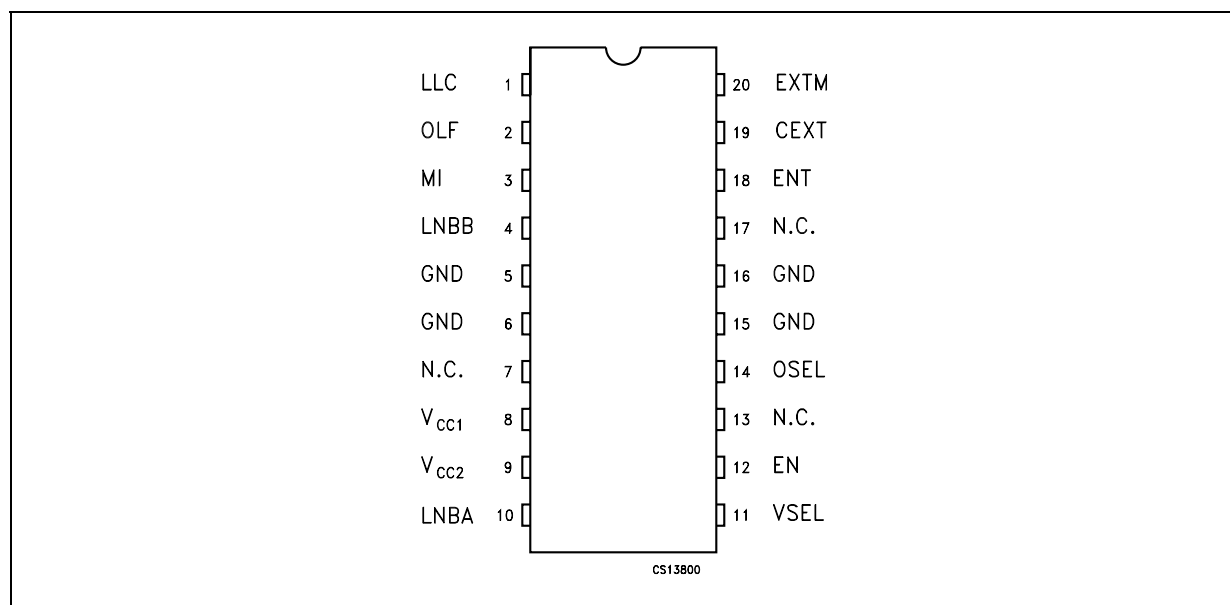


TABLE A: PIN CONFIGURATIONS

PIN N°	SYMBOL	NAME	FUNCTION
1	LLC	Line Length Compens. (1V typ)	Logic control input: see truth table
2	OLF	Over Load Flag	Logic output (open collector). Normally in HIGH IMPEDANCE, goes LOW when current or thermal overload occurs
3	MI	Master Input	In stand-by mode, the voltage on MI is routed to LNBA pin. Can be left open if bypass function is not needed
4	LNBB	Output Port	See truth tables for voltage and port selection
5, 6, 15, 16	GND	Ground	Circuit Ground. It is internally connected to the die frame
7, 13	N.C.	Not Connected	
8	V _{CC1}	Supply Input 1	15V to 27V supply. It is automatically selected when V _{OUT} = 13 or 14V
9	V _{CC2}	Supply Input 2	22V to 27V supply. It is automatically selected when V _{OUT} = 18 or 19V
10	LNBA	Output Port	See truth table voltage and port selection. In stand-by mode this port is powered by the MI pin via the internal Bypass Switch
11	V _{SEL}	Output Voltage Selection: 13 or 18V (typ)	Logic control input: see truth table
12	EN	Port Enable	Logic control input: see truth table
14	OSEL	Port Selection	Logic control input: see truth table
18	ENT	22KHz Tone Enable	Logic control input: see truth table
19	CEXT	External Capacitor	Timing Capacitor used by the Dynamic Overload protection. Typical application is 4.7μF for a 1200ms cycle
20	EXTM	External Modulator	External Modulation Input. Needs DC decoupling to the AC source. if not used, can be left open.

NOTE: the limited pin availability of the PowerSO-10 package leads to drop some functions.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter ²	Value	Unit
V _I	DC Input Voltage (V _{CC1} , V _{CC2} , MI)	28	V
I _O	Output Current (LNBA, LNBB)	Internally Limited	mA
V _I	Logic Input Voltage (ENT, EN OSEL, VSEL, LLC)	-0.5 to 7	V
I _{SW}	Bypass Switch Current	900	mA
P _D	Power Dissipation at T _{case} < 85°C	3	W
T _{stg}	Storage Temperature Range	-40 to +150	°C
T _{op}	Operating Junction Temperature Range	-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal Resistance Junction-case	15	°C/W

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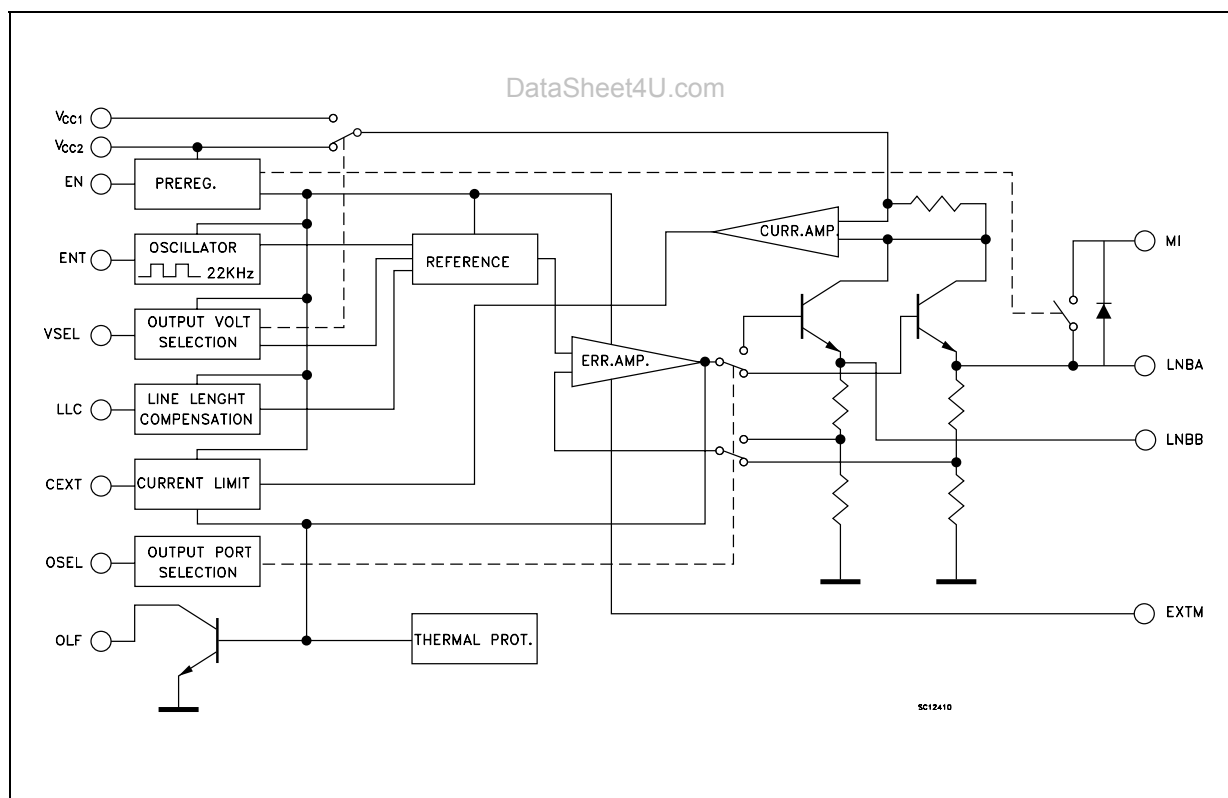
LOGIC CONTROLS TRUTH TABLE

CONTROL I/O	PIN NAME	L	H
OUT	OLF	$I_{OUT} > I_{OMAX}$ or $T_j > 150^{\circ}\text{C}$	$I_{OUT} < I_{OMAX}$
IN	ENT	22KHz tone OFF	22KHz tone ON
IN	EN	See Table Below	See Table Below
IN	OSEL	See Table Below	See Table Below
IN	VSEL	See Table Below	See Table Below
IN	LLC	See Table Below	See Table Below

EN	OSEL	VSEL	LLCO	V_{LNBA}	V_{LNBB}
L	X	X	X	$V_{MI} - 0.4\text{V (typ.)}$	Disabled
H	L	L	L	13V (typ.)	Disabled
H	L	H	L	18V (typ.)	Disabled
H	L	L	H	14V (typ.)	Disabled
H	L	H	H	19V (typ.)	Disabled
H	H	L	L	Disabled	13V (typ.)
H	H	H	L	Disabled	18V (typ.)
H	H	L	H	Disabled	14V (typ.)
H	H	H	H	Disabled	19V (typ.)

NOTE: All logic input pins have internal pull-down resistor (typ. = 250K Ω)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS FOR LNBK SERIES ($T_J = 0$ to 85°C , $C_I = 0.22\mu\text{F}$, $C_O = 0.1\mu\text{F}$, $\text{EN}=\text{H}$, $\text{ENT}=\text{L}$, $\text{LLC}=\text{L}$, $V_{\text{IN}1}=16\text{V}$, $V_{\text{IN}2}=23\text{V}$ $I_{\text{OUT}}=50\text{mA}$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{IN}1}$	$V_{\text{CC}1}$ Supply Voltage	$I_O = 400\text{ mA}$ $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$	15		27	V
		$I_O = 400\text{ mA}$ $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$	16		27	V
$V_{\text{IN}2}$	$V_{\text{CC}2}$ Supply Voltage	$I_O = 400\text{ mA}$ $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$	22		27	V
		$I_O = 400\text{ mA}$ $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$	23		27	V
$V_{\text{O}1}$	Output Voltage	$I_O = 400\text{ mA}$ $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$	17.3	18	18.7	V
		$I_O = 400\text{ mA}$ $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$		19		V
$V_{\text{O}2}$	Output Voltage	$I_O = 400\text{ mA}$ $\text{VSEL}=\text{L}$, $\text{LLC}=\text{L}$	12.5	13	13.5	V
		$I_O = 400\text{ mA}$ $\text{ENT}=\text{H}$, $\text{VSEL}=\text{L}$, $\text{LLC}=\text{H}$		14		V
ΔV_O	Line Regulation	$V_{\text{IN}1}=15$ to 18V $V_{\text{OUT}}=13\text{V}$		5	50	mV
		$V_{\text{IN}2}=22$ to 25V $V_{\text{OUT}}=18\text{V}$		5	50	mV
ΔV_O	Load Regulation	$V_{\text{IN}1}=V_{\text{IN}2}=22\text{V}$ $V_{\text{OUT}}=13$ or 18V $I_O = 0$ to 3A		65	150	mV
SVR	Supply Voltage Rejection	$V_{\text{IN}1} = V_{\text{IN}2} = 23 \pm 0.5V_{\text{ac}}$ $f_{\text{ac}} = 120\text{ Hz}$,		45		dB
I_{MAX}	Output Current Limiting		500	650	800	mA
t_{OFF}	Dynamic Overload protection OFF Time	Output Shorted $C_{\text{EXT}} = 4.7\mu\text{F}$		1100		ms
t_{ON}	Dynamic Overload protection ON Time	Output Shorted $C_{\text{EXT}} = 4.7\mu\text{F}$		$t_{\text{OFF}}/15$		ms
f_{TONE}	Tone Frequency	$\text{ENT}=\text{H}$	20	22	24	KHz
A_{TONE}	Tone Amplitude	$\text{ENT}=\text{H}$	0.55	0.72	0.9	Vpp
D_{TONE}	Tone Duty Cycle	$\text{ENT}=\text{H}$ DataSheet4U.com	40	50	60	%
t_r, t_f	Tone Rise and Fall Time	$\text{ENT}=\text{H}$	5	10	15	μs
G_{EXTM}	External Modulation Gain	$\Delta V_{\text{OUT}}/\Delta V_{\text{EXTM}}$, $f = 10\text{Hz}$ to 40KHz		5		
V_{EXTM}	External Modulation Input Voltage	AC Coupling			400	mVpp
Z_{EXTM}	External Modulation Impedance	$f = 10\text{Hz}$ to 40KHz		400		Ω
V_{SW}	Bypass Switch Voltage Drop (MI to LNBA)	$\text{EN}=\text{L}$, $I_{\text{SW}}=300\text{mA}$, $V_{\text{CC}2}-V_{\text{MI}}=4\text{V}$		0.35	0.6	V
V_{OL}	Overload Flag Pin Logic LOW	$I_{\text{OL}}=8\text{mA}$		0.28	0.5	V
I_{OZ}	Overload Flag Pin OFF State Leakage Current	$V_{\text{OH}} = 6\text{V}$			10	μA
V_{IL}	Control Input Pin Logic LOW				0.8	V
V_{IH}	Control Input Pin Logic HIGH		2.5			V
I_{IH}	Control Pins Input Current	$V_{\text{IH}} = 5\text{V}$		20		μA
I_{CC}	Supply Current	Output Disabled ($\text{EN}=\text{L}$)		0.3	1	mA
		$\text{ENT}=\text{H}$, $I_{\text{OUT}}=50\text{mA}$		3.1	6	mA
I_{OBK}	Output Backward Current	$\text{EN}=\text{L}$ $V_{\text{LNBA}} = V_{\text{LNBB}} = 18\text{V}$ $V_{\text{IN}1} = V_{\text{IN}2} = 22\text{V}$ or floating		0.2	3	mA
T_{SHDN}	Temperature Shutdown Threshold			150		$^\circ\text{C}$

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TYPICAL CHARACTERISTICS (unless otherwise specified $T_j = 25^\circ\text{C}$)

Figure 1 : Output Voltage vs Output Current

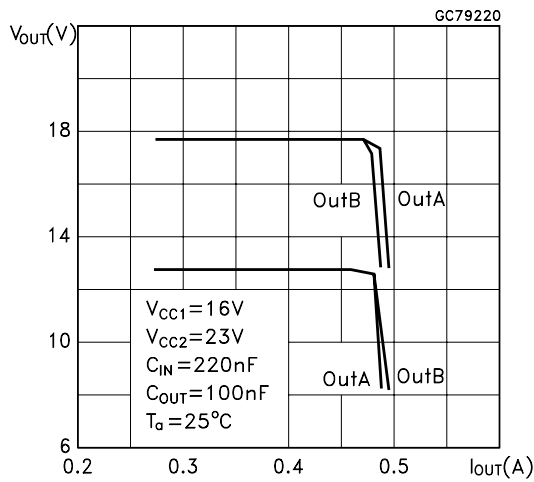


Figure 2 : Tone Duty Cycle vs Temperature

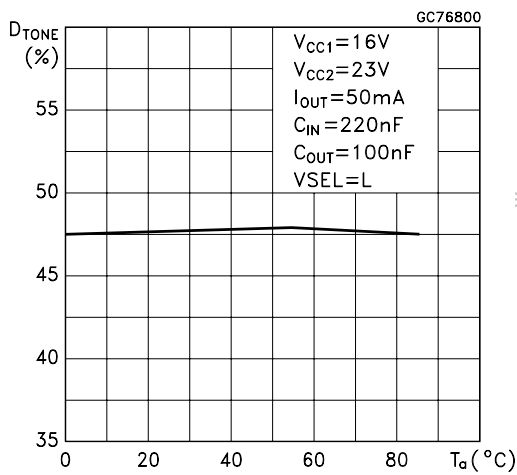


Figure 3 : Tone Fall Time vs Temperature

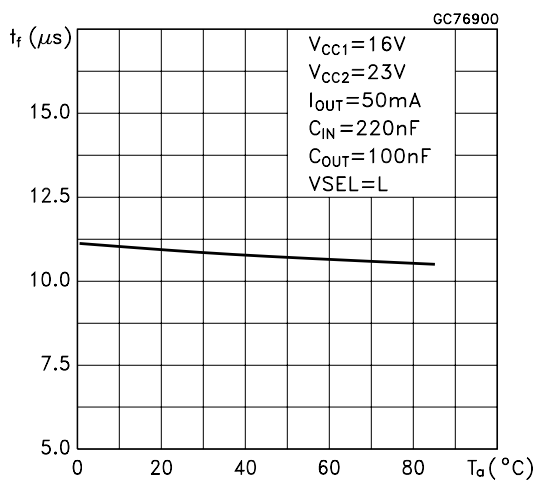


Figure 4 : Tone Frequency vs Temperature

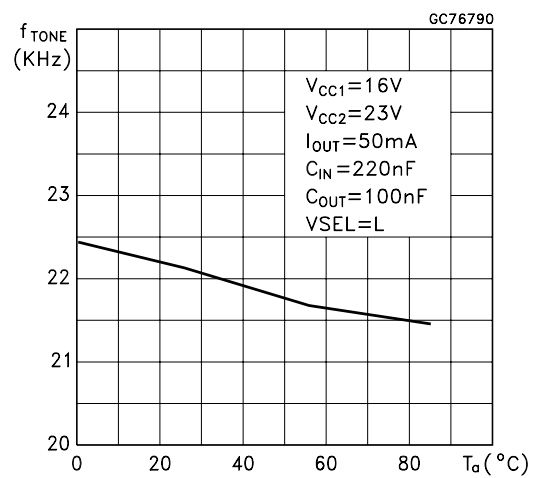


Figure 5 : Tone Rise Time vs Temperature

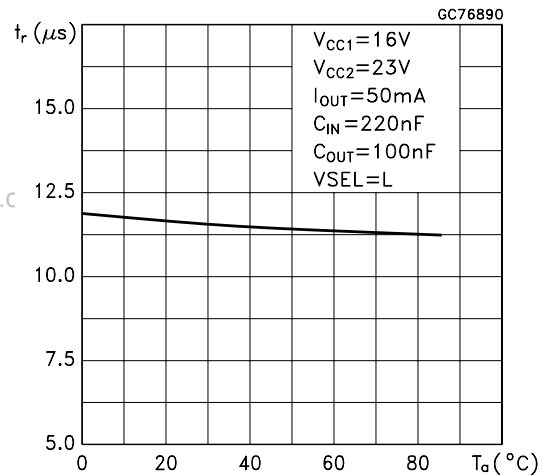


Figure 6 : Tone Amplitude vs Temperature

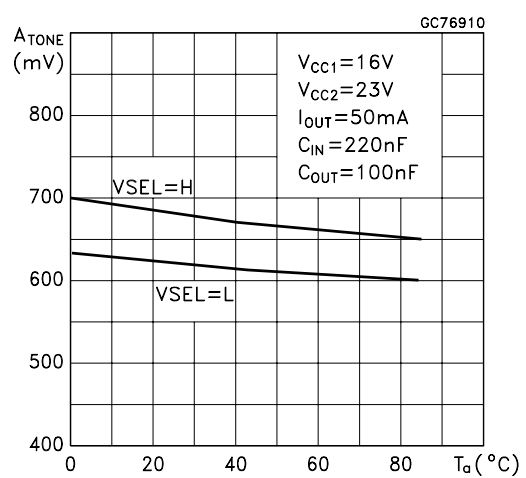


Figure 7 : S.V.R. vs Frequency

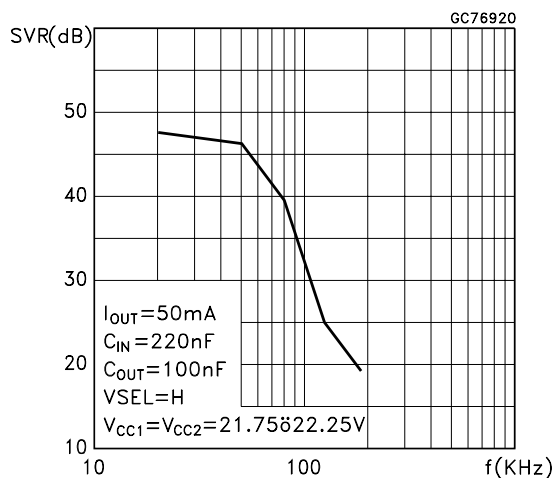


Figure 10 : LNBA External Modulation gain vs Frequency

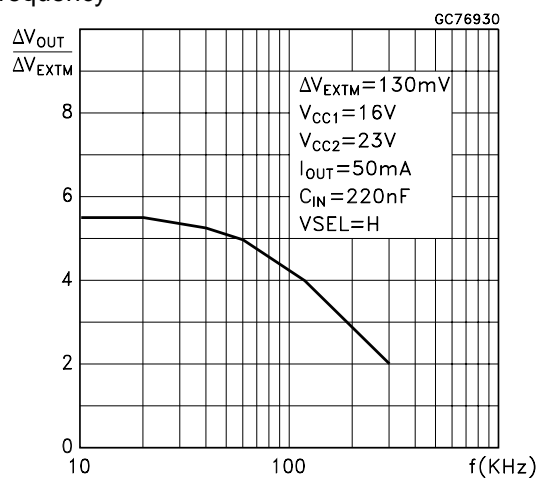


Figure 8 : External Modulation vs Temperature

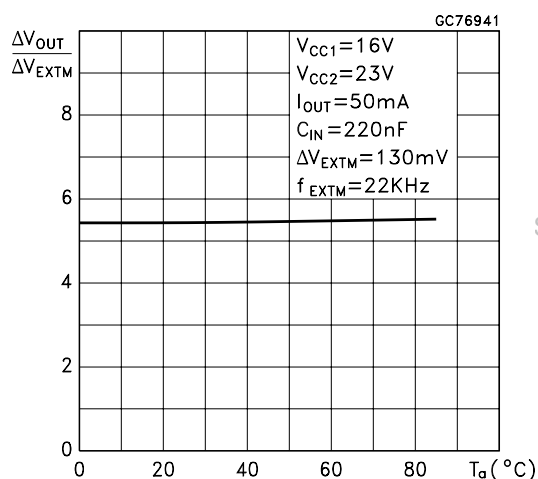


Figure 11 : Bypass switch Drop vs Output Current

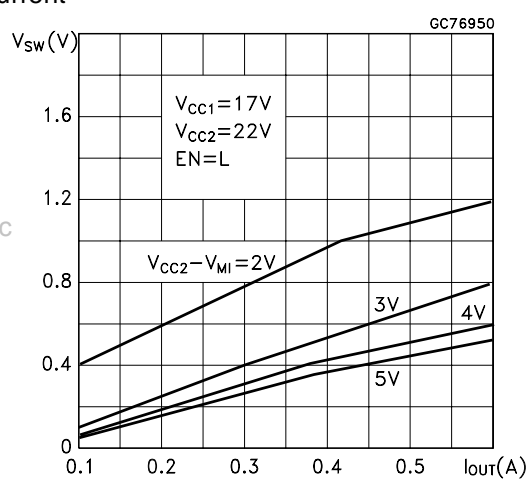


Figure 9 : Bypass Switch Drop vs Output Current

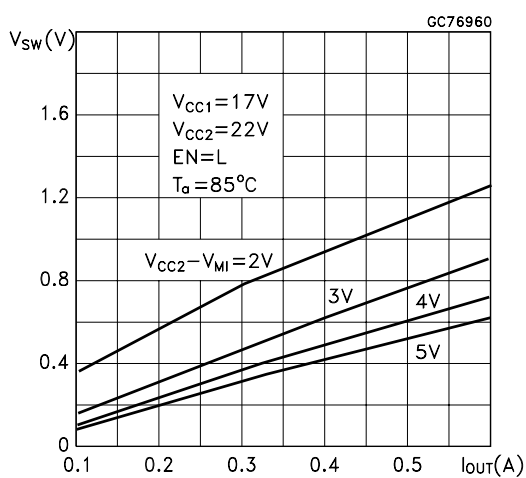
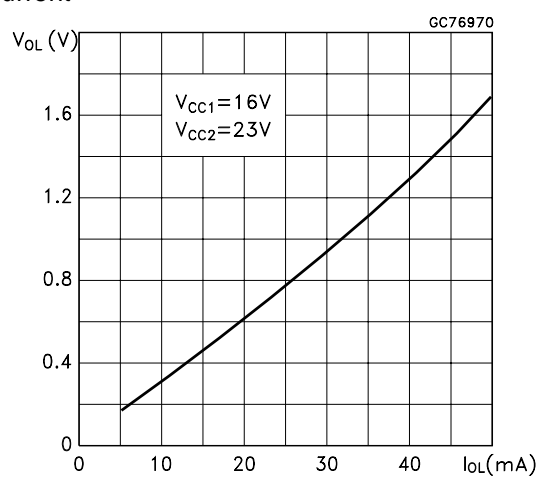


Figure 12 : overload Flag pin Logic LOW vs Flag Current



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Figure 13 : Supply Voltage vs Temperature

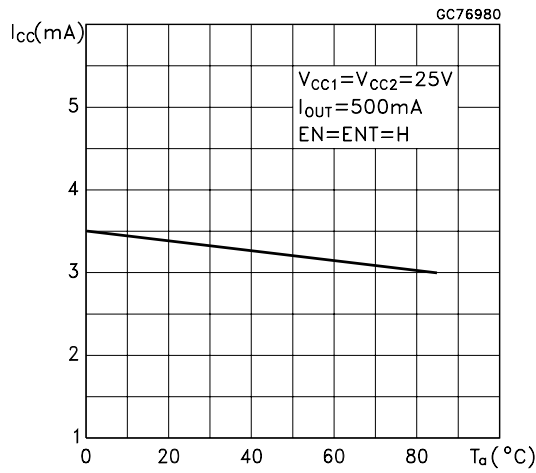


Figure 16 : Tone Enable

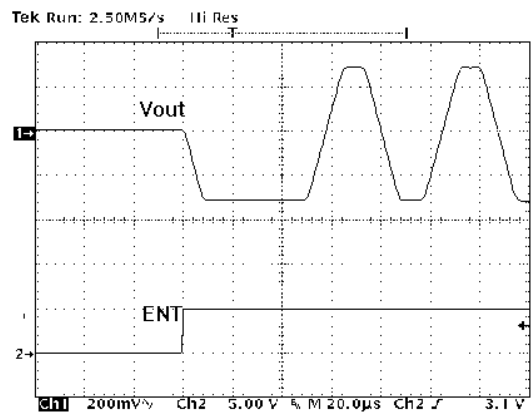


Figure 14 : Supply Current vs Temperature

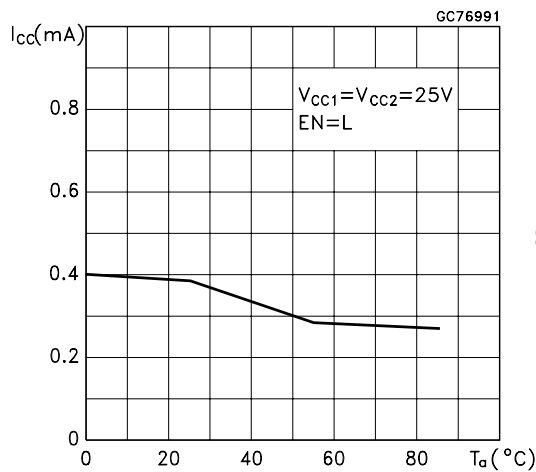


Figure 17 : Tone Disable

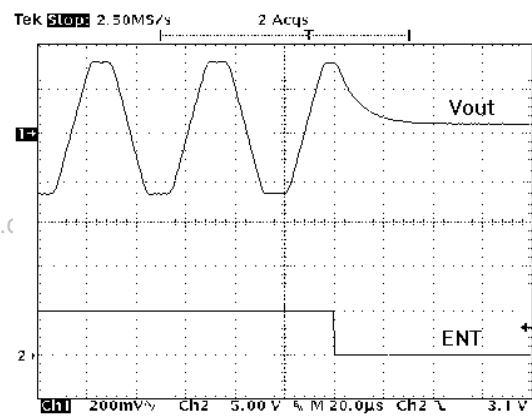


Figure 15 : Dynamic Overload protection (I_{SC} vs Time)

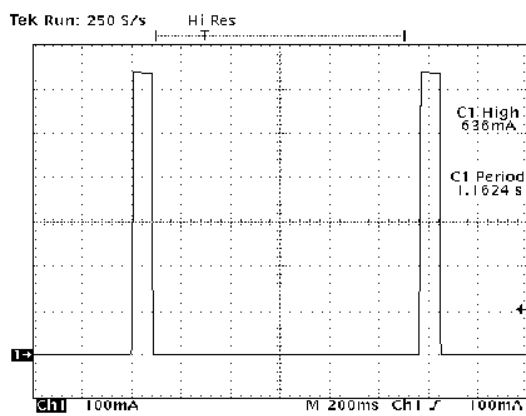
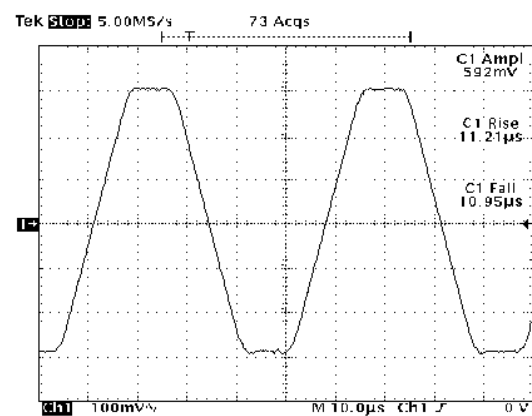
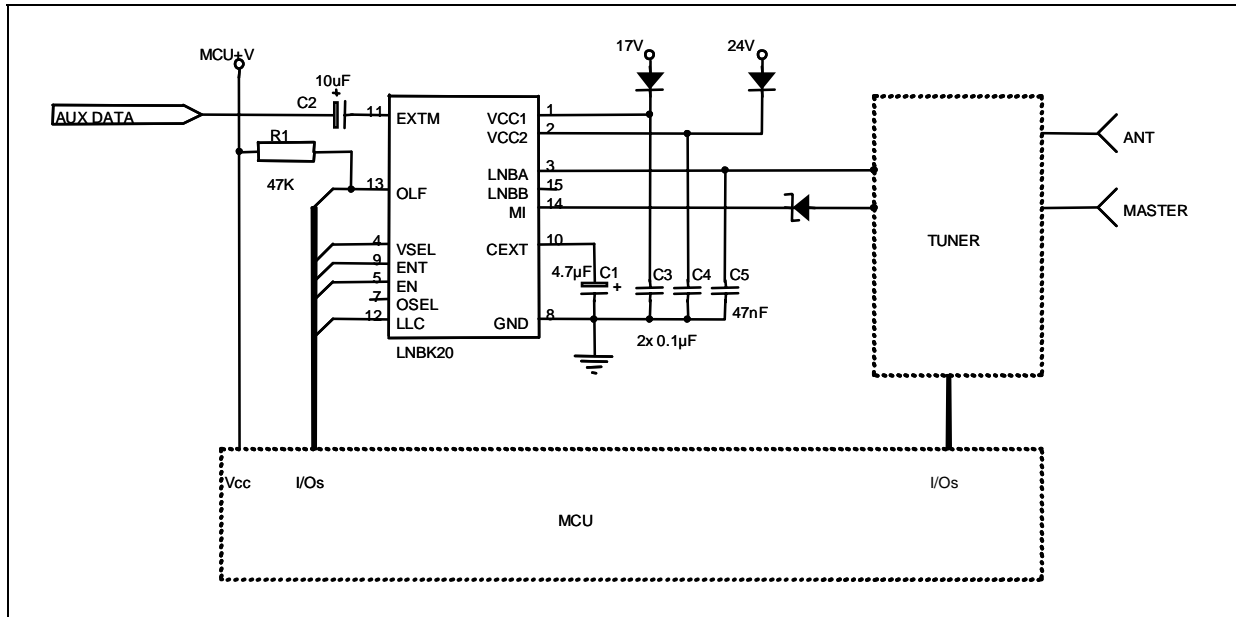


Figure 18 : 22KHz Tone

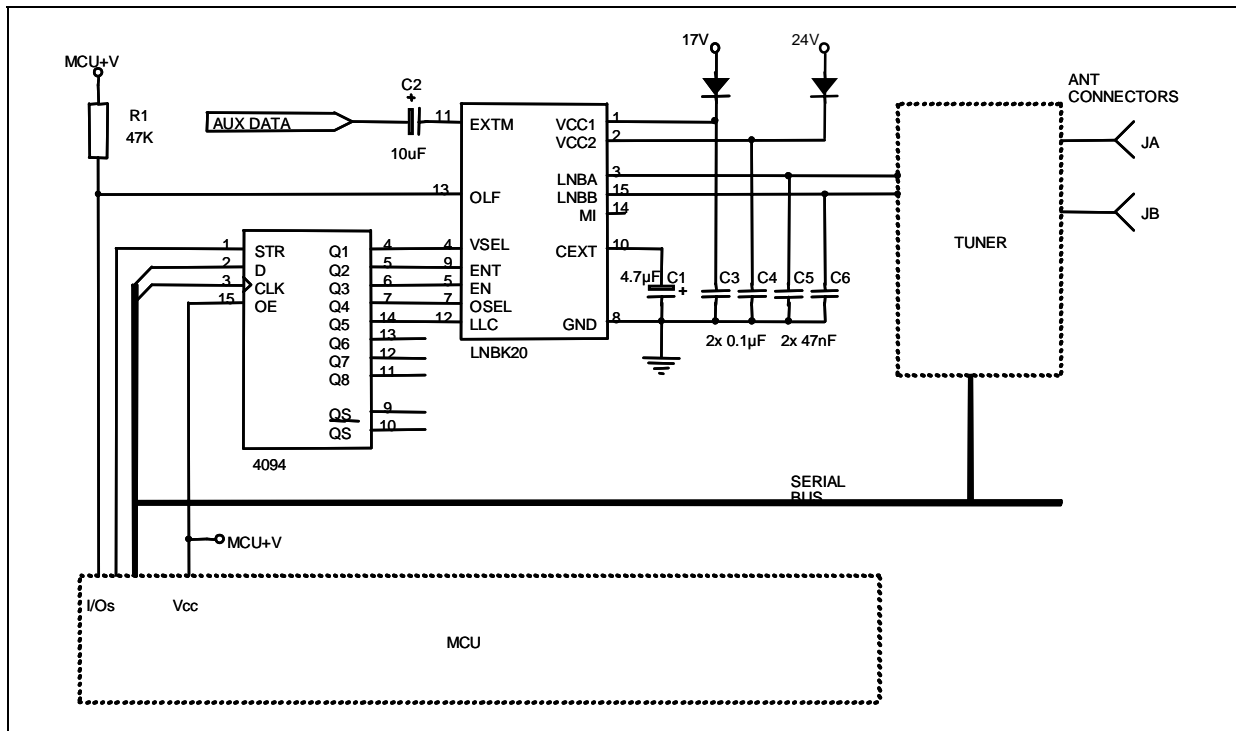


LN BK20D2

SINGLE ANTENNA RECEIVER WITH MASTER RECEIVER PORT



USING SERIAL BUS TO SAVE MPU I/Os



THERMAL DESIGN NOTE

During normal operation, this device dissipates some power. At maximum rated output current (400mA), the voltage drop on the linear regulator lead to a total dissipated power that is of about 2W. The heat generated requires a suitable heatsink to keep the junction temperature below the over temperature protection threshold. Assuming a 40°C temperature inside the Set-Top-Box case, the total $R_{thj-amb}$ has to be less than 43°C/W.

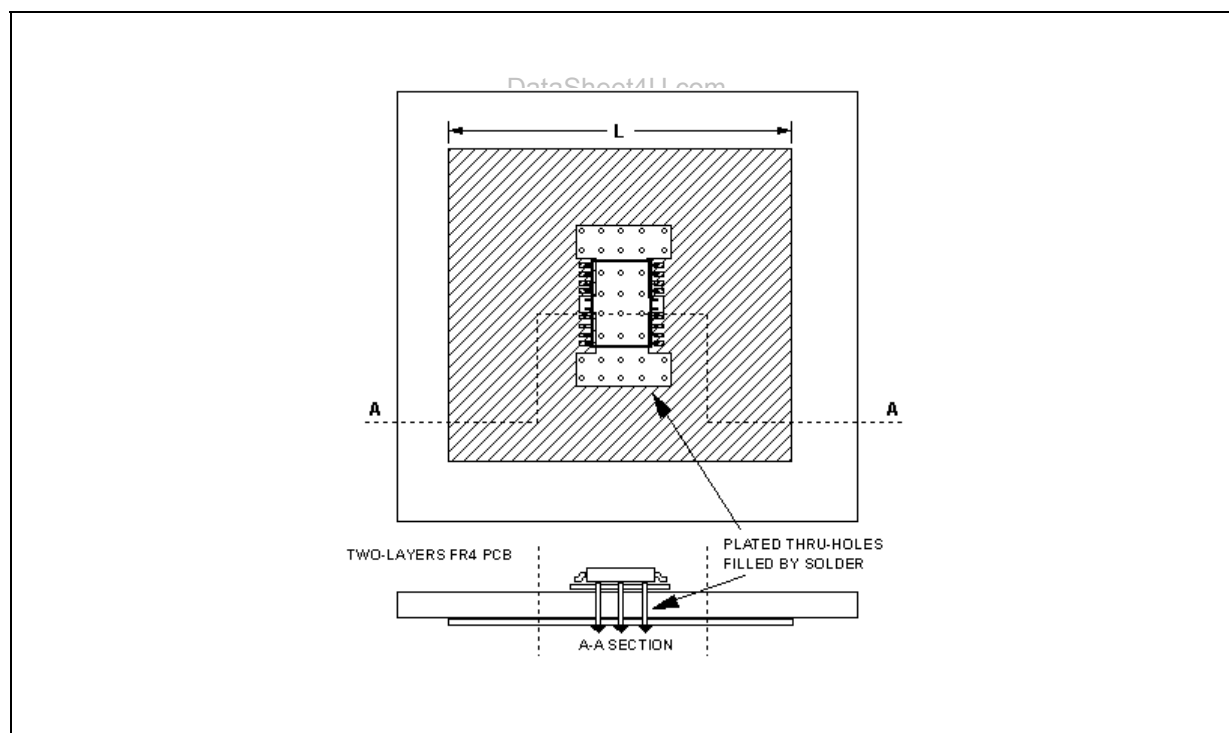
While this can be easily achieved using a through-hole power package that can be attached to a small heatsink or to the metallic frame of the receiver, a surface mount power package must rely on PCB solutions whose thermal efficiency is often limited. The simplest solution is to use a large, continuous copper area of the GND layer to dissipate the heat coming from the IC body.

The SO-20 package of this IC has 4 GND pins that are not just intended for electrical GND connection, but also to provide a low thermal resistance path between the silicon chip and the PCB heatsink. Given an R_{thj-c} equal to 15°C/W, a maximum of 28°C/W are left to the PCB heatsink. This figure is achieved if a minimum of 25cm² copper area is placed just below the IC body. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, an unbroken GND area even on the opposite side where the IC is placed. In both cases, the thermal path between the IC GND pins and the dissipating copper area must exhibit a low thermal resistance.

In figure 4, it is shown a suggested layout for the SO-20 package with a dual layer PCB, where the IC Ground pins and the square dissipating area are thermally connected through 32 vias holes, filled by solder. This arrangement, when $L=50\text{mm}$, achieves an R_{thc-a} of about 28°C/W.

Different layouts are possible, too. Basic principles, however, suggest to keep the IC and its ground pins approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

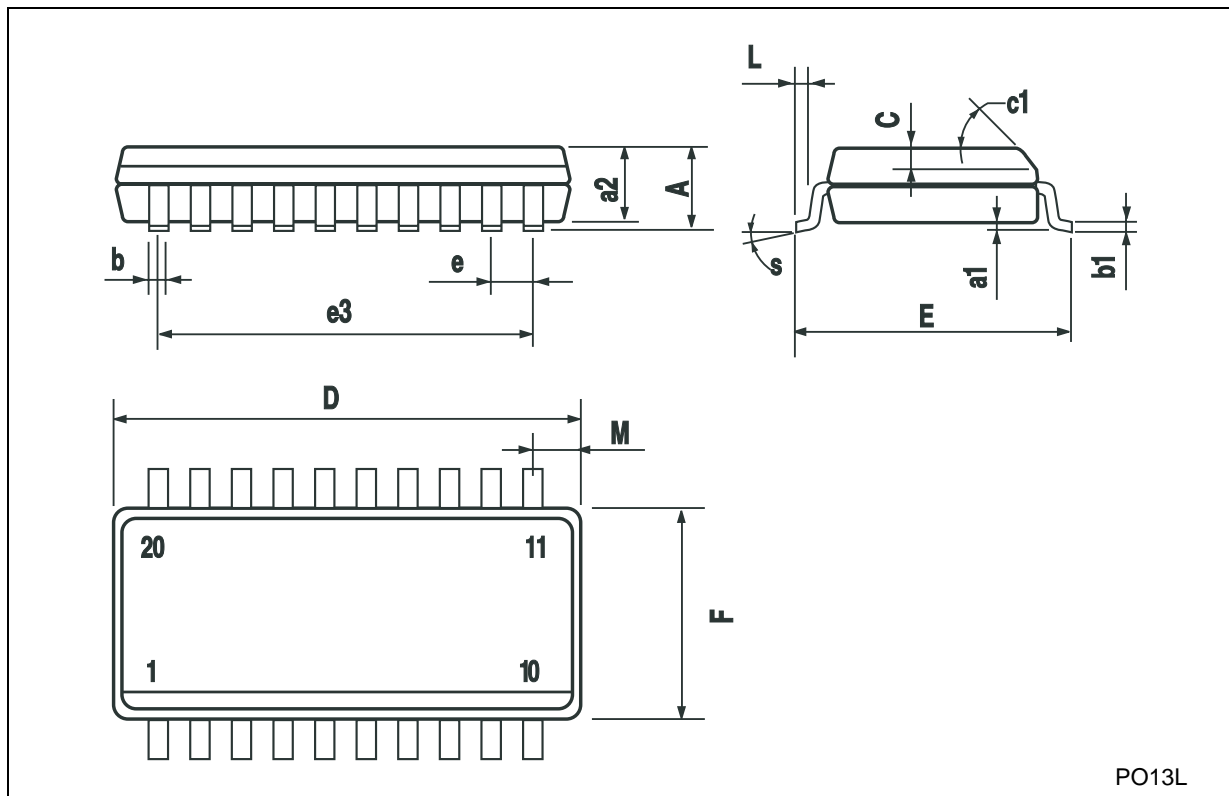
SO-20 SUGGESTED PCB HEATSINK LAYOUT



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SO-20 MECHANICAL DATA

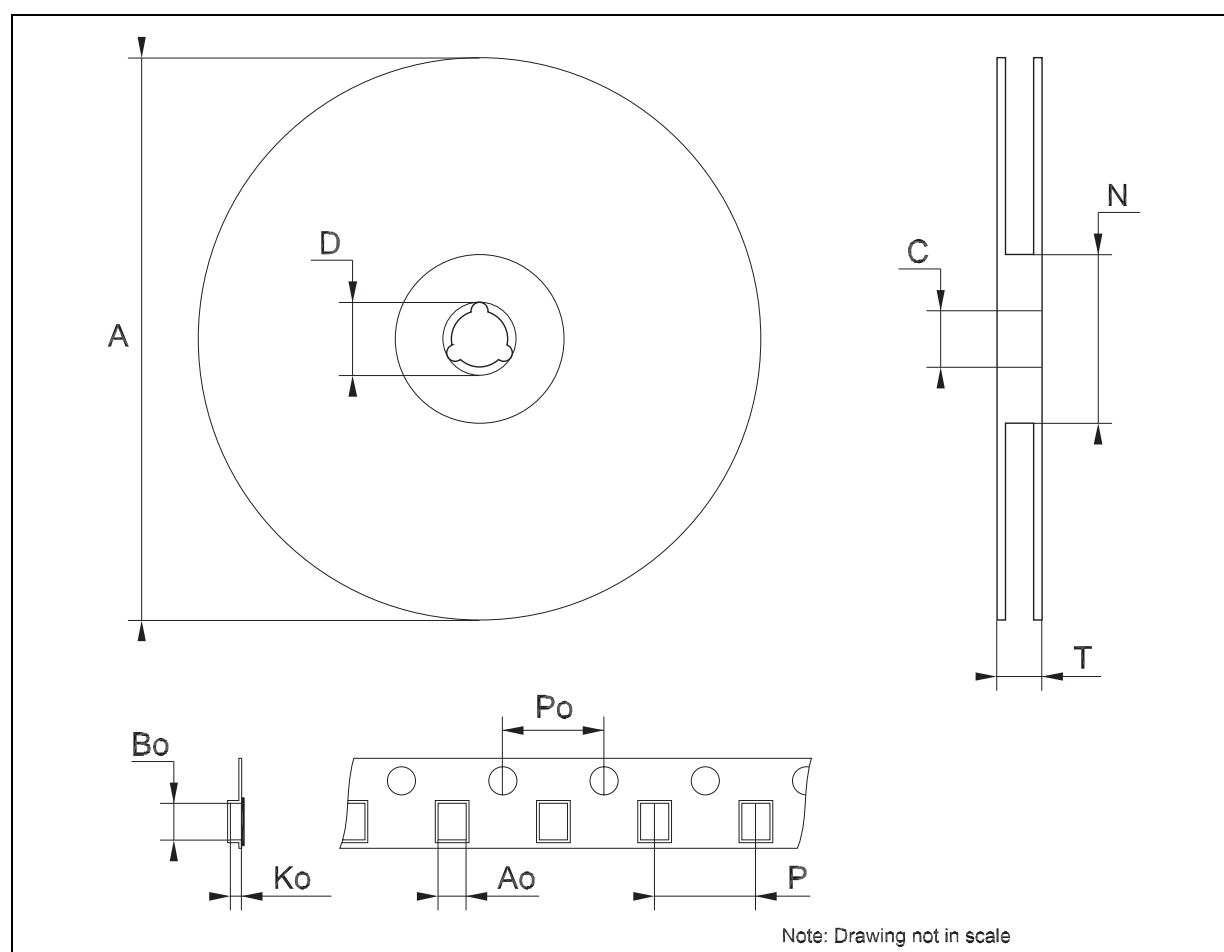
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

Tape & Reel SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



LNBK20D2

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