WM8311

Processor Power Management Subsystem

DESCRIPTION

The WM8311 is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management. It is specifically targeted at the requirements of a range of low-power portable consumer products, but is suitable to any application with a multimedia processor. The WM8311 is designed to operate as a system PMIC supporting a variety of industry-standard processors and accessories in a wide range of consumer multimedia applications.

The start-up behaviour and configuration is fully programmable in an integrated OTP non-volatile memory. This highly flexible solution helps reduce time-to-market, as changing application requirements can be very easily accommodated in the OTP. The InstantConfig™ interface enables an external EEPROM to configure the WM8311.

The WM8311 power management subsystem comprises of four programmable DC-DC converters, seven LDO regulators (one of which is low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

WM8311 can be powered from a battery, a wall adaptor or from a USB power source. An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support ‘Alive’ processor power domains external to the WM8311.

A linear on-chip battery charger supports trickle charging and constant current / constant voltage charging of single-cell lithium-ion / lithium-polymer batteries. The charge current, termination voltage, and charger time-out are programmable. WM8311 detects and handles battery fault conditions with a minimum of system software involvement.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement. The Touch Panel controller uses the same ADC on an interleaved basis.

WM8311 includes a crystal oscillator, an internal RC oscillator and Frequency Locked Loop (FLL) to generate clock signals for autonomous system start-up and processor clocking. A Secure Real-Time Clock (S-RTC) and alarm function is included, capable of system wake-up from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8311 subsystem to be independently powered down through a control interface or alternatively through register and OTP-configurable GPIOs. The device offers a standby power consumption of <10uA, making it particularly suitable for portable applications.

The WM8311 is supplied in a 8x8mm 121-ball BGA package, ideal for use in portable systems. The WM8311 forms part of the Wolfson series of audio and power management solutions.

FEATURES

Power Management

- 2 x DC-DC synchronous buck converters (0.6V - 1.8V, 1.2A, DVS)
- 1 x DC-DC synchronous buck converter (0.85V - 3.4V, 1A)
- 1 x DC-DC boost converter (up to 30V, up to 90mA)
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 100mA, 2Ω)
- 1 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1Ω)
- 1 x ‘Alive’ LDO regulator (0.8V – 1.55V, up to 25mA)

Backlight LED Current Sinks

- 2 x programmable constant current sinks, suitable for multi-LED display backlight control

Battery Charger

- Programmable single-cell lithium-ion / lithium-polymer battery charger (1A max charge current)
- Battery monitoring for temperature and voltage
- Autonomous backup battery charging and switching

System Control

- I^2C or SPI compatible primary control interface
- Interrupt based feedback communication scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection
- Intelligent power path and power source selection
- OTP memory bootstrap configuration function

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- Touch Panel interface controller (4-wire and 5-wire)
- 128-bit pseudo-random unique ID
- Secure Real-Time Clock with wake-up alarm
- 16 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, Frequency Locked Loop, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating power state, battery charger or fault status
- Selectable USB current limiting up to 1.8A (in accordance with USB Battery Charging specification Rev 1.1)

Package Options

- 8x8mm, 121-ball BGA package, 0.65mm ball pitch

APPLICATIONS

- Portable Media Players
- Portable Navigation Devices
- Cellular Handsets
- Electronic Books
- Electronic Gaming Devices

WOLFSON MICROELECTRONICS plc

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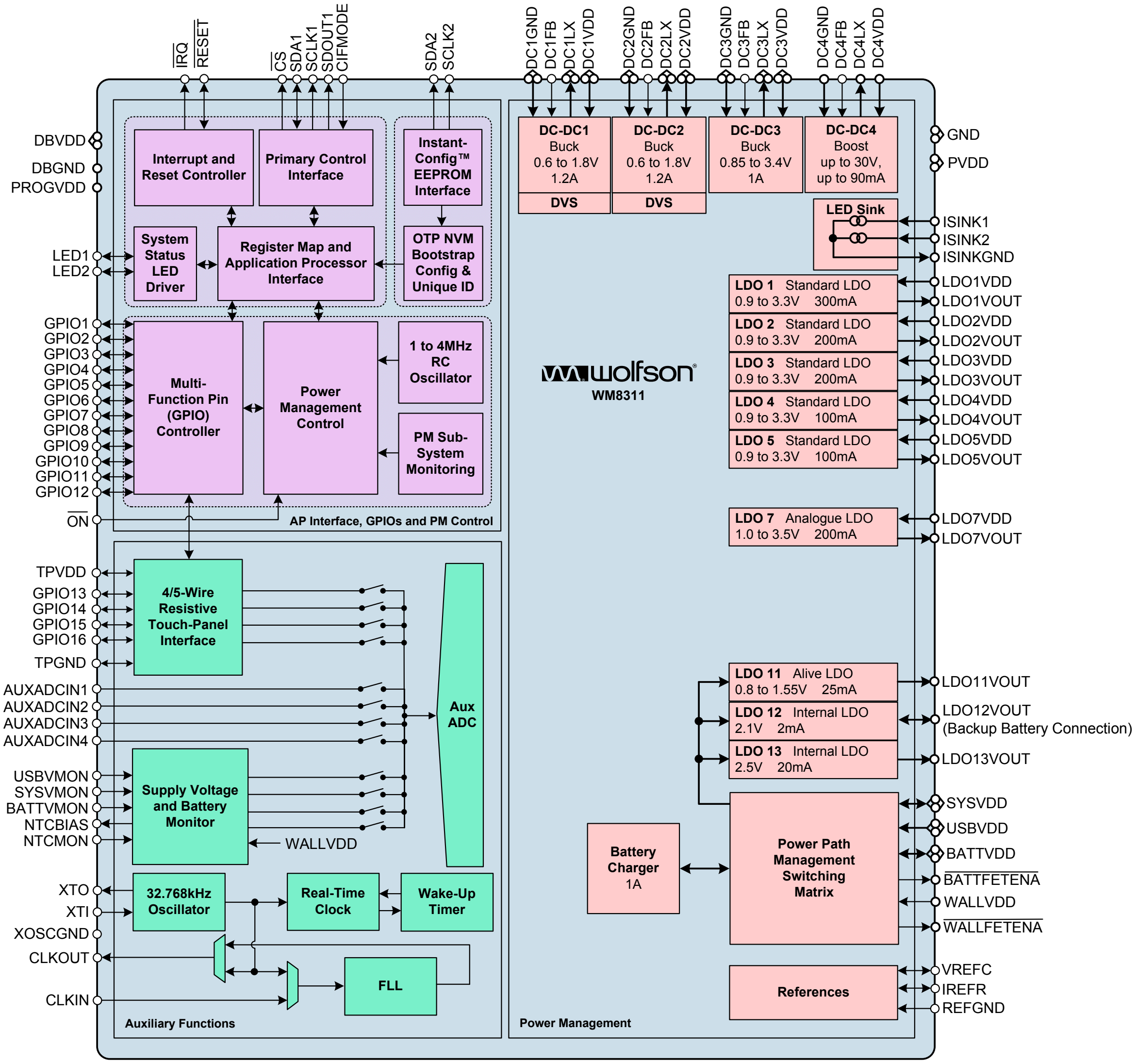
BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8311 is designed as a system PMIC device that manages multiple power supply paths (wall adapter, USB, battery) and generates configurable DC supplies to power processors and associated peripherals within a system. The WM8311 provides three DC-DC synchronous buck (step-down) converters and one DC-DC boost (step-up) converter. Seven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

Two of the DC-DC buck converters incorporate Wolfson's BuckWise™ technology specifically designed to handle rapid changes in load current; programmable slew rate DVS is also provided, as required by modern application processors. Selectable operating modes on all of the DC-DC converters allow each converter to be optimally configured for light, heavy or transient load conditions. Flexible operating configurations allow the converters to be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / bluetooth radio applications.

The WM8311 powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power / standby operation. The power control sequences and many other parameters can be stored in an integrated user-configurable OTP (One-Time Programmable) memory or may be loaded from an external memory. The WM8311 supports the programming and verification of the integrated OTP memory.

The WM8311 provides power path management which seamlessly switches between wall adapter, USB and battery power sources according to the prevailing conditions. A backup power source is also supported in order to maintain the Real Time Clock (RTC) in the absence of any other supplies. The WM8311 provides a configurable battery charger for the main battery, powered from either the wall adapter or USB supplies. The backup power source is maintained using a constant-voltage output from the WM8311.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8311 also provides two LED drivers, which can be controlled manually or configured as status indicators for the OTP memory programmer, operating power state or battery charger.

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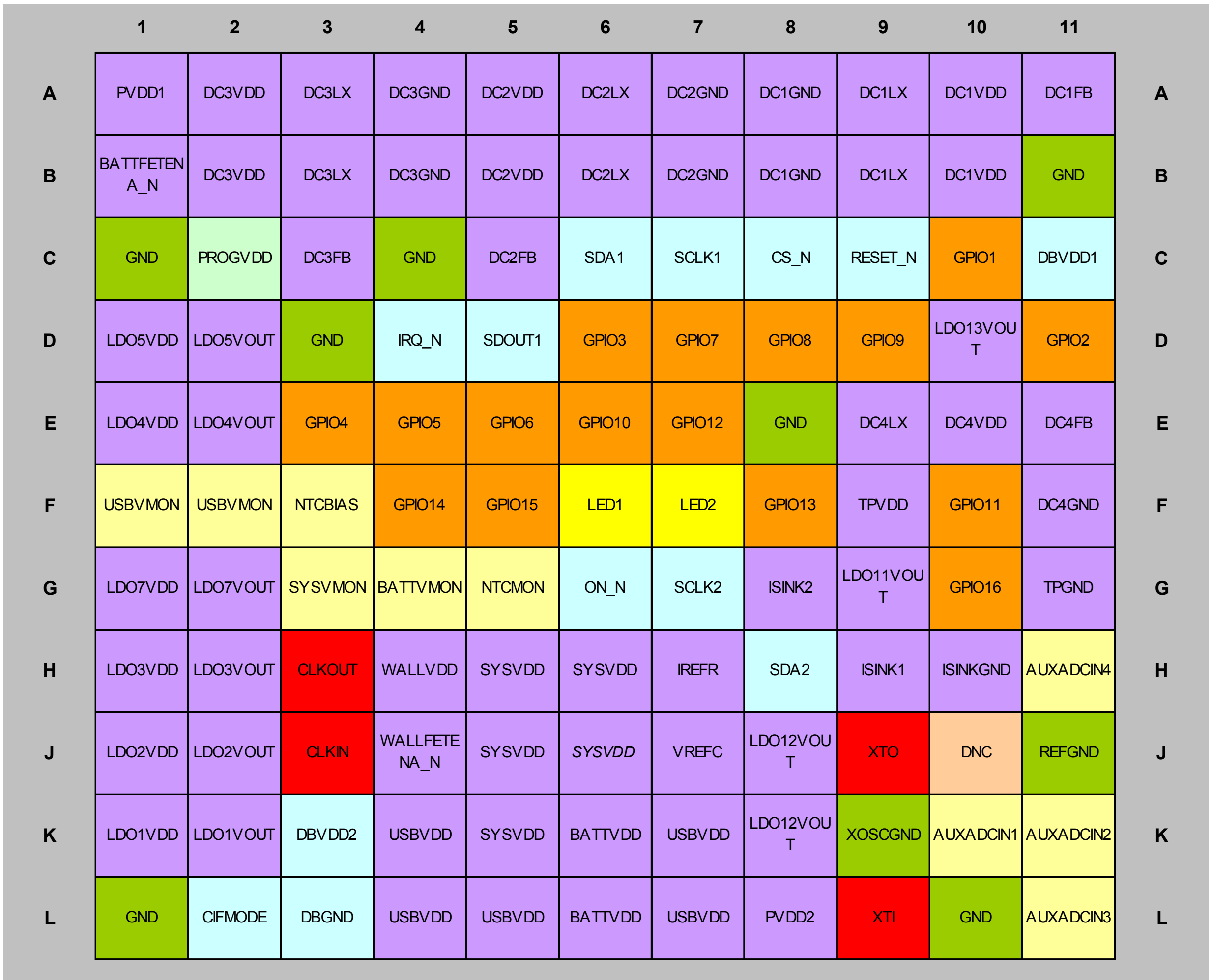
1 PIN CONFIGURATION



	1	2	3	4	5	6	7	8	9	10	11	
A	PVDD1	DC3VDD	DC3LX	DC3GND	DC2VDD	DC2LX	DC2GND	DC1GND	DC1LX	DC1VDD	DC1FB	A
B	BATTFETENA_N	DC3VDD	DC3LX	DC3GND	DC2VDD	DC2LX	DC2GND	DC1GND	DC1LX	DC1VDD	GND	B
C	GND	PROGVDD	DC3FB	GND	DC2FB	SDA1	SCLK1	CS_N	RESET_N	GPIO1	DBVDD1	C
D	LDO5VDD	LDO5VOUT	GND	IRQ_N	SDOUT1	GPIO3	GPIO7	GPIO8	GPIO9	LDO13VOUT	GPIO2	D
E	LDO4VDD	LDO4VOUT	GPIO4	GPIO5	GPIO6	GPIO10	GPIO12	GND	DC4LX	DC4VDD	DC4FB	E
F	USBVMON	USBVMON	NTCBIAS	GPIO14	GPIO15	LED1	LED2	GPIO13	TPVDD	GPIO11	DC4GND	F
G	LDO7VDD	LDO7VOUT	SYSVMON	BATTVMON	NTCMON	ON_N	SCLK2	ISINK2	LDO11VOUT	GPIO16	TPGND	G
H	LDO3VDD	LDO3VOUT	CLKOUT	WALLVDD	SYSVDD	SYSVDD	IREFR	SDA2	ISINK1	ISINKGND	AUXADCIN4	H
J	LDO2VDD	LDO2VOUT	CLKIN	WALLFETENA_N	SYSVDD	*SYSVDD*	VREFC	LDO12VOUT	XTO	DNC	REFGND	J
K	LDO1VDD	LDO1VOUT	DBVDD2	USBVDD	SYSVDD	BATTVDD	USBVDD	LDO12VOUT	XOSCGND	AUXADCIN1	AUXADCIN2	K
L	GND	CIFMODE	DBGND	USBVDD	USBVDD	BATTVDD	USBVDD	PVDD2	XTI	GND	AUXADCIN3	L

8x8 BGA - TOP VIEW (WM8311)

2 ORDERING INFORMATION

ORDER CODE	OTP	TEMPERATURE RANGE (T_A)	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8311GEB/V	Unprogrammed	-40°C to +85°C	121-ball (8 x 8mm) (Pb-free)	MSL3	260°C
WM8311GEB/RV	Unprogrammed	-40°C to +85°C	121-ball (8 x 8mm) (Pb-free, tape and reel)	MSL3	260°C
WM8311GEBxxx/RV*	Custom	-40°C to +85°C	121-ball (8 x 8mm) (Pb-free, tape and reel) **	MSL3	260°C

Note:

Reel quantity = 2200

* xxx = Unique OTP part number

** Custom OTP minimum order quantity 22,000.

3 PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the ‘always-on’ functions internal to the WM8311.
3. Note that an external level-shifter may be required when interfacing between different power domains.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Touch Panel and Auxiliary ADC				
F1, F2	USBVMON	Analogue Input	USBVDD	USBVDD Supply Voltage Monitor
G3	SYSVMON	Analogue Input	SYSVDD	SYSVDD Supply Voltage Monitor
G4	BATTVMON	Analogue Input	BATTVDD	BATTVDD Supply Voltage Monitor
K10	AUXADCIN1	Analogue Input/Output	SYSVDD	Auxiliary Analogue Input 1 / Battery Charge Current Monitor Output
K11	AUXADCIN2	Analogue Input		Auxiliary Analogue Input 2
L11	AUXADCIN3	Analogue Input		Auxiliary Analogue Input 3
H11	AUXADCIN4	Analogue Input	TPVDD	Auxiliary Analogue Input 4
F9	TPVDD	Supply		Touch panel VDD supply
G11	TPGND	Supply		Touch panel Power Ground
Clocking and Real Time Clock				
J9	XTO	Analogue Output	VPMIC	Crystal Drive Output
L9	XTI	Analogue Input		Crystal Drive Input or 32.768kHz CMOS Clock Input
K9	XOSCGND	Supply		Crystal Oscillator Ground
H3	CLKOUT	Digital Output	DBVDD	CMOS Clock Output Configurable Open Drain / CMOS mode. (External 4.7kΩ pull-up recommended in Open Drain mode.)
J3	CLKIN	Digital Input		CMOS FLL Clock Input
General Purpose Input / Output				
C10	GPIO1	Digital I/O	DBVDD or VPMIC	GPIO Pin 1 Selectable pull-up/pull-down.
D11	GPIO2	Digital I/O		GPIO Pin 2 Selectable pull-up/pull-down.
D6	GPIO3	Digital I/O		GPIO Pin 3 Selectable pull-up/pull-down.
E3	GPIO4	Digital I/O	DBVDD or SYSVDD	GPIO Pin 4 Selectable pull-up/pull-down.
E4	GPIO5	Digital I/O		GPIO Pin 5 Selectable pull-up/pull-down.
E5	GPIO6	Digital I/O		GPIO Pin 6 Selectable pull-up/pull-down.
D7	GPIO7	Digital I/O	DBVDD or VPMIC	GPIO Pin 7 Selectable pull-up/pull-down.
D8	GPIO8	Digital I/O		GPIO Pin 8 Selectable pull-up/pull-down.
D9	GPIO9	Digital I/O		GPIO Pin 9 Selectable pull-up/pull-down.
E6	GPIO10	Digital I/O	DBVDD or SYSVDD	GPIO Pin 10 Selectable pull-up/pull-down.
F10	GPIO11	Digital I/O		GPIO Pin 11 Selectable pull-up/pull-down.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
E7	GPIO12	Digital I/O		GPIO Pin 12 Selectable pull-up/pull-down.	
F8	GPIO13	Digital I/O	TPVDD	GPIO Pin 13 / Touch panel interface Selectable GPIO pull-up/pull-down.	
F4	GPIO14	Digital I/O		GPIO Pin 14 / Touch panel interface Selectable GPIO pull-up/pull-down.	
F5	GPIO15	Digital I/O		GPIO Pin 15 / Touch panel interface Selectable GPIO pull-up/pull-down.	
G10	GPIO16	Digital I/O		GPIO Pin 16 / Touch panel interface Selectable GPIO pull-up/pull-down.	
Processor Interface and IC Control					
G6	$\overline{ON}$	Digital Input	VPMIC	ON Request Pin (Internal pull-up)	
C9	$\overline{RESET}$	Digital I/O	DBVDD	System Reset Input and Open Drain Output. (Internal pull-up)	
D4	$\overline{IRQ}$	Digital Output	DBVDD	PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.)	
L2	CIFMODE	Digital Input	DBVDD	Primary Control Interface Mode Select: 0 = I^{2}C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode	
				SPI Compatible Control Interface Mode	*I^{2}C Compatible Control Interface Mode*
D5	SDOUT1	Digital Output	DBVDD	Control Interface Serial Data Out. Open Drain output; external 4.7kΩ pull-up recommended.	No Function
C7	SCLK1	Digital Input		Control Interface Serial Clock	Control Interface Serial Clock
C6	SDA1	Digital I/O		Control Interface Serial Data In	Control Interface Serial Data Input and Open Drain Output. External 4.7kΩ pull-up recommended. (Output can extend above DBVDD domain.)
C8	$\overline{CS}$	Digital Input		Control Interface Chip Select	I^{2}C Address Select: 0 = 68h 1 = 6Ch
G7	SCLK2	Digital I/O	VPMIC	Control Interface Serial Clock for external InstantConfig™ EEPROM (ICE) (Internal pull-down)	
H8	SDA2	Digital I/O		Control Interface Serial Data to/from external InstantConfig™ EEPROM (ICE) (Internal pull-down)	
C11	DBVDD1	Supply		Digital Buffer Supply	
K3	DBVDD2	Supply		Digital Buffer Supply	
L3	DBGND	Supply		Digital Buffer Ground	
OTP Memory					
C2	PROGVDD	Supply		High-voltage input for OTP programming.	

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
DC-DC Converters and LDO Regulators				
B11, C1, C4, D3, E8, L1, L10	GND	Supply		Ground
A1	PVDD1	Supply		Internal VDD supply; Connect to SYSVDD
L8	PVDD2	Supply		
A8, B8	DC1GND	Supply		DC-DC1 Power Ground
A11	DC1FB	Analogue Input	DC1VDD	DC-DC1 Feedback Pin
A9, B9	DC1LX	Analogue I/O		DC-DC1 Inductor Connection
A10, B10	DC1VDD	Supply		DC-DC1 Power Input (connect to SYSVDD supply)
A7, B7	DC2GND	Supply		DC-DC2 Power Ground
C5	DC2FB	Analogue Input	DC2VDD	DC-DC2 Feedback Pin
A6, B6	DC2LX	Analogue I/O		DC-DC2 Inductor Connection
A5, B5	DC2VDD	Supply		DC-DC2 Power Input (connect to SYSVDD supply)
A4, B4	DC3GND	Supply		DC-DC3 Power Ground
C3	DC3FB	Analogue Input	DC3VDD	DC-DC3 Feedback Pin
A3, B3	DC3LX	Analogue I/O		DC-DC3 Inductor Connection
A2, B2	DC3VDD	Supply		DC-DC3 Power Input (connect to SYSVDD supply)
F11	DC4GND	Supply		DC-DC4 Power Ground
E11	DC4FB	Analogue Input	DC4VDD	DC-DC4 Feedback Connection
E9	DC4LX	Analogue I/O		DC-DC4 Inductor Connection
E10	DC4VDD	Supply		DC-DC4 Power Input (connect to SYSVDD supply)
K1	LDO1VDD	Supply		LDO1 Power Input (must be ≤ SYSVDD supply)
K2	LDO1VOUT	Analogue Output	LDO1VDD	LDO1 Power Output
J1	LDO2VDD	Supply		LDO2 Power Input (must be ≤ SYSVDD supply)
J2	LDO2VOUT	Analogue Output	LDO2VDD	LDO2 Power Output
H1	LDO3VDD	Supply		LDO3 Power Input (must be ≤ SYSVDD supply)
H2	LDO3VOUT	Analogue Output	LDO3VDD	LDO3 Power Output
E1	LDO4VDD	Supply		LDO4 Power Input (must be ≤ SYSVDD supply)
E2	LDO4VOUT	Analogue Output	LDO4VDD	LDO4 Power Output
D1	LDO5VDD	Supply		LDO5 Power Input (must be ≤ SYSVDD supply)
D2	LDO5VOUT	Analogue Output	LDO5VDD	LDO5 Power Output
G1	LDO7VDD	Supply		LDO7 Power Input
G2	LDO7VOUT	Analogue Output	LDO7VDD	LDO7 Power Output
G9	LDO11VOUT	Analogue Output	PVDD	LDO11 (Alive) Power Output
J10, K10	LDO12VOUT	Analogue I/O	PVDD	LDO12 (Internal VPMIC) Output; Backup battery supply input / output
D10	LDO13VOUT	Analogue I/O	PVDD	LDO13 (Internal INTVDD) Output; not for general use
Current Sinks				
H9	ISINK1	Analogue Output	SYSVDD	LED String Current Sink 1
G8	ISINK2	Analogue Output		LED String Current Sink 2
H10	ISINKGND	Supply		LED String Current Sink Ground
Voltage and Current References				
J7	VREFC	Analogue I/O	VPMIC	Voltage Reference capacitor connection point
H7	IREFR	Analogue I/O		Current Reference resistor connection point
J11	REFGND	Supply		Reference Ground

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Power Path Management				
H5, H6, J5, J6, K5	SYSVDD	Supply		System VDD Supply
K4, K7, L4, L5, L7	USBVDD	Supply		USB VDD Supply
K6, L6	BATTVDD	Supply		Primary Battery Supply
B1	$\overline{\text{BATTFETENA}}$	Digital Output	PVDD	External Battery FET Driver
H4	WALLVDD	Supply		Wall VDD Supply/Sense
J4	$\overline{\text{WALLFETENA}}$	Digital Output	highest VDD supply	External Wall FET Driver. Power domain is the highest out of WALLVDD, USBVDD or BATTVDD.
F3	NTCBIAS	Analogue Output	VPMIC	Battery NTC Temperature Monitor Supply
G5	NTCMON	Analogue Input		Battery NTC Temperature Monitor Voltage Sense Input
System LED Drivers				
F6	LED1	Digital Output	SYSVDD	Status LED Driver 1. Open Drain Output
F7	LED2	Digital Output		Status LED Driver 2. Open Drain Output
Do Not Connect				
J10	DNC			Do Not Connect

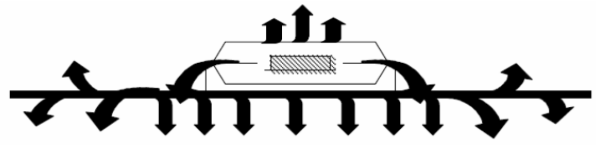
4 THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8311 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (convection and radiation).
- Package bottom to PCB (convection and radiation).
- Package leads to PCB (conduction).

(Note that radiation is not normally significant at the moderate temperatures experienced in typical applications.)



The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated by the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8311, Θ_{JA} = 45°C/W
- The quoted Θ_{JA} is based on testing to the EIA/JEDEC-51-2 test environment (ie. $1ft^3$ box, still air, with specific PCB stack-up and tracking rules). Note that this is not guaranteed to reflect all typical end applications.

The junction temperature T_J is given by $T_J = T_A + T_R$

- T_A, is the ambient temperature.

The worst case conditions are when the WM8311 is operating in a high ambient temperature, and under conditions which cause high power dissipation, such as the DC-DC converters operating at low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could cause the maximum junction temperature of the device to be exceeded. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- P_D = 500mW (example figure)
- Θ_{JA} = 45°C/W
- $T_R = P_D * \Theta_{JA}$ = 22.5°C
- T_A = 85°C (example figure)
- $T_J = T_A + T_R$ = 107.5°C

The minimum and maximum operating junction temperatures for the WM8311 are quoted in Section 5. The maximum junction temperature is 125°C. Therefore, the junction temperature in the above example is within the operating limits of the WM8311.

5 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8311 has been classified as MSL3.

CONDITION	**MIN**	**MAX**
OTP Programming Supply (PROGVDD)	-0.3V	7.0V
BATTVDD, WALLVDD and USBVDD supplies	-0.3V	7.0V
Input voltage for LDO regulators	-0.3V	7.0V
Input voltage for DC-DC converters	-0.3V	7.0V
Digital buffer supply (DBVDD1, DBVDD2)	-0.3V	4.5V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Operating Temperature Range, T_A	-40°C	+85°C
Junction Temperature, T_J	-40°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		45°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

6 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Wall Input power source	WALLVDD	4.3		5.5	V
Battery Input power source	BATTVDD	2.7		5.5	V
USB Input power source	USBVDD	4.3		5.5	V
Digital buffer supply	DBVDD1, DBVDD2	1.71		3.6	V
Touch Panel supply (see note 1)	TPVDD	1.71	2.5	3.6	V
OTP Programming Supply (see note 2)	PROGVDD	6.25	6.5	6.75	V
	LDO12VOUT		3.3		V
Ground	GND, DC1GND, DC2GND, DC3GND, DC4GND, DBGND, TPGND, XOSCGND, REFGND		0		V

Notes:

1. When the Touch Panel Controller is enabled, then TPVDD must be connected to LDO13VOUT (2.5V). The min/max TPVDD conditions noted above do not apply when the Touch Panel Controller is enabled. (Note that, when the Touch Panel is not enabled, TPVDD is the power domain for GPIO pins 13-16.)
2. The OTP Programming Supply PROGVDD should only be present when programming the OTP. At other times, this pin should be left unconnected. The LDO12VOUT must be overdriven by an external supply when programming the OTP. At other times, the voltage at this pin is driven by the internal circuits of the WM8311.

7 ELECTRICAL CHARACTERISTICS

7.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

DC-DC1 and DC-DC2

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, MODE = FCCM$^{(1)}$, T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} = SYSVDD	2.7		5.5	V
Programmable Output Voltage	V_{OUT}	F_{SW} = 2MHz	0.6		1.8	V
		F_{SW} = 4MHz	0.6		1.4	
V_{OUT} Step Size	V_{OUT_STEP}			12.5		mV
V_{OUT} Accuracy	V_{OUT_ACC}	V_{IN} = 2.7V to 5.5V, I_{OUT} = 0mA to 1200mA	-3		3	%
Undervoltage margin		0.6V ≤ V_{OUT} < 0.9V		50		mV
		0.9V ≤ V_{OUT} < 1.3V		80		
		1.3V ≤ V_{OUT} ≤ 1.8V		100		
Overvoltage margin		0.6V ≤ V_{OUT} ≤ 1.8V		100		mV
Output Current	I_{OUT}	FCCM$^{(1)}$ and Auto (CCM/DCM with PS$^{(2)}$) Modes	0		1200	mA
		Hysteretic Mode	0		150	
		LDO Mode	0		10	
P-channel Current Limit	I_{P_LIM}	F_{SW} = 2MHz		1800		mA
		F_{SW} = 4MHz		2000		
Quiescent Current	I_Q	I_{OUT} = 0mA, FCCM$^{(1)}$ and Auto (CCM/DCM with PS$^{(2)}$) Modes (excluding switching losses)		500		µA
		I_{OUT} = 0mA, Hysteretic Mode		70		
		I_{OUT} = 0mA, LDO Mode		25		
Shutdown Current	I_{SD}	DC*m*_ENA = 0		0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = 100mA		140		mΩ
N-channel On Resistance	R_{DSN}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = -100mA		130		mΩ
Switching Frequency	F_{SW}	DC*m*_FREQ = 01		2		MHz
		DC*m*_FREQ = 11		4		

Notes:

1. Forced Continuous Conduction Mode
2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode

DC-DC3

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, MODE = FCCM$^{(1)}$, T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} = SYSVDD	2.7		5.5	V
Programmable Output Voltage	V_{OUT}		0.85$^{(4)}$		3.4	V
V_{OUT} Step Size	V_{OUT_STEP}			25		mV
V_{OUT} Accuracy	V_{OUT_ACC}	V_{IN} = 2.7V to 5.5V, I_{OUT} = 0mA to 1000mA	-4		4	%
Undervoltage margin		0.85V ≤ V_{OUT} ≤ 3.4V		50		mV
Output Current	I_{OUT}	FCCM$^{(1)}$ and Auto (CCM/DCM with PS$^{(2)}$) Modes	0		1000	mA
		Hysteretic Mode, DC3_STNBY_LIM=01	0		200$^{(3)}$	
		LDO Mode	0		10	
P-channel Current Limit	I_{P_LIM}			1600		mA
Quiescent Current	I_Q	I_{OUT} = 0mA, FCCM$^{(1)}$ and Auto (CCM/DCM with PS$^{(2)}$) Modes (excluding switching losses)		330		μA
		I_{OUT} = 0mA, Hysteretic Mode		110		
		I_{OUT} = 0mA, LDO Mode		30		
Shutdown Current	I_{SD}	DC3_ENA = 0		0.01		μA
P-channel On Resistance	R_{DSP}	V_{IN} = V_{GS} = 3.8V, I_{DC3LX} = 100mA		165		mΩ
N-channel On Resistance	R_{DSN}	V_{IN} = V_{GS} = 3.8V, I_{DC3LX} = -100mA		155		mΩ
Switching Frequency	F_{SW}			2		MHz

Notes:

1. Forced Continuous Conduction Mode
2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode
3. The maximum output current in Hysteretic Mode can be adjusted using the DC*m*_STNBY_LIM registers
4. In FCCM mode, the minimum V_{OUT} is 1.2V

7.2 DC-DC STEP UP CONVERTER

DC-DC4

Unless otherwise noted: V_{IN} = 3.8V, T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} = SYSVDD	2.7		5.5	V
Output Voltage	V_{OUT}		6.5		30	V
Load Current	I_{LOAD}	$V_{OUT} \leq 8V$	0		90	mA
		V_{OUT} = 6.5V to 20V	0		40	
		V_{OUT} = 20V to 30V	0		25	
Quiescent Current	I_Q	DC4_ENA=1		330		µA
Shutdown Current	I_{SD}	DC4_ENA=0		0.1	1	µA
N-channel On Resistance	R_{DSN}			150		mΩ
Regulated feedback voltage	V_{ISINKn}			500		mV
Out of regulation level	V_{ISINKn}			440		mV
Overvoltage detection	V_{DC4FB}			500		mV
Switching frequency	F_{SW}			1		MHz
N-channel Current limit	I_{N_LIM}			800		mA

7.3 CURRENT SINKS

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sink Current	I_{ISINKn}	0.3 <= V_{ISINKn} <= SYSVDD	2		28000	µA
Current Accuracy	I_{ISINKn}	I_{ISINKn} =12mA, V_{ISINKn} = 0.5V		TBD		V
Current matching	I_{ISINKn}	I_{ISINKn} =12mA, V_{ISINKn} = 0.5V		TBD		

7.4 LDO REGULATORS

LDO1

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} ≤ SYSVDD	1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		300	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 150mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 300mA		0.015		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =150mA, V_{OUT} > 2.7V		250		mV
		I_{LOAD} =150mA, V_{OUT} 1.8V to 2.7V		300		
		I_{LOAD} =150mA, V_{OUT} < 1.8V		500		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 300mA	I_Q (no load) + 1% of load			
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 150mA, <= 1kHz		53		dB
		I_{LOAD} = 150mA, 10kHz		53		
		I_{LOAD} = 150mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		1.5		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		1.2		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		0.85		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		0.7		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		600		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO2, LDO3

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} ≤ SYSVDD	1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 100mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 200mA		0.015		%/mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} > 2.7V		200		mV
		I_{LOAD} =100mA, V_{OUT} 1.8V to 2.7V		250		
		I_{LOAD} =100mA, V_{OUT} < 1.8V		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 200mA	I_Q (no load) + 1% of load			
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 100mA, <= 1kHz		55		dB
		I_{LOAD} = 100mA, 10kHz		55		
		I_{LOAD} = 100mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		1.5		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		1.2		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		0.85		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		0.7		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		400		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO4, LDO5

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} ≤ SYSVDD	1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		100	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 50mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 100mA		0.025		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} > 2.7V		200		mV
		I_{LOAD} =100mA, V_{OUT} 1.8V to 2.7V		250		
		I_{LOAD} =100mA, V_{OUT} < 1.8V		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 100mA	I_Q (no load) + 1% of load			
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 50mA, <= 1kHz		55		dB
		I_{LOAD} = 50mA, 10kHz		55		
		I_{LOAD} = 50mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		3.2		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		2.1		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		1.35		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		1.1		

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		230		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO7

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.71		5.5	V
Programmable Output Voltage	V_{OUT}		1.0		3.5	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 1.0V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.5V		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low Power mode	0		50	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-2.5		+2.5	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 100mA Note that V_{IN} must be >= 1.71V		0.025		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 200mA		0.003		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} =1.8V		95		mV
		I_{LOAD} =100mA, V_{OUT} =2.5V		65		
		I_{LOAD} =100mA, V_{OUT} =3.3V		60		
Undervoltage level	V_{OUT}	V_{OUT} Falling		93		%
Quiescent Current	I_Q	Normal mode, no load		110		µA
		Low Power mode, no load		70		
		I_{LOAD} = 1mA to 200mA	I_Q (no load) + 0.1% of load			
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 100mA, <= 1kHz		70		dB
		I_{LOAD} = 100mA, 10kHz		67		
		I_{LOAD} = 100mA, 100kHz		48		
Output noise voltage	V_{OUT}	f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 1mA		30		μV_{RMS}
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 10mA		32		
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 100mA		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.71V, I_{LOAD} = 100mA		550		mΩ
		V_{IN} = 1.8V, I_{LOAD} = 100mA		500		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		330		
		V_{IN} = 3.5V, I_{LOAD} = 100mA		250		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		320		mA
Start-up time	t_{start_up}	No load, Output cap 4.7 µF, 90% of V_{OUT}		50		µs
Shutdown time	t_{shut_down}	No load, Output cap 4.7 µF, 10% of V_{OUT}			10	ms

LDO11

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Output Voltage	V_{OUT}		0.8		1.55	V
V_{OUT} Step Size	V_{OUT_STEP}			50		mV
Output Current	I_{OUT}	SYSVDD < 3.1V	0		10	mA
		SYSVDD ≥ 3.1V	0		25	
V_{OUT} Accuracy	V_{OUT}	V_{IN} = 2.7 to 5.5V ; I_{LOAD} = 100µA	-4		+4	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7 to 5.5V; I_{LOAD} = 1mA		0.4		%/V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} = 100µA to 10mA		0.2		%/mA
Quiescent Current	I_Q	No load		2.5		µA
Start-up time	t_{start_up}	No load, Output cap 0.1 µF, 90% of V_{OUT}		0.3	1	ms
Shutdown time	t_{shut_down}	No load, Output cap 0.1 µF, 10% of V_{OUT}		0.3	1	ms

7.5 RESET THRESHOLDS

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power On Reset						
Power on Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between NO POWER and BACKUP states	$V_{POR,\ DE\text{-}ASSERT}$	VPMIC rising		1.18		V
	$V_{POR,\ ASSERT}$	VPMIC falling		1.08		V
Power on Reset hysteresis	$V_{POR,\ HYST}$			100		mV
Device Reset Control						
Device Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between BACKUP and OFF states	$V_{RES,\ DE\text{-}ASSERT}$	VPMIC rising		1.94		V
	$V_{RES,\ ASSERT}$	VPMIC falling		1.85		V
Device Reset hysteresis	$V_{RES,\ HYST}$			92		mV
Device Shutdown						
Shutdown threshold SYSVDD voltage at which the device forces an OFF transition	$V_{SHUTDOWN}$	SYSVDD falling		2.7		V
SYSLO threshold accuracy SYSVDD voltage at which SYSLO is asserted	V_{SYSLO}	SYSVDD falling, V_{SYSLO} set by SYSLO_THR (2.8V to 3.5V)	-3.5		+3.5	%
SYSOK threshold accuracy SYSVDD voltage at which SYSOK is asserted.	V_{SYSOK}	SYSVDD rising, V_{SYSOK} set by SYSOK_THR (2.8V to 3.5V) Note the SYSOK hysteresis margin ($V_{SYSOK,\ HYST}$) is added to SYSOK_THR.	-3.5		+3.5	%
SYSOK hysteresis	$V_{SYSOK,\ HYST}$			40		mV

7.6 REFERENCES

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Reference	V_{VREFC}			0.8		V
Current Reference	V_{IREFR}	100kΩ to REFGND		0.5		V

7.7 BATTERY CHARGER

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
Supply voltage (Voltage required to commence charging; note that charging can continue at lower supply voltages, eg. under current throttling conditions)	V_{SYSVDD}		4.3		5.5	V
Target voltage	V_{BATT_TGT}	CHG_VSEL = 00	4.0	4.05	4.1	V
		CHG_VSEL = 01	4.05	4.10	4.15	
		CHG_VSEL = 10	4.1	4.15	4.2	
		CHG_VSEL = 11	4.15	4.20	4.25	
Charger re-start threshold (Trickle charging starts when battery voltage is below this threshold)	V_{BATT_RSTRT}			V_{BATT_TGT} - 100mV		V
Defective battery threshold	V_{BATT_DEF}			2.85		V
Defective battery timeout	t_{BATT_DEF}			30		mins
Overvoltage threshold	V_{BATT_OV}			4.5		V
End of Charge Current	I_{EOC}	Set by CHG_ITERM		20 to 90		mA
Maximum trickle charge current	I_{TRKL_LIM}	Set by CHG_TRKL_ILIM		50 to 200		mA
Fast charge threshold (Fast charging fast-charge is only possible when battery voltage is above this threshold)	V_{FAST_CHG}			2.85		V
Maximum fast charge current	I_{FAST_LIM}	Set by CHG_FAST_ILIM		50 to 1000		mA
Supply voltage regulation level (Current throttling is applied if supply drops to this level)	V_{SYS_REG}					
Internal Battery FET 'On' Resistance	R_{CHG_SW}	$V_{BATTVDD}$ = 3.8V		90		mΩ
		$V_{BATTVDD}$ = 3.3V		100		
Battery Temperature Monitoring						
Battery temperature monitor source (NTCBIAS)	$V_{NTCBIAS}$			2.1		V
NTCMON voltage for high battery temperature detection	V_{BTEMP_H}	V_{NTCMON} falling		$0.344 \times V_{NTCBIAS}$		V
		V_{NTCMON} rising		$0.365 \times V_{NTCBIAS}$		
NTCMON voltage for low battery temperature detection	V_{BTEMP_L}	V_{NTCMON} rising		$0.767 \times V_{NTCBIAS}$		V
		V_{NTCMON} falling		$0.743 \times V_{NTCBIAS}$		
NTCMON voltage for 'no NTC' detection	V_{NO_NTC}	V_{NTCMON} rising		$0.961 \times V_{NTCBIAS}$		V
		V_{NTCMON} falling		$0.931 \times V_{NTCBIAS}$		

7.8 USB POWER CONTROL

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	V_{USBVDD}		4.3		5.5	V
USB FET ‘On’ Resistance	R_{USB_SW}	USB_ILIM = 010		230		mΩ
		USB_ILIM = 011 or greater		96		
Current limit	I_{USBVDD}	USB_ILIM = 010		91	100	mA
		USB_ILIM = 011		454	500	
		USB_ILIM = 100		805	900	
		USB_ILIM = 101		1343	1500	
		USB_ILIM = 110		1609	1800	
		USB_ILIM = 111		496	550	
Current limit response time				10		µs

7.9 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO1, GPIO2, GPIO3, GPIO7, GPIO8, GPIO9						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.25 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1		180		kΩ
Pull-down resistance	R_{PD}			180		kΩ
GPIO4, GPIO5, GPIO6, GPIO10, GPIO11, GPIO12						
Input HIGH Level	V_{IH}		0.85 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1 and SYSVDD=3.8V		180		kΩ
Pull-down resistance	R_{PD}			180		kΩ
GPIO13, GPIO14, GPIO15, GPIO16						
Input HIGH Level	V_{IH}		0.75 x TPVDD			V
Input LOW Level	V_{IL}				0.25 x TPVDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x TPVDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x TPVDD	V
Pull-up resistance to TPVDD	R_{PU}	TPVDD=1.8V		180		kΩ
Pull-down resistance	R_{PD}	TPVDD=1.8V		180		kΩ

Notes:

1. ‘VDD’ is the voltage of the applicable power domain for each pin (selected by the corresponding GPn_PWR_DOM register).
2. Pull-up / pull-down resistance only applies when enabled using the GPn_PULL registers.
3. Pull-up / pull-down resistors are disabled when the GPIO pin is tri-stated.
4. Pull-up / pull-down resistance may change with the applicable power domain (as selected by GPn_PWR_DOM).

7.10 DIGITAL INTERFACES

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{ON}}$, $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, CIFMODE, SDOUT1, SCLK1, SDA1, $\overline{\text{CS}}$, SCLK2, SDA2						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
'VDD' is the voltage of the applicable power domain for each pin, as defined in Section 3.						
ON pin pull-up resistance	R_{PU}			140		kΩ
RESET pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		kΩ
		DBVDD=3.6V		85		
IRQ pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		kΩ
		DBVDD=3.6V		85		
SCLK2 pin pull-down resistance	R_{PD}			100		kΩ
SDA2 pin pull-down resistance	R_{PD}			100		kΩ

7.11 AUXILIARY ADC

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input resistance	$R_{AUXADCINn}$	During measurement		400		kΩ
Input voltage range	$V_{AUXADCIN1, 2, 3}$		0		V_{SYSVDD}	V
	$V_{AUXADCIN4}$		0		V_{TPVDD}	
Input capacitance	$C_{AUXADCINn}$			2		pF
AUXADC Resolution				12		bits
AUXADC Conversion Time				39		μs
AUXADC accuracy		Input voltage = 3V	-2.5		+2.5	%

7.12 TOUCH PANEL CONTROLLER

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	V_{SYSVDD}	TPVDD connected to LDO13VOUT		2.5		V
Input voltage range	$V_{GPIO13, 14, 15, 16}$ $V_{AUXADCIN4}$		0		V_{TPVDD}	V
Programmable pull-up resistor	R_{PU}	TCH_RPU = 0000		64		kΩ
		TCH_RPU = 0111		8		
		TCH_RPU = 1111		4		
Pen down detection threshold	V_{PDD_THR}			TPVDD/2		V
Pressure measurement current (4-wire mode only)	I_{TCH_PRESS}	TCH_ISEL = 0		200		µA
		TCH_ISEL = 1		400		
Switch matrix internal impedance	R_{TCH_SW}			12		Ω
ADC Resolution				12		bits
ADC Conversion Time (including default settling time)		TCH_DELAY = 010		160		µs
ADC accuracy			-2.5		+2.5	%

7.13 SYSTEM STATUS LED DRIVERS

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED1 and LED2						
Sink current				10		mA

7.14 CLOCKING

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLL input reference	32.768kHz	FLL_CLK_SRC=00		32.768		kHz
	CLKIN	FLL_CLK_SRC=01	32		25000	kHz
FLL output frequency	CLKOUT	CLKOUT_SRC=0	32		25000	kHz

8 TYPICAL POWER CONSUMPTION

Data to follow

9 TYPICAL PERFORMANCE DATA

9.1 DC-DC CONVERTERS

Data to follow

9.2 LDO REGULATORS

Data to follow

10 SIGNAL TIMING REQUIREMENTS

10.1 CONTROL INTERFACE

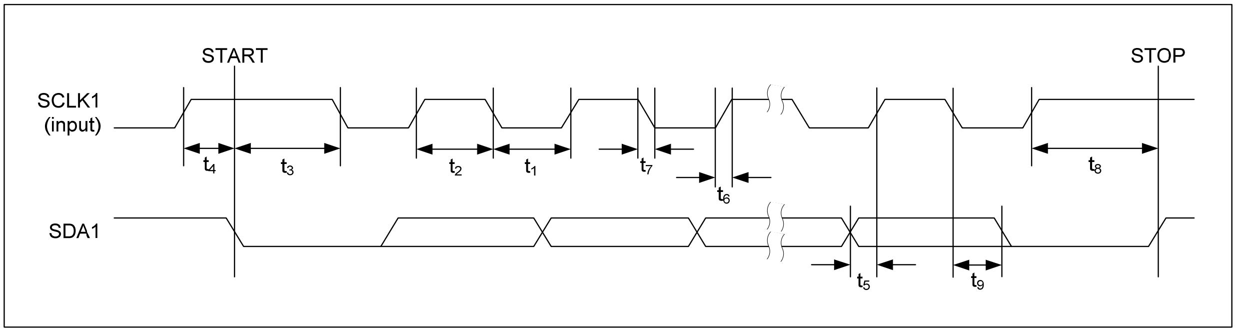


Figure 1 Control Interface Timing - 2-wire (I2C) Control Mode

Test Conditions

T_J = -40ºC to +125 ºC unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK1 Frequency		0		400	kHz
SCLK1 Low Pulse-Width	t_1	1300			ns
SCLK1 High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA1, SCLK1 Rise Time	t_6			300	ns
SDA1, SCLK1 Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

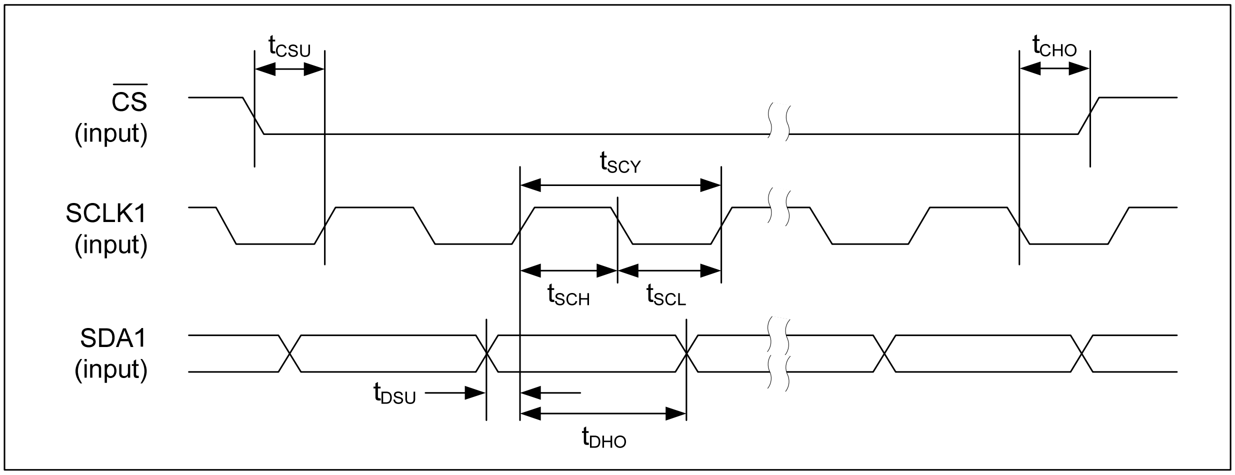


Figure 2 Control Interface Timing - 4-wire (SPI) Control Mode (Write Cycle)

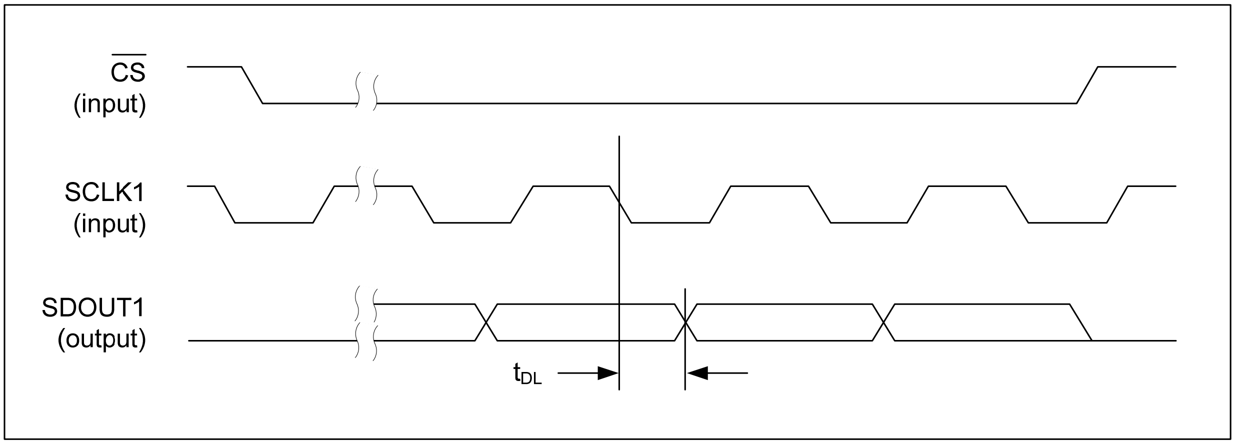


Figure 3 Control Interface Timing - 4-wire (SPI) Control Mode (Read Cycle)

Test Conditions

T_J = -40ºC to +125 ºC unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
$\overline{CS}$ falling edge to SCLK1 rising edge	t_{CSU}	40			ns
SCLK1 falling edge to $\overline{CS}$ rising edge	t_{CHO}	10			ns
SCLK1 pulse cycle time	t_{SCY}	200			ns
SCLK1 pulse width low	t_{SCL}	80			ns
SCLK1 pulse width high	t_{SCH}	80			ns
SDA1 to SCLK1 set-up time	t_{DSU}	40			ns
SDA1 to SCLK1 hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK1 falling edge to SDOUT1 transition	t_{DL}			40	ns

The $\overline{CS}$ pin must be held high for at least 1µs after every register write operation in SPI mode.

11 DEVICE DESCRIPTION

11.1 GENERAL DESCRIPTION

The WM8311 is a multi-purpose Power Management device with a comprehensive range of features. The WM8311 provides 4 DC-DC converters and 7 LDO regulators which are all programmable to application-specific requirements. The on-board oscillator and two additional LDOs support the clocking and control functions for the DC-DC converters and other core functions. The device has flexible power supply options, which enable hot-switching between external supplies (Wall adaptor or USB), or a battery. The WM8311 provides a configurable charger for the main battery and maintains the backup power source using a constant-voltage output. Other features include 2 Current Sinks (LED drivers), flexible GPIO capability, touch panel controller interface and LED outputs for system status indications.

The WM8311 also provides a 32.768kHz crystal oscillator and secure Real Time Clock (SRTC). The Frequency Locked Loop (FLL) enables different clock frequencies to be generated from the 32kHz reference to provide clocking for external circuits. An auxiliary ADC is included, for measurement of internal and external voltages

Under typical operating conditions, the device is powered up and shut down under the control of the $\overline{\text{ON}}$ pin. The device executes a programmable sequence of enabling or disabling the DC-DC converters, LDOs and other functions when commanded to power up or shut down respectively. An alternate device state (SLEEP power state) is provided, in which selected functions may be separately configured for a low-power or other operating condition. The configuration of the normal operating state may be programmed into an integrated OTP non-volatile memory. If desired, the OTP memory can be programmed during device manufacture in accordance with the user's specification. See Section 14 for details of the OTP and associated bootstrap configuration functions.

In the absence of suitable power supplies, the WM8311 automatically reverts to a backup state, under which a minimal functionality is maintained to enable a smooth return to normal operation when the supplies are restored. With a backup supply present, the RTC is updated in the backup state, allowing the main battery to be depleted or changed without loss of RTC function. Without a backup battery, a small capacitor is sufficient to maintain the RTC (unclocked) for up to 5 minutes.

11.2 POWER STATES

The WM8311 has 6 main power states, which are described below. Different levels of functionality are associated with each of the power states. Some of the state transitions are made autonomously by the WM8311 (eg. transitions to/from BACKUP are scheduled according to the available power supply conditions). Other transitions are initiated as a result of instructions issued over the Control Interface or as a result of software functions (eg. Watchdog timer) or hardware functions such as the $\overline{\text{ON}}$ pin. The valid transitions and the associated conditions are detailed below.

NO POWER - This is the device state when no power is available. All functions are disabled and all register data is lost.

OFF - This is the device state when power is available but the device is switched off. The RTC is enabled and the register map contents are maintained. The $\overline{\text{RESET}}$ pin is pulled low in this state. LDO11 may optionally be enabled in this state; all other DC-DCs and LDOs are disabled (except LDO12, which supports internal functions).

ON - This is the normal operating state when the device is switched on. All device functions are available in this state.

SLEEP - This is a user-configurable operating state which is intended for a low-power operating condition. Selected functions may be enabled, disabled or re-configured according to the user's requirements. A programmable configuration sequence for the DC-DCs and LDOs is executed on transition to/from SLEEP mode.

BACKUP - This is the operating state when the available power supplies are below the reset threshold of the device. Typically, this means that USB or Wall supplies are not present and that the main battery is either discharged or removed. All DC-DC converters and LDO regulators are disabled in this state. The RTC and oscillator and a 'software scratch' memory area can be maintained from the backup supply (if available) in this state. All other functions and registers are reset in BACKUP. (Note that, for power saving, an 'unclocked' mode, in which the RTC is held constant, may be selected if required.)

PROGRAM - This is a special operating state which is used for programming the integrated OTP memory with the device configuration data. The settings stored in the OTP define the device configuration in the ON state, and also the time/sequencing data associated with ON/OFF power state transitions. See Section 14 for details of the OTP features.

The valid power state transitions are illustrated in Figure 4.

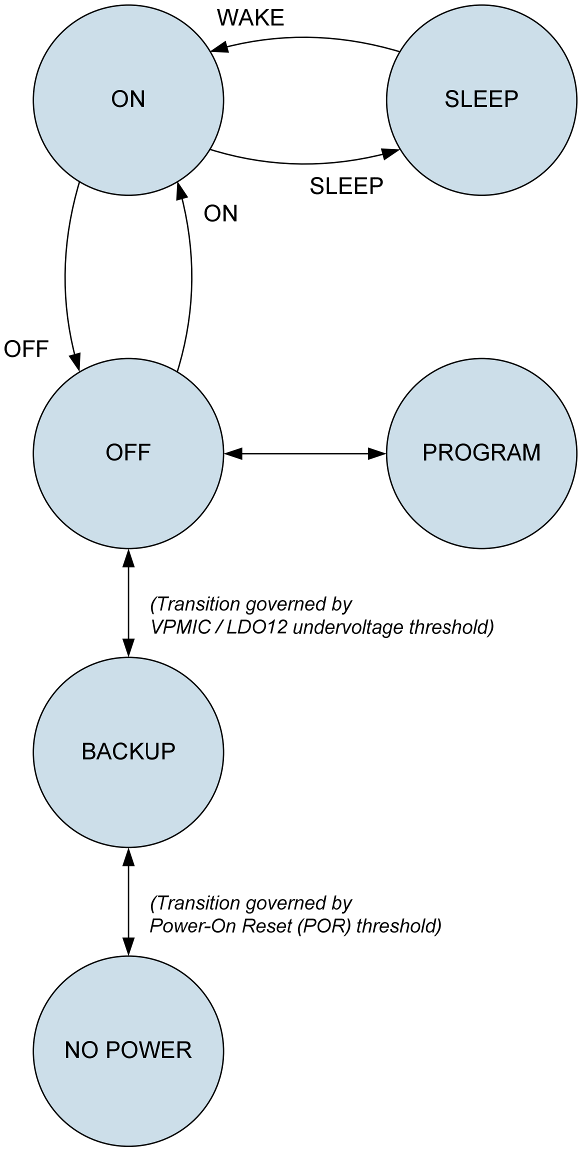


Figure 4 Power States and Transitions

State transitions to/from the NO POWER state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the NO POWER state when this voltage is below the Power-On Reset (POR) threshold. See Section 24 for more details on Power-On Reset.

State transitions to/from the BACKUP state are controlled automatically by the internal supply (VPMIC) voltage generated by LDO12. The device is in the BACKUP state when this voltage is below the Device Reset threshold. See Section 24 for more details on Resets.

State transitions to/from the PROGRAM state are required to follow specific control sequences. See Section 14 for details of the PROGRAM functions.

The remaining transitions between the OFF, ON and SLEEP states may be initiated by a number of different mechanisms - some of them automatic, some of them user-controlled. Transitions between these states are time-controlled sequences of events. These are the OFF, ON, SLEEP and WAKE sequences shown in Figure 4. These transitions are programmable, using data stored in the integrated OTP memory or else data loaded from an external InstantConfig™ EEPROM (ICE) memory. See Section 14 for details.

Note that a transition from the SLEEP state to the OFF state is not a controlled transition. If an 'OFF' event occurs whilst in the SLEEP state, then the WM8311 will select the OFF state, but all the enabled converters and regulators will be disabled immediately; the time-controlled sequence is not implemented in this case. See Section 11.3 for details of the WM8311 'OFF' events.

The current power state of the WM8311 can be read from the MAIN_STATE register field. A restricted definition of this field is shown in Table 1. Note that other values of MAIN_STATE are defined for transition states, but it is recommended that only the values quoted below should be used to confirm power state transitions.

A power state transition to the BACKUP, SLEEP, ON or OFF state is indicated by the Interrupt bits described in Section 11.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16397 (400Dh) System Status	4:0	MAIN_STATE [4:0]	0_0000	Main State Machine condition 0_0000 = OFF 0_1011 = PROGRAM 1_1100 = SLEEP 1_1111 = ACTIVE (ON)

Table 1 Power State Readback

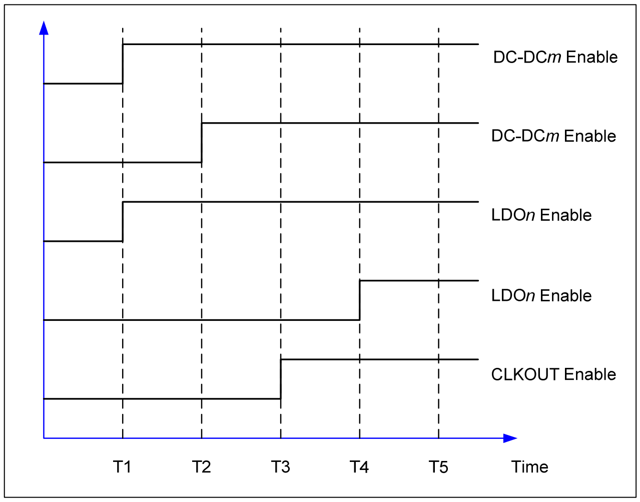
11.3 POWER STATE CONTROL

The OFF, ON, SLEEP and WAKE sequences are initiated by many different conditions. When such a condition occurs, the WM8311 schedules a series of 5 timeslots, enabling a sequence of enable/disable events to be controlled. The nominal duration of the timeslots is fixed at 2ms, though this may be extended if any selected circuit has not started up within this time, as described later in this section. The OFF, SLEEP and WAKE sequences commence after a programmable delay set by PWRSTATE_DLY. This allows a host processor to request a WM8311 state transition and then complete other tasks before the transition actually occurs.

The ON sequence is the transition from OFF to ON power states. Each LDO and each DC-DC Converter (except DC-DC4) may be associated with any one of the available timeslots in the ON sequence. This determines the time, within the sequence, at which that DC-DC Converter or LDO will be enabled following an 'ON' event.

The clock output (CLKOUT) and GPIO pins configured as External Power Enable (EPE) outputs can also be associated with any one of the available timeslots in the ON sequence. The EPE function is a logic output that may be used to control external circuits, including external DC-DC converters.

An example 'ON' state transition sequence is illustrated in Figure 5. Each of the DC-DC Buck Converters and LDO Regulators can be individually assigned to one of the five timeslots (shown as T1, T2, T3, T4, T5), providing total flexibility in the power sequence.



Note that only 4 Power Management functions are illustrated. However, individual control is possible for all of the DC-DC (Buck) Converters and all of the LDO Regulators.
The CLKOUT signal can also be associated with a timeslot in the ON sequence, as illustrated.

The nominal time delay between each of the timeslots is 2ms. This time is extended if necessary to ensure any Undervoltage conditions have cleared before the sequence continues.

Figure 5 Example Control Sequence for 'ON' state transition

The possible 'ON' events that may trigger the ON sequence are listed in Table 3. The ON sequence is only permitted when the supply voltage SYSVDD exceeds a programmable threshold SYSOK. See Section 24 for details of SYSVDD voltage monitoring.

The OFF sequence is the reverse of the ON sequence. Each DC-DC Converter, LDO Regulator or GPIO output that is associated with a timeslot in the ON sequence is switched off in the reverse sequence following an 'OFF' event. If CLKOUT is assigned to a timeslot in the ON sequence, then this is disabled in the reverse (OFF) sequence also.

The possible 'OFF' events are listed in Table 3. Note that it is possible to modify the OFF sequence by writing to the associated registers in the ON power state if required; this allows the OFF sequence to be independent of the ON sequence.

The SLEEP sequence is the transition from ON to SLEEP power states. Each LDO and each DC-DC Converter (except DC-DC4) may be associated with any one of the available timeslots in the SLEEP sequence. This determines the time, within the sequence, at which that DC Converter or LDO will be disabled following a 'SLEEP' event.

The clock output (CLKOUT) and GPIO pins configured as External Power Enable (EPE) outputs can also be associated with any one of the available timeslots in the SLEEP sequence. The possible 'SLEEP' events are listed in Table 3.

The WAKE sequence is the reverse of the SLEEP sequence. Each DC-DC Converter, LDO Regulator or GPIO output that is associated with a timeslot in the SLEEP sequence is switched on in the reverse sequence following a 'WAKE' event. If CLKOUT is assigned to a timeslot in the SLEEP sequence, then this is disabled in the reverse (WAKE) sequence also.

The possible 'WAKE' events are listed in Table 3. Note that it is possible to modify the WAKE sequence by writing to the associated registers in the SLEEP power state if required; this allows the WAKE sequence to be independent of the SLEEP sequence.

Any DC-DC Converter or LDO that is not associated with one of the 5 timeslots in the ON sequence may, instead, be configured to be hardware controlled via a GPIO pin configured as one of the Hardware Enable inputs. See Section 21 for details of the GPIO functions. Any DC-DC Converter or LDO that is not under Hardware control may be enabled or disabled under Software control in the ON state, regardless of whether it is associated with any timeslot in the ON sequence.

When a valid OFF event occurs, any DC-DC Converter or LDO which is not allocated a timeslot in the ON sequence is disabled immediately. This includes any DC-DC Converter or LDO which is under GPIO (Hardware Enable) control. The only exception is LDO11 which may, optionally, be configured to be enabled in the OFF state.

The WM8311 monitors the DC-DC Converters and LDOs during the ON sequence to ensure that the required circuits have powered up successfully before proceeding to the next timeslot. The nominal timeslot durations are extended if necessary in order to wait for the selected DC-DC Converters or LDOs to power up. If the ON sequence has not completed within 2 seconds of starting the transition, then a Power Sequence Failure has occurred, resulting in the OFF state being forced.

Note that, when the OFF state is forced as a result of a Power Sequence failure, all converters and regulators will be shut down. The shutdown sequence is not controlled in this case; all enabled converters and regulators will be disabled immediately on detection of a Power Sequence failure.

The most recent ON or WAKE event can be determined by reading the bits in the “ON Source” register, R400Eh. The most recent OFF event can be determined by reading the bits in the “OFF Source” register, R400Fh.

The “ON Source” register is updated when a new ON event occurs. The “OFF Source” register is updated when a new OFF event occurs. Note that some Reset conditions (see Section 24) result in an OFF transition followed by an ON transition; these events are recorded as Reset events in the “ON Source” register.

The ON Source and OFF Source register fields are defined in Table 2.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16387 (4003h) Power State	15	CHIP_ON	0	Indicates whether the system is ON or OFF. 0 = OFF 1 = ON (or SLEEP) OFF can be commanded by writing CHIP_ON = 0. Note that writing CHIP_ON = 1 is not a valid ‘ON’ event, and will not trigger an ON transition.
	14	CHIP_SLP	0	Indicates whether the system is in the SLEEP state. 0 = Not in SLEEP 1 = SLEEP WAKE can be commanded by writing CHIP_SLP = 0. SLEEP can be commanded by writing CHIP_SLP = 1.
	11:10	PWRSTATE_DLY	10	Power State transition delay 00 = No delay 01 = No delay 10 = 1ms 11 = 10ms
R16398 (400Eh) ON Source	15	ON_TRANS	0	Most recent ON/WAKE event type 0 = WAKE transition 1 = ON transition
	11	ON_GPIO	0	Most recent ON/WAKE event type 0 = Not caused by GPIO input 1 = Caused by GPIO input
	10	ON_SYSLO	0	Most recent WAKE event type 0 = Not caused by SYSVDD 1 = Caused by SYSLO threshold. Note that the SYSLO threshold cannot trigger an ON event.
	9	ON_PEN_DOWN	0	Most recent WAKE event type 0 = Not caused by Pen Down 1 = Caused by Touch Panel Pen Down detection. Note that the Pen Down detection cannot trigger an ON event.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	8	ON_CHG	0	Most recent WAKE event type 0 = Not caused by Battery Charger 1 = Caused by Battery Charger
	7	ON_WDOG_TO	0	Most recent WAKE event type 0 = Not caused by Watchdog timer 1 = Caused by Watchdog timer
	6	ON_SW_REQ	0	Most recent WAKE event type 0 = Not caused by software WAKE 1 = Caused by software WAKE command (CHIP_SLP = 0)
	5	ON_RTC_ALM	0	Most recent ON/WAKE event type 0 = Not caused by RTC Alarm 1 = Caused by RTC Alarm
	4	ON_ON_PIN	0	Most recent ON/WAKE event type 0 = Not caused by the ON pin 1 = Caused by the ON pin
	3	RESET_CNV_UV	0	Most recent ON event type 0 = Not caused by undervoltage 1 = Caused by a Device Reset due to a Converter (LDO or DC-DC) undervoltage condition
	2	RESET_SW	0	Most recent ON event type 0 = Not caused by Software Reset 1 = Caused by Software Reset
	1	RESET_HW	0	Most recent ON event type 0 = Not caused by Hardware Reset 1 = Caused by Hardware Reset
	0	RESET_WDOG	0	Most recent ON event type 0 = Not caused by the Watchdog 1 = Caused by a Device Reset triggered by the Watchdog timer
R16399 (400Fh) OFF Source	13	OFF_INTLDO_ERR	0	Most recent OFF event type 0 = Not caused by LDO13 Error condition 1 = Caused by LDO13 Error condition
	12	OFF_PWR_SEQ	0	Most recent OFF event type 0 = Not caused by Power Sequence Failure 1 = Caused by a Power Sequence Failure
	11	OFF_GPIO	0	Most recent OFF event type 0 = Not caused by GPIO input 1 = Caused by GPIO input
	10	OFF_SYSVDD	0	Most recent OFF event type 0 = Not caused by SYSVDD 1 = Caused by the SYSLO or SHUTDOWN threshold
	9	OFF_THERR	0	Most recent OFF event type 0 = Not caused by temperature 1 = Caused by over-temperature

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6	OFF_SW_REQ	0	Most recent OFF event type 0 = Not caused by software OFF 1 = Caused by software OFF command (CHIP_ON = 0)
	4	OFF_ON_PIN	0	Most recent OFF event type 0 = Not caused by the ON pin 1 = Caused by the ON pin

Table 2 Power State Control Registers

Table 3 lists all of the events which can trigger an ON, WAKE, OFF or SLEEP transition sequence. It also lists the associated status bits of the ‘ON Source’ and ‘OFF Source’ register bits which are asserted under each condition.

TRANSITION SEQUENCE	EVENT	NOTES	ON SOURCE / OFF SOURCE
ON (see note 1)	RTC alarm	An ON request occurs if the RTC Alarm occurs in the OFF power state. See Section 20.	ON_TRANS, ON_RTC_ALM
	GPIO ON request	Requires a GPIO to be configured as “Power On request” or “Power On/Off request”. See Section 21.	ON_TRANS, ON_GPIO
	$\overline{\text{ON}}$ pin request	Requires the $\overline{\text{ON}}$ pin to be configured to generate ON request. See Section 11.6.	ON_TRANS, ON_ON_PIN
WAKE	Software WAKE	Writing CHIP_SLP = 0. See Table 2.	ON_SW_REQ
	Battery Charger event	Occurs when a Charger Interrupt event is triggered. See Section 17.7.8.	ON_CHG
	Watchdog timeout	Requires the Watchdog to be configured to generate WAKE request. See Section 25.	ON_WDOG_TO
	RTC alarm	A WAKE request occurs if the RTC Alarm occurs in the SLEEP power state. See Section 20.	ON_RTC_ALM
	Touch Panel pen down	Requires the Touch Panel to be configured to generate WAKE request. See Section 19.	ON_PEN_DOWN
	GPIO WAKE request	Requires a GPIO to be configured as “Sleep/Wake request”. See Section 21.	ON_GPIO
	SYSVDD undervoltage	Requires the SYSVDD monitor circuit to be configured to generate WAKE request. See Section 24.4.	ON_SYSLO
	$\overline{\text{ON}}$ pin request	Requires the $\overline{\text{ON}}$ pin to be configured to generate WAKE request. See Section 11.6.	ON_ON_PIN
OFF (see note 2)	Watchdog timeout	Requires the Watchdog to be configured to generate Device Reset. See Section 25.	RESET_WDOG (See note 3)
	Hardware Reset	See Section 24.	RESET_HW (See note 3)
	Software Reset	See Section 24.	RESET_SW (See note 3)
	Power Management Undervoltage Reset	Configurable option for each LDO/DC-DC converter. See Section 15.	RESET_CNV_UV (See note 3)
	Software OFF request	Writing CHIP_ON = 0. See Table 2.	OFF_SW_REQ
	ON pin request	Requires the $\overline{\text{ON}}$ pin to be configured to generate OFF request. See Section 11.6.	OFF_ON_PIN
	Thermal shutdown	See Section 26.	OFF_THERR
	SYSVDD undervoltage	Requires the SYSVDD monitor circuit to be configured to generate OFF request. See Section 24.4.	OFF_SYSVDD
	SYSVDD shutdown	SYSVDD has fallen below the SHUTDOWN threshold. See Section 24.4.	OFF_SYSVDD

	GPIO OFF request	Requires a GPIO to be configured as “Power On/Off request”. See Section 21.	OFF_GPIO
	Power Sequence failure	DC-DC converters, LDOs or CLKOUT circuits (including FLL) have failed to start up within the permitted time.	OFF_PWR_SEQ
	Internal LDO error	Error condition detected in LDO13	OFF_INTLDO_ERR
SLEEP	Software SLEEP request	Writing CHIP_SLP = 1. See Table 2.	See note 4 and note 5
	GPIO SLEEP request	Requires a GPIO to be configured as “Sleep request” or “Sleep/Wake request”. See Section 21.	See note 4 and note 5

Table 3 Power State Transition Events

Notes:

1. An ON sequence is only permitted when the supply voltage SYSVDD exceeds a programmable threshold V_{SYSOK}. See Section 24.4 for details of SYSVDD voltage monitoring.
2. Selected OFF events may be masked during Battery Charging using the CHG_OFF_MASK bit. This allows user-initiated OFF events (Software OFF, ON pin request, GPIO OFF request) to be inhibited. See Section 17.7.2.
3. These Reset conditions result in an OFF transition followed by an ON transition. These events are recorded as Reset events in the ‘ON Source’ register.
4. SLEEP transitions are not possible when any of the Battery Charger Interrupts is set. If any of the Battery Charger Interrupts is asserted when a SLEEP transition is requested, then the transition will be unsuccessful and the WM8311 will remain in the ON power state. See Section 17.7.8 for details of the Battery Charger Interrupts.
5. SLEEP events are not recorded in the ‘OFF Source’ register.

11.4 POWER STATE INTERRUPTS

Power State transitions are associated with a number of Interrupt event flags. Transitions to BACKUP, SLEEP, ON or OFF states are indicated by the Interrupt bits described in Table 4. Each of these secondary interrupts triggers a primary Power State Interrupt, PS_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 4.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	2	PS_POR_EINT	Power On Reset interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	1	PS_SLEEP_OFF_EINT	SLEEP or OFF interrupt (Power state transition to SLEEP or OFF states) (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	0	PS_ON_WAKE_EINT	ON or WAKE interrupt (Power state transition to ON state) (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16410 (401Ah) Interrupt Status 2 Mask	2	IM_PS_POR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_PS_SLEEP_OFF_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_PS_ON_WAKE_EINT	Interrupt mask. 0 = Do not mask interrupt.

ADDRESS	BIT	LABEL	DESCRIPTION
			1 = Mask interrupt. Default value is 1 (masked)

Table 4 Power State Interrupts

11.5 POWER STATE GPIO INDICATION

The WM8311 can be configured to generate logic signals via GPIO pins to indicate the current Power State. See Section 21 for details of configuring GPIO pins.

A GPIO pin configured as “ON state” output will be asserted when the WM8311 is in the ON state.

A GPIO pin configured as “SLEEP state” output will be asserted when the WM8311 is in the SLEEP state.

11.6 ON PIN FUNCTION

The $\overline{\text{ON}}$ pin is intended for connection to the master power switch on the user’s application. It can be used to start-up the WM8311 from the SLEEP or OFF states and also to power down the system. This pin operates on the LDO12 (VPMIC) power domain and has an internal pull-up resistor. This pin is asserted by shorting it to GND. A de-bounce circuit is provided on this input pin.

The behaviour of the $\overline{\text{ON}}$ pin is programmable. The primary action taken on asserting this pin is determined by the ON_PIN_PRIMACT register field. Note that the ON_PIN_INT interrupt event is always raised when the $\overline{\text{ON}}$ pin is asserted.

If the pin is held asserted for longer than the timeout period set by ON_PIN_TO, then a secondary action is executed. The secondary action is determined by the ON_PIN_SECACT register field.

If the pin is held asserted for a further timeout period, then a tertiary action is executed. The tertiary action is not programmable, and is to generate an OFF request.

An OFF request initiated by the $\overline{\text{ON}}$ pin may be masked during Battery Charging when the CHG_OFF_MASK bit is set. This allows user-initiated OFF events to be disabled in order to maintain the Battery Charger operation. See Section 17.7.2.

The status of the $\overline{\text{ON}}$ pin can be read at any time via the ON_PIN_STS register.

Note that the $\overline{\text{ON}}$ pin control registers are locked by the WM8311 User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16389 (4005h) ON Pin Control	9:8	ON_PIN_SECACT	01	Secondary action of $\overline{\text{ON}}$ pin (taken after 1 timeout period) 00 = Interrupt 01 = ON request 10 = OFF request 11 = Reserved *Protected by user key*
	5:4	ON_PIN_PRIMACT	00	Primary action of $\overline{\text{ON}}$ pin 00 = Ignore 01 = ON request 10 = OFF request 11 = Reserved Note that an Interrupt is always raised. *Protected by user key*
	3	ON_PIN_STS	0	Current status of $\overline{\text{ON}}$ pin 0 = Asserted (logic 0) 1 = Not asserted (logic 1)

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	ON_PIN_TO	00	$\overline{\text{ON}}$ pin timeout period 00 = 1s 01 = 2s 10 = 4s 11 = 8s *Protected by user key*

Table 5 ON Pin Control Registers

The $\overline{\text{ON}}$ pin interrupt event is always raised as part of the primary action when the $\overline{\text{ON}}$ pin is asserted. The $\overline{\text{ON}}$ pin interrupt is a selectable option as the secondary action. The $\overline{\text{ON}}$ pin interrupt event is also raised when the $\overline{\text{ON}}$ pin is de-asserted.

The $\overline{\text{ON}}$ pin interrupt event is indicated by the ON_PIN_CINT register field. This secondary interrupt triggers a primary ON Pin Interrupt, ON_PIN_INT (see Section 23). This can be masked by setting the mask bit as described in Table 6.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	12	ON_PIN_CINT	ON pin interrupt. (Rising and Falling Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	12	IM_ON_PIN_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 6 ON Pin Interrupt

11.7 RESET PIN FUNCTION

The $\overline{\text{RESET}}$ pin is an active low input/output which is used to command Hardware Resets in the WM8311 and in other connected devices. The pin is an open-drain type, with integrated pull-up; it can be driven low by external sources or by the WM8311 itself.

The WM8311 drives the $\overline{\text{RESET}}$ pin low in the OFF state. The output status of the $\overline{\text{RESET}}$ pin in SLEEP is configurable; this is determined by the RST_SLPENA register bit as defined in Table 7.

The WM8311 clears the $\overline{\text{RESET}}$ pin following the transition to ON. On completion of the state transition, the $\overline{\text{RESET}}$ pin is held low for a further delay time period, extending the $\overline{\text{RESET}}$ low duration. The $\overline{\text{RESET}}$ delay period is set by the RST_DUR register bit. See Figure 6 for further details.

The WM8311 detects a Hardware Reset request whenever the $\overline{\text{RESET}}$ pin is driven low by an external source. In this event, the WM8311 resets the internal control registers (excluding the RTC) and initiates a start-up sequence. See Section 24.

It is possible to mask the $\overline{\text{RESET}}$ pin input in the SLEEP state by setting the RST_SLP_MSK register bit. In SLEEP mode, if RST_SLP_MSK is set, the WM8311 will take no action if the $\overline{\text{RESET}}$ pin is pulled low.

Note that the $\overline{\text{RESET}}$ pin control registers are locked by the WM8311 User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16390 (4006h) Reset Control	5	RST_SLP_MSK	1	Masks the $\overline{\text{RESET}}$ pin input in SLEEP mode 0 = External $\overline{\text{RESET}}$ active in SLEEP 1 = External $\overline{\text{RESET}}$ masked in SLEEP *Protected by user key*

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4	RST_SLPENA	1	Sets the output status of RESET pin in SLEEP 0 = RESET high (not asserted) 1 = RESET low (asserted) *Protected by user key*
	1:0	RST_DUR	11	Delay period for releasing RESET after ON or WAKE sequence 00 = 3ms 01 = 11ms 10 = 51ms 11 = 101ms *Protected by user key*

Table 7 RESET Pin Control Registers

The WM8311 can generate an Auxiliary Reset output via a GPIO pin configured as "Auxiliary Reset" output (see Section 21). This signal is asserted in the OFF state. The status of the Auxiliary Reset in the SLEEP state is configurable, using the AUXRST_SLPENA register bit as defined in Table 8.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16390 (4006h) Reset Control	6	AUXRST_SLPENA	1	Sets the output status of Auxiliary Reset (GPIO) function in SLEEP 0 = Auxiliary Reset not asserted 1 = Auxiliary Reset asserted *Protected by user key*

Table 8 Auxiliary Reset (GPIO) Control

The timing details of the RESET pin relative to an ON state transition are illustrated in Figure 6.

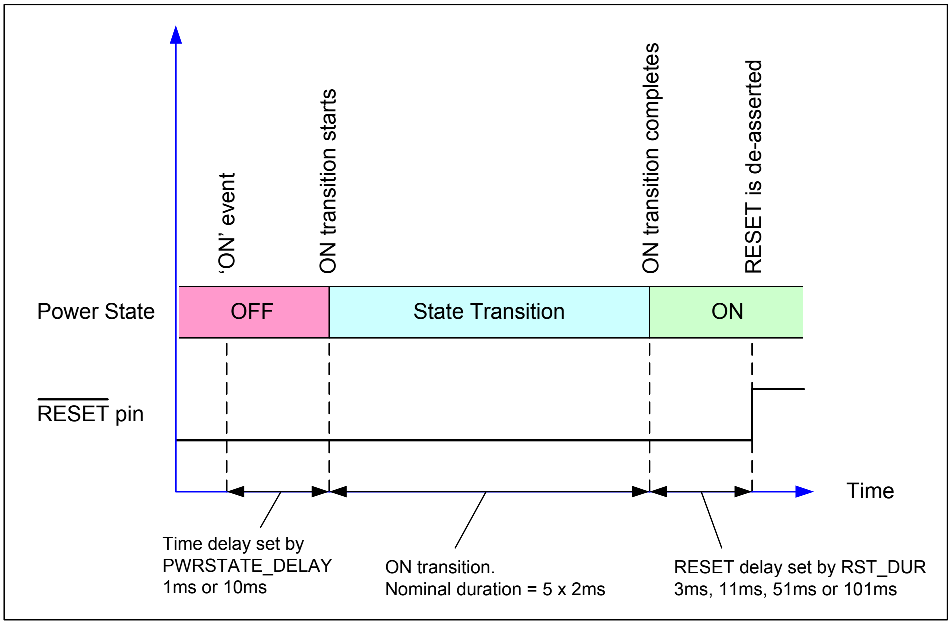


Figure 6 RESET Pin Output

12 CONTROL INTERFACE

12.1 GENERAL DESCRIPTION

The WM8311 is controlled by writing to its control registers. Readback is available for all registers, including Chip ID, power management status and GPIO status. The control interface can operate as a 2-wire (I2C) or 4-wire (SPI) control interface. Readback is provided on the bi-directional pin SDA1 in 2-wire (I2C) mode. The WM8311 Control Interface is powered by the DBVDD power domain.

The control interface mode is determined by the logic level on the CIFMODE pin as shown in Table 9.

CIFMODE	INTERFACE FORMAT
Low	2-wire (I2C) mode
High	4-wire (SPI) mode

Table 9 Control Interface Mode Selection

12.2 2-WIRE (I2C) CONTROL MODE

In 2-wire (I2C) mode, the WM8311 is a slave device on the control interface; SCLK1 is a clock input, while SDA1 is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8311 transmits logic 1 by tri-stating the SDA1 pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA1 line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single 2-wire control bus, every device on the bus has a unique 8-bit device ID (this is not the same as the 16-bit address of each register in the WM8311). The device ID is determined by the logic level on the $\overline{\text{CS}}$ pin as shown in Table 10. The LSB of the device ID is the Read/Write bit; this bit is set to logic 1 for “Read” and logic 0 for “Write”.

$\overline{\text{CS}}$	DEVICE ID
Low	0110 100x = 68h(write) / 69h(read)
High	0110 110x = 6Ch(write) / 6Dh(read)

Table 10 Control Interface Device ID Selection

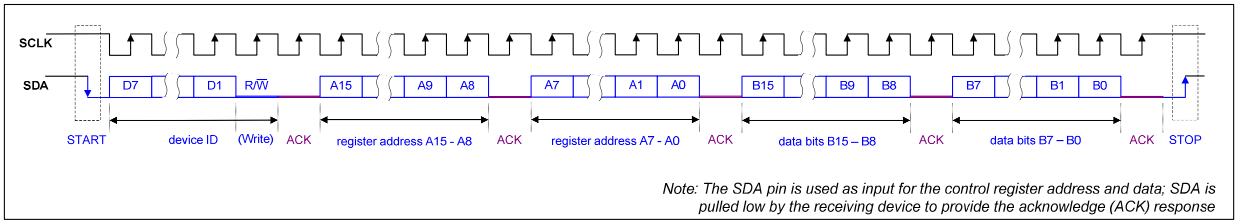
The WM8311 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDA1 while SCLK1 remains high. This indicates that a device ID, register address and data will follow. The WM8311 responds to the start condition and shifts in the next eight bits on SDA1 (8-bit device ID including Read/Write bit, MSB first). If the device ID received matches the device ID of the WM8311, then the WM8311 responds by pulling SDA1 low on the next clock pulse (ACK). If the device ID is not recognised or the R/W bit is set incorrectly, the WM8311 returns to the idle condition and waits for a new start condition and valid address.

If the device ID matches the device ID of the WM8311, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA1 while SCLK1 remains high. After receiving a complete address and data sequence the WM8311 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA1 changes while SCLK1 is high), the device returns to the idle condition.

The WM8311 supports the following read and write operations:

- Single write
- Single read
- Multiple write using auto-increment
- Multiple read using auto-increment

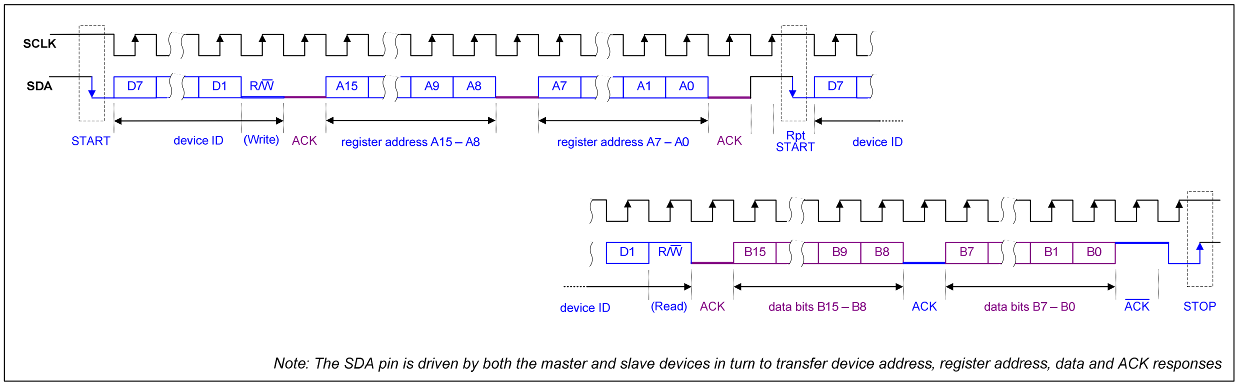
The sequence of signals associated with a single register write operation is illustrated in Figure 7.



Note: The SDA pin is used as input for the control register address and data; SDA is pulled low by the receiving device to provide the acknowledge (ACK) response

Figure 7 Control Interface 2-wire (I2C) Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 8.



Note: The SDA pin is driven by both the master and slave devices in turn to transfer device address, register address, data and ACK responses

Figure 8 Control Interface 2-wire (I2C) Register Read

The Control Interface also supports other register operations, as listed above. The interface protocol for these operations is summarised below. The terminology used in the following figures is detailed in Table 11.

Note that, for multiple write and multiple read operations, the auto-increment option must be enabled. This feature is enabled by default; it is described in Table 12 below.

TERMINOLOGY	DESCRIPTION	
S	Start Condition	
Sr	Repeated start	
A	Acknowledge (SDA Low)	
$\overline{\text{A}}$	Not Acknowledge (SDA High)	
P	Stop Condition	
R/$\overline{\text{W}}$	ReadNotWrite	0 = Write 1 = Read
[White field]	Data flow from bus master to WM8311	
[Grey field]	Data flow from WM8311 to bus master	

Table 11 Control Interface Terminology

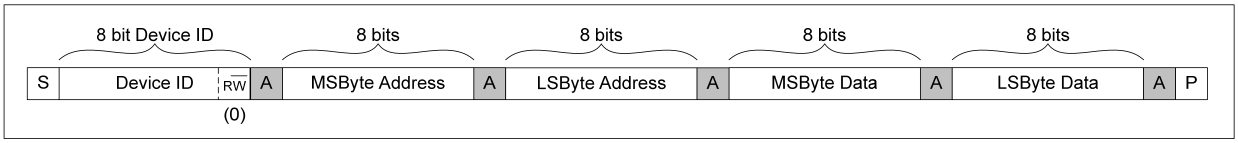


Figure 9 Single Register Write to Specified Address

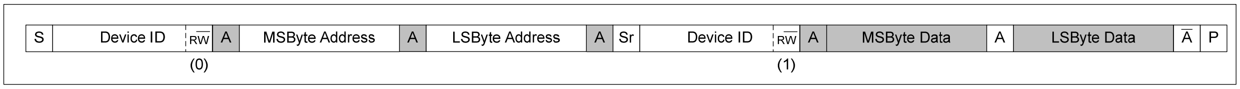


Figure 10 Single Register Read from Specified Address

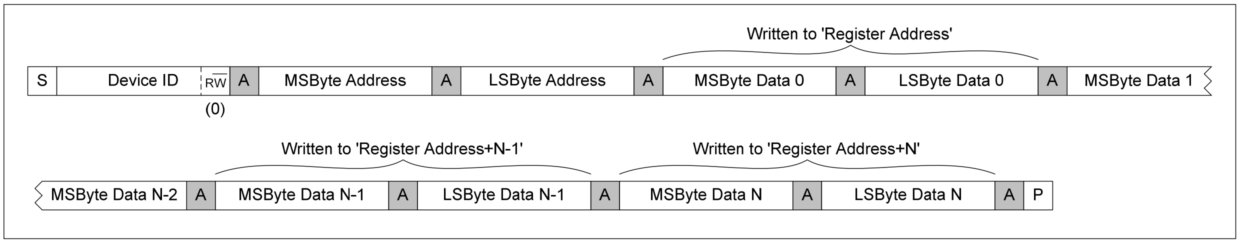


Figure 11 Multiple Register Write to Specified Address using Auto-increment

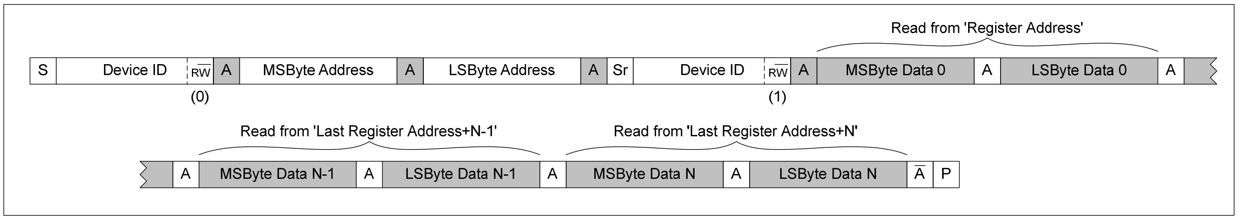


Figure 12 Multiple Register Read from Specified Address using Auto-increment

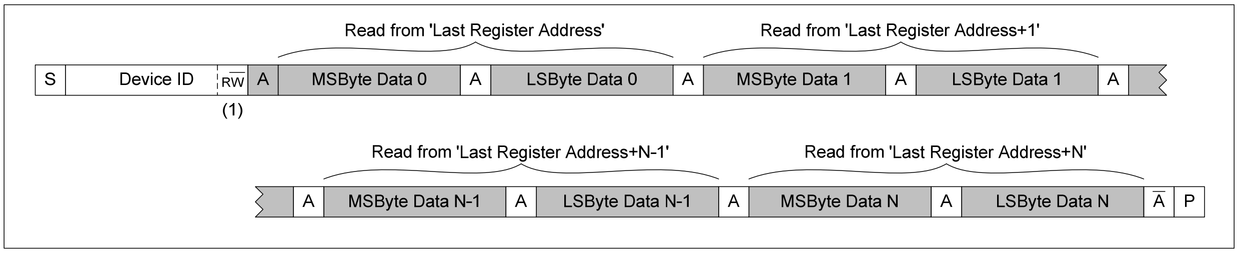


Figure 13 Multiple Register Read from Last Address using Auto-increment

Multiple Write and Multiple Read operations enable the host processor to access sequential blocks of the data in the WM8311 register map faster than is possible with single register operations. The auto-increment option is enabled when the AUTOINC register bit is set. This bit is defined in Table 12. Auto-increment is enabled by default.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16391 (4007h) Control Interface	2	AUTOINC	1	Enable Auto-Increment function 0 = Disabled 1 = Enabled

Table 12 Auto-Increment Control

12.3 4-WIRE (SPI) CONTROL MODE

In this mode, the WM8311 registers are accessed using a 4-wire serial control interface. The $\overline{CS}$ and SCLK1 pins provide the 'Chip Select' and 'Serial Data Clock' functions respectively. Serial data input is supported on the SDA1 pin; serial data output is supported on the SDOUT1 pin.

A control word consists of 32 bits. The first bit is the read/write bit (R/W), which is followed by 15 address bits (A14 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

In Write operations (R/W=0), all SDA1 bits are driven by the controlling device. Each rising edge of SCLK1 clocks in one data bit from the SDA1 pin. A rising edge on $\overline{CS}$ latches in a complete control word consisting of the last 32 bits.

In Read operations, the SDA1 pin is ignored following receipt of the valid register address. The data bits are output by the WM8311 on the SDOUT1 pin. SDOUT1 is undriven (high impedance) when not outputting register data bits.

The SDOUT1 pin is an Open Drain output; an external pull-up resistor to DBVDD is required on SDOUT1 in 4-wire (SPI) mode.

The sequence of signals associated with a register write operation is illustrated in Figure 14.

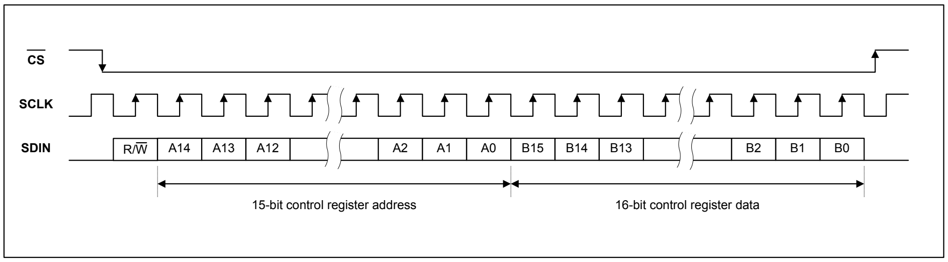


Figure 14 Control Interface 4-wire (SPI) Register Write

The sequence of signals associated with a register read operation is illustrated in Figure 15.

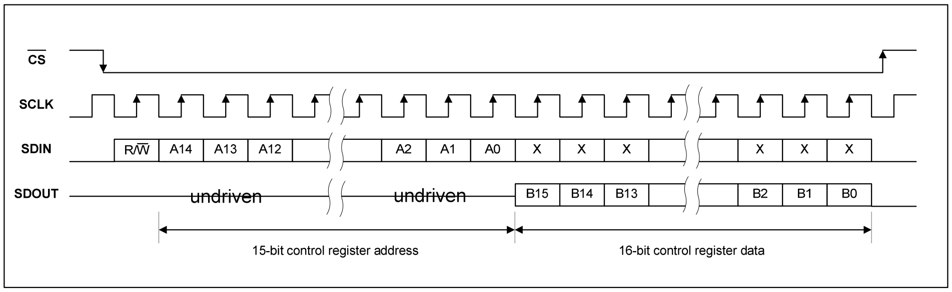


Figure 15 Control Interface 4-wire (SPI) Register Read

12.4 REGISTER LOCKING

Selected registers are protected by a security key. These registers can only be written to when the appropriate 'unlock' code has been written to the Security Key register.

The protected registers include those associated with Reset Control, OTP Programming, RTC Trim and Battery Charger operation. Other selected functions also include protected registers; the affected registers are identified in the Register Map definitions throughout the document, and also in Section 29.

To unlock the protected registers, a value of 9716h must be written to the Security register (R16392), as defined in Table 13.

It is recommended to re-lock the protected registers immediately after writing to them. This helps protect the system against accidental overwriting of register values. To lock the protected registers, a value of 0000h should be written to the Security register.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16392 (4008h) Security Key	15:0	SECURITY [15:0]	0000h	Security Key A value of 9716h must be written to this register to access the user-keyed registers.

Table 13 Security Key Registers

12.5 SOFTWARE RESET AND CHIP ID

A Software Reset can be commanded by writing to Register 0000h. This is a read-only register field and the contents of this register will not be affected by a write operation. For more details of the different reset types, see Section 24.

Note that a maximum of 6 Software Resets is permitted. If more than 6 Software Resets are scheduled, the WM8311 will remain in the OFF state until the next valid ON state transition event occurs.

The Chip ID can be read back from Register 0000h. Other ID fields can be read from the registers defined in Table 14.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (0000h) Reset/ID	15:0	CHIP_ID [15:0]	0000h	Writing to this register causes a Software Reset. The register map contents may be reset, depending on SW_RESET_CFG. Reading from this register will indicate Chip ID.
R1 (0001h) Revision	15:8	PARENT_REV [7:0]	00h	The revision number of the parent die
	7:0	CHILD_REV [7:0]	00h	The revision number of the child die (when present)
R16384 (4000h) Parent ID	15:0	PARENT_ID [15:0]	6204h	The ID of the parent die

Table 14 Reading Device Information

12.6 SOFTWARE SCRATCH REGISTER

The WM8311 provides one 16-bit register as a “Software Scratch” register. This is available for use by the host processor to store data for any purpose required by the application.

The contents of the Software Scratch register are retained in the BACKUP power state.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16393 (4009h) Software Scratch	15:0	SW_SCRATCH [15:0]	0000h	Software Scratch Register for use by the host processor. Note that this register’s contents are retained in the BACKUP power state.

Table 15 Software Scratch Register

13 CLOCKING AND OSCILLATOR CONTROL

13.1 GENERAL DESCRIPTION

The WM8311 incorporates a 32.768kHz crystal oscillator in order to maintain the Real Time Clock (RTC). An external crystal is normally required. Alternatively, a 32.768kHz signal may be input directly on the XTI pin. The crystal oscillator and RTC are enabled at all times, including the OFF and BACKUP power states. It is possible to disable the crystal oscillator in BACKUP for power-saving RTC 'unclocked' mode if desired. The WM8311 clock functions are illustrated in Figure 16.

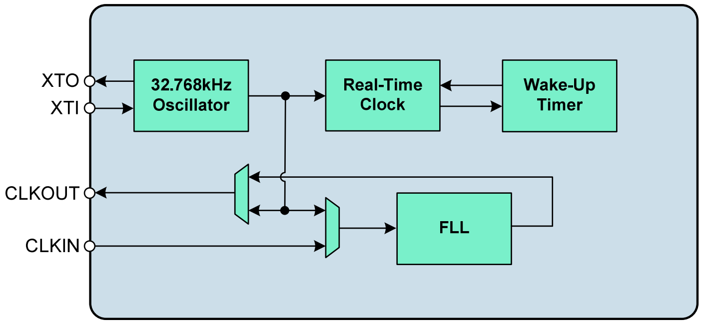


Figure 16 Clocking Configuration

The 32.768kHz crystal oscillator is enabled using the XTAL_ENA register. The crystal oscillator is enabled in the OFF, ON and SLEEP states when XTAL_ENA is set. The status of the crystal oscillator in BACKUP is selected using the XTAL_BKUPENA register.

Note that the XTAL_ENA field is set via OTP/ICE settings only; it cannot be changed by writing to the control register. Also, if an external 32.768kHz signal is connected as an input to the XTI pin, and the crystal is omitted, it is still required to set XTAL_ENA = 1 for normal operation.

The crystal oscillator can be disabled in the BACKUP state by setting the XTAL_BKUPENA register bit to 0. This feature may be used to minimise the device power consumption in the BACKUP state, as described in Section 20.5. The crystal oscillator is maintained in the BACKUP state if both XTAL_ENA and XTAL_BKUPENA are set to 1.

A clock output signal CLKOUT is provided, for the purpose of clocking other devices. This output may be driven by the 32.768kHz oscillator or by the output of a Frequency Locked Loop (FLL). The FLL provides a flexible capability to generate a new clock signal either from the 32.768kHz oscillator or from an external input CLKIN. The FLL is tolerant of jitter and may be used to generate a stable clock signal from a less stable input reference. The FLL output can be routed to the CLKOUT pin.

The CLKOUT signal can be enabled or disabled directly by writing to the CLKOUT_ENA register in the ON or SLEEP power states. The CLKOUT can also be controlled as part of the power state transitions using the CLKOUT_SLOT and CLKOUT_SLP_SLOT register fields. See Section 11.3 for a description of the state transition timeslots.

The CLKOUT pin may be configured as a CMOS output or as an Open-Drain output. At high frequencies, the CMOS output is recommended. The CLKOUT signal is referenced to the DBVDD power domain.

If the XTAL_INH bit is set, then an 'ON' state transition is delayed until the CLKOUT output is valid. (Note that CLKOUT may be the crystal oscillator output, or may be the FLL output.). This may be desirable if the CLKOUT signal is used as a clock for another circuit, to ensure that the CLKOUT signal has been verified before the 'ON' state transition occurs. Note that the CLKOUT output is always disabled in the OFF power state; it is typically enabled as part of the 'ON' state transition sequence. Setting XTAL_INH = 1 ensures that the CLKOUT output cannot be enabled until the source signal (crystal oscillator or FLL) has been verified.

The CLKOUT control fields are described in Table 16. Some of these controls may also be stored in the integrated OTP memory. See Section 14 for details.

The 32.768kHz oscillator may also be output on a GPIO pin, as described in Section 21. Note that a GPIO pin configured as 32.768kHz output will continue to output the oscillator clock in the OFF power state; this may be used to provide clocking to the processor in the OFF state, provided that the selected power domain for that GPIO pin remains enabled in the OFF state. The CLKOUT output is always disabled in the OFF power state.

A separate internal RC oscillator generates the required clocks for the integrated DC-DC Converters on the WM8311. Note that a 2MHz 'External Power Clock', derived from this oscillator, may be output on a GPIO pin to provide synchronised clocking of external DC-DC Converters if required (see Section 21). The 2MHz External Power Clock is only enabled when either of the External Power Enable signals EPE1 or EPE2 is asserted. The External Power Enable (EPE) signals are controlled as described in Section 15.3.

Note that the CLKOUT_ENA control register is locked by the WM8311 User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16528 (4090h) Clock Control 1	15	CLKOUT_ENA	0	CLKOUT output enable 0 = Disabled 1 = Enabled *Protected by user key*
	13	CLKOUT_OD	0	CLKOUT pin configuration 0 = CMOS 1 = Open Drain
	10:8	CLKOUT_SLOT	000	CLKOUT output enable ON slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Do not enable 111 = Do not enable
	6:4	CLKOUT_SLPSLOT	000	CLKOUT output SLEEP slot select 000 = Controlled by CLKOUT_ENA 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = Controlled by CLKOUT_ENA 111 = Controlled by CLKOUT_ENA
	0	CLKOUT_SRC	0	CLKOUT output source select 0 = FLL output 1 = 32.768kHz oscillator
R16529 (4091h) Clock Control 2	15	XTAL_INH	0	Crystal Start-Up Inhibit 0 = Disabled 1 = Enabled When XTAL_INH=1, the 'ON' transition is inhibited until the crystal oscillator is valid
	13	XTAL_ENA	0	Crystal Oscillator Enable 0 = Disabled at all times 1 = Enabled in OFF, ON and SLEEP states (Note that the BACKUP behaviour is determined by XTAL_BKUPENA.)
	12	XTAL_BKUPENA	1	Selects the RTC and 32.768kHz oscillator in BACKUP state

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				0 = RTC unclocked in BACKUP 1 = RTC maintained in BACKUP (Note that XTAL_ENA must also be set if the RTC is to be maintained in BACKUP.)

Table 16 Clocking Control

13.2 CRYSTAL OSCILLATOR

The crystal oscillator generates a 32.768kHz reference clock, which is used to provide reference clock for the Real Time Clock (RTC) in the WM8311. It may also be used as a reference input to the FLL, for the purpose of generating other clocks. The oscillator requires an external crystal on the XTI and XTO pins, as well as two capacitors, connected as shown in Figure 17.

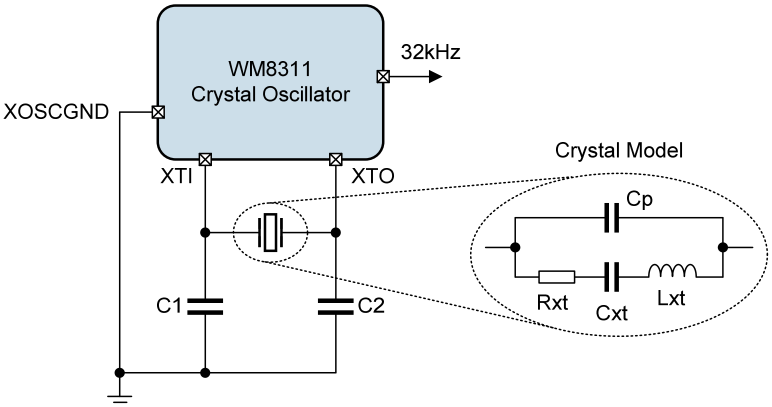


Figure 17 Crystal Oscillator

A suitable crystal oscillator should be selected in accordance with the following requirements:

PARAMETER	MIN	MAX	UNITS
Nominal frequency	32.768		kHz
Series resistance	50	70	kΩ
Maximum driving level	0.5		μW

Table 17 Selection of Crystal Oscillator Component

The load capacitors C1 and C2 should be selected according to the recommended load capacitance, C_L of the crystal, which is given by the following equation:

$$\text{Load Capacitance } C_L = \frac{C1 \times C2}{C1 + C2} + C_{STRAY}$$

Assuming C1 = C2 and C_{STRAY} = 2.75pF (typical pad i/o capacitance), then:

$C1 = C2 = 2 \times (C_L - 2.75\text{pF})$.

For example, if the crystal has a load capacitance C_L = 9pF, then C1 = C2 = 12.5pF.

If a suitable 32.768kHz clock is already present elsewhere in the system, it is possible for the WM8311 to use that external clock instead. The external clock should be applied to pin XTI, and the XTO pin left floating in this case.

13.3 FREQUENCY LOCKED LOOP (FLL)

The integrated FLL can be used to generate a clock on the CLKOUT pin from a wide variety of different reference sources and frequencies. The FLL can use either CLKIN or the 32.768kHz oscillator as its reference. A wide range of CLKIN frequencies can be supported; this may be a high frequency (eg. 12.288MHz) or low frequency (eg. 32.768kHz) reference. The FLL is tolerant of jitter and may be used to generate a stable clock reference from a less stable input signal. The FLL characteristics are summarised in “Electrical Characteristics”.

To simplify the configuration of the FLL, an ‘automatic’ mode is provided in order to synthesize a number of commonly used reference frequencies using the 32.768kHz crystal oscillator as a reference.

The FLL is enabled using the FLL_ENA register bit. Note that, when changing FLL settings, it is recommended that the digital circuit be disabled via FLL_ENA and then re-enabled after the other register settings have been updated. When changing the input reference frequency F_{REF}, it is recommended that the FLL be reset by setting FLL_ENA to 0.

Note that, when FLL_ENA = 0, the readback value of all the FLL configuration registers (R16530 through to R16534) is not valid. It is still possible to write to the registers as normal, but the correct values will not read back until the FLL is enabled by setting FLL_ENA to 1.

The FLL input reference is configured using the FLL_CLK_SRC register bit. The available sources are the CLKIN pin or the 32.768kHz crystal oscillator.

The field FLL_CLK_REF_DIV provides the option to divide the selected input reference by 1, 2, 4 or 8. This field should be set to bring the reference down to 13.5MHz or below. For best performance, it is recommended that the highest possible frequency - within the 13.5MHz limit - should be selected.

The field FLL_CTRL_RATE controls internal functions within the FLL; it is recommended that only the default setting be used for this parameter. FLL_GAIN controls the internal loop gain and should be set to the recommended value quoted in Table 20.

The FLL output frequency is directly determined from FLL_FRATIO, FLL_OUTDIV and the real number represented by FLL_N and FLL_K. The field FLL_N is an integer (LSB = 1); FLL_K is the fractional portion of the number (MSB = 0.5). The fractional portion is only valid when enabled by the field FLL_FRAC.

Power consumption in the FLL is reduced in integer mode; however, the performance may also be reduced, with increased noise or jitter on the output.

If low power consumption is required, then FLL settings must be chosen where N.K is an integer (ie. FLL_K = 0). In this case, the fractional mode can be disabled by setting FLL_FRAC = 0.

For best FLL performance, a non-integer value of N.K is required. In this case, the fractional mode must be enabled by setting FLL_FRAC = 1. The FLL settings must be adjusted, if necessary, to produce a non-integer value of N.K.

The FLL output frequency is generated according to the following equation:

$$F_{OUT} = (F_{VCO} / FLL\_OUTDIV)$$

The FLL operating frequency, F_{VCO} is set according to the following equation:

$$F_{VCO} = (F_{REF} \times N.K \times FLL\_FRATIO)$$

See Table 20 for the coding of the FLL_OUTDIV and FLL_FRATIO fields.

F_{REF} is the input frequency, as determined by FLL_CLK_REF_DIV.

F_{VCO} must be in the range 90-100 MHz. Frequencies outside this range cannot be supported.

Note that the output frequencies that do not lie within the ranges quoted above cannot be guaranteed across the full range of device operating temperatures.

In order to follow the above requirements for F_{VCO}, the value of FLL_OUTDIV should be selected according to the desired output F_{OUT}. The divider, FLL_OUTDIV, must be set so that F_{VCO} is in the range 90-100MHz. The available divisions are integers from 4 to 64. Some typical settings of FLL_OUTDIV are noted in Table 18.

OUTPUT FREQUENCY F_{OUT}	FLL_OUTDIV
2.8125 MHz - 3.125 MHz	011111 (divide by 32)
3.75 MHz - 4.1667 MHz	010111 (divide by 24)
5.625 MHz - 6.25 MHz	001111 (divide by 16)
11.25 MHz - 12.5 MHz	000111 (divide by 8)
18 MHz - 20 MHz	000100 (divide by 5)
22.5 MHz - 25 MHz	000011 (divide by 4)

Table 18 Selection of FLL_OUTDIV

The value of FLL_FRATIO should be selected as described in Table 19.

REFERENCE FREQUENCY F_{REF}	FLL_FRATIO
1MHz - 13.5MHz	000 (divide by 1)
256kHz - 1MHz	001 (divide by 2)
128kHz - 256kHz	010 (divide by 4)
64kHz - 128kHz	011 (divide by 8)
Less than 64kHz	100 (divide by 16)

Table 19 Selection of FLL_FRATIO

In order to determine the remaining FLL parameters, the FLL operating frequency, F_{VCO}, must be calculated, as given by the following equation:

$$F_{VCO} = (F_{OUT} \times FLL\_OUTDIV)$$

The value of FLL_N and FLL_K can then be determined as follows:

$$N.K = F_{VCO} / (FLL\_FRATIO \times F_{REF})$$

See Table 20 for the coding of the FLL_OUTDIV and FLL_FRATIO fields.

Note that F_{REF} is the input frequency, after division by FLL_CLK_REF_DIV, where applicable.

In FLL Fractional Mode, the fractional portion of the N.K multiplier is held in the FLL_K register field. This field is coded as a fixed point quantity, where the MSB has a weighting of 0.5. Note that, if desired, the value of this field may be calculated by multiplying K by 2^16 and treating FLL_K as an integer value, as illustrated in the following example:

If N.K = 8.192, then K = 0.192.

Multiplying K by 2^16 gives 0.192 x 65536 = 12582.912 (decimal) = 3126 (hex).

For best FLL performance, the FLL fractional mode is recommended. Therefore, if the calculations yield an integer value of N.K, then it is recommended to adjust FLL_OUTDIV in order that N.K is a non-integer value. Care must always be taken to ensure that the FLL operating frequency, F_{VCO}, is within its recommended limits of 90-100 MHz.

The register fields that control the FLL are described in Table 20.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16530 (4092h) FLL Control 1	2	FLL_FRAC	0	Fractional enable 0 = Integer Mode 1 = Fractional Mode Integer mode offers reduced power consumption. Fractional mode offers best FLL performance, provided also that N.K is a non-integer value.
	0	FLL_ENA	0	FLL Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.
R16531 (4093h) FLL Control 2	13:8	FLL_OUTDIV [5:0]	000000	F_{OUT} clock divider 000000 = Reserved 000001 = Reserved 000010 = Reserved 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 ($F_{OUT} = F_{VCO}$ / FLL_OUTDIV)
	6:4	FLL_CTRL_RATE [2:0]	000	Frequency of the FLL control block 000 = F_{VCO} / 1 (Recommended value) 001 = F_{VCO} / 2 010 = F_{VCO} / 3 011 = F_{VCO} / 4 100 = F_{VCO} / 5 101 = F_{VCO} / 6 110 = F_{VCO} / 7 111 = F_{VCO} / 8 Recommended that this register is not changed from default.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	FLL_FRATIO [2:0]	000	F_{VCO} clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for high F_{REF} 011 recommended for low F_{REF}
R16532 (4094h) FLL Control 3	15:0	FLL_K [15:0]	0000h	Fractional multiply for F_{REF} (MSB = 0.5)
R16533 (4095h) FLL Control 4	14:5	FLL_N [9:0]	177h	Integer multiply for F_{REF} (LSB = 1)
	3:0	FLL_GAIN [3:0]	0000	Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1XXX = x 256 Recommended that this register is not changed from default.
R16534 (4096h) FLL Control 5	4:3	FLL_CLK_REF_DIV [1:0]	00	FLL Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 CLKIN must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.
	1:0	FLL_CLK_SRC [1:0]	00	FLL Clock source 00 = 32.768kHz xtal oscillator 01 = CLKIN 10 = Reserved 11 = Reserved

Table 20 FLL Control

13.3.1 FLL AUTO MODE

To simplify the configuration of the FLL, an ‘automatic’ mode is provided in order to synthesize a number of commonly used reference frequencies using the 32.768kHz crystal oscillator as a reference.

FLL Automatic mode is selected by setting the FLL_AUTO register bit as described in Table 21. When FLL_AUTO is set, the FLL is automatically configured to select the 32.768kHz oscillator as the FLL reference, and will generate the output frequency selected by FLL_AUTO_FREQ.

FLL Automatic mode should be selected while the FLL is disabled (FLL_ENA = 0). After Automatic mode has been selected, the FLL can be enabled and disabled using FLL_ENA, as described in Table 20.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16529 (4091h) Clock Control 2	7	FLL_AUTO	1	FLL Automatic Mode Enable 0 = Manual configuration mode 1 = Automatic configuration mode (To enable the FLL output, FLL_ENA must also be set in Automatic mode)
	2:0	FLL_AUTO_FREQ [2:0]	000	FLL Automatic Mode Frequency select 000 = 2.048MHz 001 = 11.2896MHz 010 = 12MHz 011 = 12.288MHz 100 = 19.2MHz 101 = 22.5792MHz 110 = 24MHz 111 = 24.576MHz

Table 21 FLL Automatic Mode

14 INSTANTCONFIG™ (ICE) AND OTP MEMORY CONTROL

14.1 GENERAL DESCRIPTION

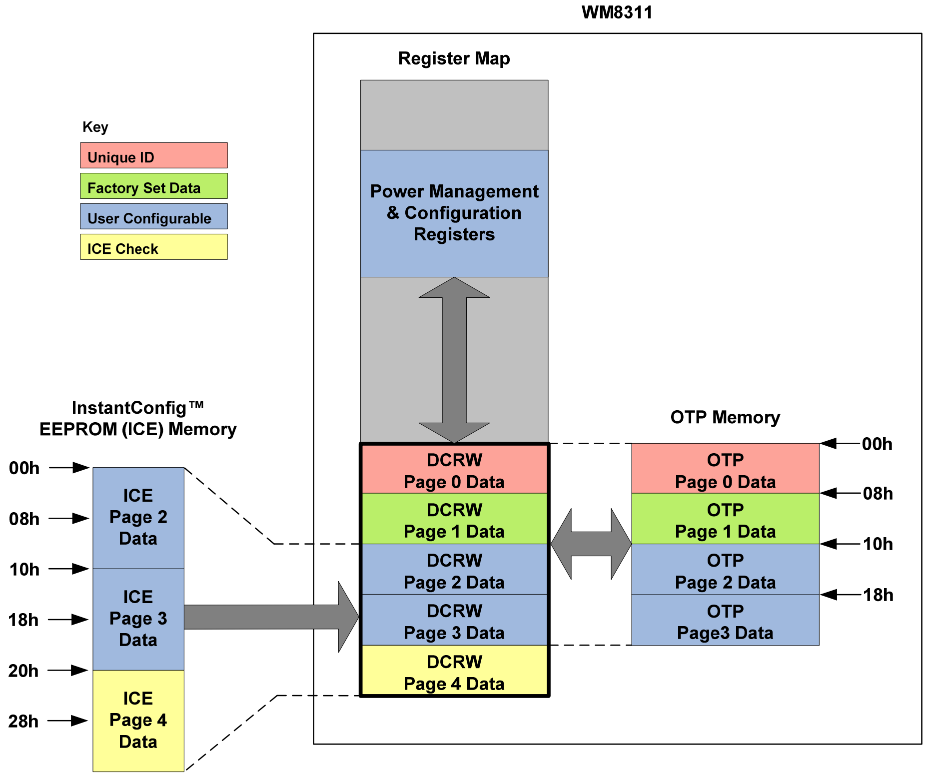
The WM8311 is a highly configurable device which can be tailored specifically to the requirements of a complex system application. The sequencing and voltage control of the integrated DC-DC Converters and LDOs in power-up, shut-down and SLEEP conditions is crucial to the robust operation of the application.

In development, the WM8311 allows designers to modify or experiment with different settings of the control sequences by writing to the applicable registers in the OFF state prior to commanding an ‘ON’ state transition. Configuration settings can also be stored on an external EEPROM and loaded onto the WM8311 as required, using the InstantConfig™ EEPROM (ICE) interface.

For production use, the WM8311 provides an on-chip One-Time Programmable (OTP) memory, in which the essential parameters for starting up the device can be programmed. This allows the WM8311 to start up and shut down the system with no dependency on any other devices for application-specific configuration parameters.

14.2 ICE AND OTP MEMORY DEFINITION

An illustration of the WM8311 memory locations is shown in Figure 18. The main Register Map of the WM8311 contains a block of data in a ‘Window’ area which is mirrored in the OTP and/or the ICE Memory. Data from the external ICE Memory can be loaded into the Window area. Data can be transferred from the Window into OTP Memory and also from the OTP Memory into the Window. The Window is called the Device Configuration Register Window (DCRW); the data in this Window is mirrored in other locations within the WM8311 Register Map.



Note that the recommended external ICE memory is arranged in 8-bit words

Figure 18 ICE and OTP Memory Layout

The DCRW contains 5 pages of data, as illustrated in Figure 18.

Page 0 of the DCRW contains a 128-bit pseudo-random unique ID. The unique ID is written to the OTP at the time of manufacture. It is copied to the DCRW when the WM8311 schedules an 'ON' transition. This data cannot be changed.

Page 1 of the DCRW contains factory-set calibration and configuration data. This data is written to the OTP at the time of manufacture. It is copied to the DCRW when the WM8311 schedules an 'ON' transition. This data cannot be changed.

Page 2 and Page 3 of the DCRW contain bootstrap configuration data. This defines the sequence and voltage requirements for powering up the WM8311, and for configuring functions such as the clocks, FLL, GPIO1-6 and LED status indicators. Under default conditions, the bootstrap data is loaded into the DCRW when the WM8311 schedules an 'ON' transition. The WM8311 automatically determines whether to load the bootstrap data from ICE or from OTP as described in Section 14.3.

Page 4 of the DCRW contains a register that is used for ICE validity checking. It is copied to the DCRW whenever the bootstrap configuration data is loaded from ICE in response to a start-up request in development mode. This register field enables the ICE data to be checked for valid content.

The OTP contains 4 pages of data, as illustrated in Figure 18. The contents of the OTP pages correspond to Pages 0, 1, 2 and 3 of the DCRW register map addresses.

The ICE memory contains 3 pages of data, as illustrated in Figure 18. The contents of the ICE pages correspond to Pages 2, 3 and 4 of the DCRW register map addresses.

Note that the ICE memory (recommended component) is arranged as 8-bit words in "big-endian" format, and is therefore addressed as 6 pages of 8-bit data, corresponding to 3 pages of 16-bit data. For example, the ICE memory address 00h corresponds to bits 15:8 of the first register map word in DCRW Page 2, and ICE address 01h corresponds to bits 7:0 of that same register word in DCRW.

The DCRW can be accessed directly using the Control Interface in the OFF, ON and SLEEP power states. Note that Read/Write access to the ICE or OTP memories is not possible directly; these can only be accessed by copying to/from the DCRW.

In the PROGRAM state, Page 2 and Page 3 of the DCRW can be written to the OTP.

14.3 BOOTSTRAP (START-UP) FUNCTION

Under default conditions, the WM8311 bootstrap configuration data is loaded when the WM8311 schedules an 'ON' transition. The bootstrap configuration data is loaded into Page 2 and Page 3 of the DCRW from either an external ICE or from the integrated OTP. (The factory-set data in Page 0 and Page 1 is always loaded from the integrated OTP memory.)

If Development mode is selected, then the bootstrap data is loaded from the InstantConfig™ EEPROM (ICE). If Development mode is not selected, then the bootstrap data is loaded from the OTP memory.

14.3.1 START-UP FROM OTP MEMORY

In volume production, development mode is not usually selected. In this case, the bootstrap configuration data is loaded from the internal OTP memory.

The WM8311 performs a check for valid OTP data; if the OTP_CUST_ID field is set to zero, then the WM8311 remains in the OFF power state. A non-zero OTP_CUST_ID field is used to confirm valid OTP contents.

The OTP memory contents are defined similarly to Pages 0, 1, 2 and 3 of the DCRW memory contents listed in Section 14.6.

14.3.2 START-UP FROM ICE MEMORY (DEVELOPMENT MODE)

Development mode is selected if a logic high level (referenced to the LDO12 VPMIC voltage) is present on SCLK2. This should be implemented using a pull-up resistor. See Section 14.3.4 for details of the External ICE Memory connection.

If development mode is selected, then the WM8311 performs a check for valid ICE data; if the ICE is not connected or contains invalid data, then the WM8311 remains in the OFF power state. The ICE data is deemed valid is the ICE_VALID_DATA field contains the value A596h.

The WM8311 also performs a check for valid contents in the OTP_CUST_ID field in development mode; if the OTP_CUST_ID field is set to zero, then the WM8311 remains in the OFF power state. A non-zero OTP_CUST_ID field is used to confirm valid ICE contents.

Note that, if a GPIO pin is configured in ICE memory as “Power On/Off request” (GPn_FN=02h), then inverted (active low) polarity should be selected for that GPIO (GPn_POL=0). The non-inverted (active high) polarity cannot be fully supported for this function in development mode.

This restriction is only applicable in development mode, and applies only to the GPIO “Power On/Off request” function. See Section 21 for details of the GPIO pin configuration registers.

The non-inverted (active high) polarity can be supported for the GPIO “Power On/Off request” function in development mode if the corresponding GPn_POL register bit in the OTP memory is set to 1. Note that, if the OTP memory is unprogrammed, the GPn_POL bits will default to 0.

14.3.3 START-UP FROM DCRW REGISTER SETTINGS

Under default settings, the bootstrap configuration data is always loaded when an ON transition is scheduled. For development purposes, this can be disabled by clearing the RECONFIG_AT_ON register bit. (Note that RECONFIG_AT_ON only selects whether Page 2/3/4 data is loaded; Page 0/1 data is always loaded from OTP whenever an ON transition is scheduled.)

When RECONFIG_AT_ON = 1, the bootstrap data is reloaded from either the ICE or OTP when an ON transition is scheduled. The logic level on SCLK2 is checked to determine whether the ICE or the OTP memory should be used. If RECONFIG_AT_ON = 0, then the latest contents of the DCRW are used to configure the start-up sequence.

Note that, when WM8311 start-up is scheduled using this method, the contents of OTP_CUST_ID is still checked for valid contents. In development mode, the ICE_VALID_DATA field is also checked. See Section 14.3.2 for details.

Note that the RECONFIG_AT_ON control register is locked by the WM8311 User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16390 (4006h) Reset Control	15	RECONFIG_AT_ON	1	Selects if the bootstrap configuration data should be reloaded when an ON transition is scheduled 0 = Disabled 1 = Enabled *Protected by user key*

Table 22 Bootstrap Configuration Reload Control

14.3.4 EXTERNAL ICE MEMORY CONNECTION

The recommended component for the external ICE is the Microchip 24AA32A, which provides 32 bytes of memory space. The ICE interfaces with the WM8311 via the SCLK2 and SDA2 pins, and initiates an I2C transfer of data from the ICE when required. The necessary electrical connections for this device are illustrated in Figure 19. The WM8311 assumes an EEPROM device ID of 1010 0001 (A1h) for ICE read cycles.

The ICE memory contents are defined similarly to Pages 2, 3 and 4 of the DCRW memory contents listed in Section 14.6.

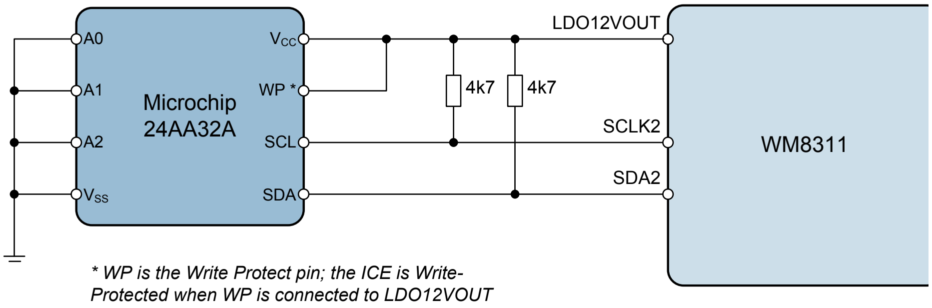


Figure 19 ICE Memory Connection

Note that the WM8311 does not support programming the external ICE memory.

External programming of ICE whilst physically connected to the WM8311 is possible by putting the WM8311 in the OFF state. This is supported on the evaluation board, provided the voltage levels on SCLK2 and SDA2 are less than or equal to the LDO12 VPMIC voltage. Note that the Write-Protect (WP) pin on the ICE must be connected to GND (Vss) in this case.

14.4 OTP / ICE MEMORY CONTROL

The OTP and ICE Memory commands are initiated by writing to the OTP Control Register, as defined in Section 14.4.6. The supported commands are described below.

READ ICE MEMORY - This command instructs the WM8311 to load data from the external ICE into the WM8311 DCRW memory area. Note that this command is performed automatically when the WM8311 starts up in development mode.

READ OTP MEMORY - This command instructs the WM8311 to load data from the integrated OTP memory area into the WM8311 DCRW memory area. Note that this command is performed automatically when the WM8311 starts up in normal (ie. non-development) mode.

WRITE OTP MEMORY - This command instructs the WM8311 to program the integrated OTP, by writing a copy of the DCRW memory area (Pages 0, 1, 2 and 3) to the OTP memory. This command should be performed after the required settings have been configured in the DCRW memory. The required settings can be configured in the DCRW either as a result of a ICE Read command, or else through register writes in the PROGRAM power state. Note that the Write OTP command should only be performed once on each OTP page; after the Write OTP command has been performed, the contents of the affected page(s) cannot be erased or re-programmed.

VERIFY OTP MEMORY - This command instructs the WM8311 to compare the contents of the OTP memory with the contents of the DCRW memory. The Verify OTP command performs a check that the OTP data is identical to the DCRW contents, in order to confirm the success of the Write OTP operation. For increased reliability, the WM8311 can apply a ‘Margin Read’ function when verifying the OTP memory; it is recommended that the Margin Read option is used, as described in Section 14.4.4.

FINALISE OTP PAGES - This command instructs the WM8311 to set the OTP_CUST_FINAL bit in the OTP memory. The Finalise OTP command ensures that any subsequent OTP_WRITE commands to Page 2 or Page 3 of the OTP will have no effect and that the OTP contents are maintained securely.

The OTP and ICE Memory commands are each described in the following sections. Note that, in some cases, commands may be executed on a single page of memory or may be executed as a Bulk operation on all available memory pages.

Completion of each OTP or ICE Memory command is indicated via an Interrupt flag, as described in Section 14.5. The pass/fail outcome of any Verify OTP command is also indicated by the Interrupt bits. Note that read/write access to the WM8311 Register Map is not supported while a ICE/OTP command is in progress. It is recommended that the $\overline{\text{IRQ}}$ pin is configured to indicate any ICE/OTP

Interrupt event; the host processor should read the OTP/ICE Interrupt event flags to confirm the OTP/ICE command status following the assertion of the $\overline{\text{IRQ}}$ pin.

The programming supply voltage PROGVDD is required for the OTP Write commands and the OTP Finalise command. It is also necessary to overdrive the LDO12VOUT pin from an external supply. See Section 6 for details of the required supply voltages.

14.4.1 ENTERING / EXITING THE PROGRAM STATE

The ICE and OTP commands are only supported when the WM8311 is in the PROGRAM state. The WM8311 can only enter the PROGRAM state as a transition from the OFF state. This is commanded by setting the OTP_PROG register bit.

Important note - when the PROGRAM state is selected, the WM8311 will read all pages of the OTP memory into the corresponding pages of the DCRW. This is required in order to confirm if the OTP contents have already been finalised (see Section 14.4.5). The previous contents of the DCRW registers will be lost when the PROGRAM state is entered.

The transition into the PROGRAM state can be confirmed by reading the MAIN_STATE register field as defined in Section 11.2. When the MAIN_STATE register reads back a value of 01011, then the WM8311 is in the PROGRAM state.

In the PROGRAM state, the ICE and OTP commands are initiated by further writes to the OTP Control Register (R16394), as described in the following sections.

To exit the PROGRAM state and resume normal operations, a Device Reset must be scheduled.

14.4.2 OTP / ICE READ COMMAND

The Read command loads either one or all data pages from the ICE or OTP into the corresponding page(s) of the DCRW. The Read commands are selected by writing 1 to the OTP_READ bit.

To read the OTP, the OTP_MEM bit should be set to 1. To read the ICE, the OTP_MEM bit should be set to 0.

The Read Margin Level is selected by setting the OTP_READ_LVL. Note that this register relates to the OTP only; it has no effect on ICE Read commands. The recommended setting for the OTP Read command is ‘Normal’ level. The OTP_READ_LVL field should be set to 00b.

To read a single memory page, the applicable page is selected by setting the OTP_PAGE field. To read all memory pages, the OTP_BULK bit should be set to 1.

Note that the OTP_PAGE field is defined differently for ICE pages and for OTP pages, as detailed in Section 14.4.6.

All other bits in the OTP Control Register should be set to 0 when a Read command is issued. (Note that OTP_PROG should be set to 0 when a Read command is issued.)

For typical applications, the Bulk Read commands are recommended. The OTP Control Register contents for the OTP / ICE Bulk Read Commands are detailed in Table 23.

READ COMMAND	OTP CONTROL REGISTER VALUE
ICE Read All	0120h
OTP Read All	2120h

Table 23 OTP / ICE Read Command

14.4.3 OTP WRITE COMMAND

The Write command programs one or all data pages of the OTP with data from the corresponding page(s) of the DCRW. The Write commands are selected by writing 1 to the OTP_WRITE bit.

The OTP memory is selected by setting the OTP_MEM bit to 1. (Note that the WM8311 does not support programming the external ICE memory.)

To write a single memory page, the applicable page is selected by setting the OTP_PAGE field. To write all memory pages, the OTP_BULK bit should be set to 1.

Note that Page 0 and Page 1 will be programmed during manufacture, and cannot be re-written. OTP Write is then only possible to Page 2 and Page 3. Selecting the OTP_BULK bit will select OTP Write to Page 2 and Page 3 only.

Note that selecting the OTP_BULK option will cause an OTP Error to be indicated (see Section 14.5). This is because the Bulk Write to Page 0 and Page 1 is not permitted after the factory configuration of the WM8311. It is still possible to Verify the OTP Bulk Write, but the OTP_ERR_EINT flag must be cleared before doing so. The recommended procedure is to Write Page 2 and Page 3 using single page OTP Write commands.

All other bits in the OTP Control Register should be set to 0 when a Write command is issued. (Note that OTP_PROG should be set to 0 when a Write command is issued.)

The programming supply voltage PROGVDD is required for the OTP Write command. It is also necessary to overdrive the LDO12VOUT pin from an external supply. See Section 6 for details of the required supply voltages.

For typical applications, it is recommended to Write Page 2 and Page 3 in two separate commands. The OTP Control Register contents for these OTP Write Commands are detailed in Table 24.

WRITE COMMAND	OTP CONTROL REGISTER VALUE
OTP Write Page 2	2202h
OTP Write Page 3	2203h

Table 24 OTP Write Command

14.4.4 OTP VERIFY COMMAND

The Verify command compares one or all data pages of the OTP with data in the corresponding page(s) of the DCRW. The Verify commands are selected by writing 1 to the OTP_VERIFY bit.

The OTP memory is selected by setting the OTP_MEM bit to 1. (Note that the WM8311 does not support verifying the external ICE memory.)

The Read Margin Level is selected by setting the OTP_READ_LVL. The recommended setting for the OTP Verify command is Margin 1. The OTP_READ_LVL field should be set to 10b.

To verify a single memory page, the applicable page is selected by setting the OTP_PAGE field. To verify all memory pages, the OTP_BULK bit should be set to 1.

All other bits in the OTP Control Register should be set to 0 when a Verify command is issued. (Note that OTP_PROG should be set to 0 when a Verify command is issued.)

If the OTP Verify operation is unsuccessful (ie. the WM8311 detects a difference between the selected pages of the OTP and DCRW memories), then this is indicated by the OTP_ERR_EINT Interrupt flag, as described in Section 14.5.

Note that, when Verifying the OTP after it has been Finalised, the CUST_OTP_FINAL bit needs to be set in the DCRW using a register write to R30736 prior to the OTP_VERIFY operation. This is because the OTP_FINAL command does not set the CUST_OTP_FINAL bit in the DCRW; it only sets it in the OTP memory. If the CUST_OTP_FINAL bit is not set in DCRW, then the OTP_VERIFY command will result in an OTP error indication.

The OTP Control Register contents for all OTP Verify Commands are detailed in Table 25.

VERIFY COMMAND	OTP CONTROL REGISTER VALUE
OTP Verify Page 0	2480h
OTP Verify Page 1	2481h
OTP Verify Page 2	2482h
OTP Verify Page 3	2483h
OTP Verify All	24A0h

Table 25 OTP Verify Command (Margin 1)

14.4.5 OTP FINALISE COMMAND

The Finalise command sets the OTP finalise bit for the user-programmable pages of the OTP memory. The Finalise commands are selected by writing 1 to the OTP_FINAL bit.

Note that Page 0 and Page 1 will be programmed and finalised during manufacture; these memory pages cannot be re-written by users. Following the user Finalise command, Page 2 and Page 3 of the OTP memory will be prevented from any further OTP Write commands. Each page of the OTP memory can be programmed only once; the OTP Finalise command ensures that any subsequent Write commands will have no effect and that the OTP contents are maintained securely.

The OTP memory is selected by setting the OTP_MEM bit to 1. (Note that the WM8311 does not support this function on the external ICE memory.)

The Customer Finalise bit (CUST_OTP_FINAL) is in Page 2. This page is selected by setting OTP_PAGE = 10. Note that the Page 2 finalise bit locks the contents of Page 2 and Page 3.

All other bits in the OTP Control Register should be set to 0 when a Finalise command is issued. (Note that OTP_PROG should be set to 0 when a Finalise command is issued.)

The programming supply voltage PROGVDD is required for the OTP Finalise command. It is also necessary to overdrive the LDO12VOUT pin from an external supply. See Section 6 for details of the required supply voltages.

Note that the OTP_FINAL command does not set the CUST_OTP_FINAL bit in the DCRW; it only sets it in the OTP memory. Care is required when verifying a Finalised OTP page, to avoid an OTP error indication, as described in Section 14.4.4.

The OTP Control Register contents for the OTP Finalise Command is detailed in Table 26. This is the only recommended OTP Finalise Command; no variants of the Finalise Command should be used.

FINALISE COMMAND	OTP CONTROL REGISTER VALUE
OTP Finalise Page 2 (Note that this command finalises the contents of OTP Page 2 and Page 3.)	2802h

Table 26 OTP Finalise Command

14.4.6 OTP CONTROL REGISTER

The OTP Control register (R16394) is defined in Table 27. Note that some of the OTP Programming registers are locked by the WM8311 User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16394 (400Ah) OTP Control	15	OTP_PROG	0	Selects the PROGRAM device state. 0 = No action 1 = Select PROGRAM mode Note that, after PROGRAM mode has been selected, the chip will remain in PROGRAM mode until a Device Reset. *Protected by user key*
	13	OTP_MEM	1	Selects ICE or OTP memory for Program commands. 0 = ICE 1 = OTP *Protected by user key*
	11	OTP_FINAL	0	Selects the FINALISE command, preventing further OTP programming. 0 = No action 1 = Finalise Command *Protected by user key*
	10	OTP_VERIFY	0	Selects the VERIFY command for the selected OTP memory page(s).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				0 = No action 1 = Verify Command *Protected by user key*
	9	OTP_WRITE	0	Selects WRITE command for the selected OTP memory page(s). 0 = No action 1 = Write Command *Protected by user key*
	8	OTP_READ	0	Selects READ command for the selected memory page(s). 0 = No action 1 = Read Command *Protected by user key*
	7:6	OTP_READ_LVL [1:0]	00	Selects the Margin Level for READ or VERIFY OTP commands. 00 = Normal 01 = Reserved 10 = Margin 1 11 = Margin 2 *Protected by user key*
	5	OTP_BULK	0	Selects the number of memory pages for ICE / OTP commands. 0 = Single Page 1 = All Pages
	1:0	OTP_PAGE [1:0]	00	Selects the single memory page for ICE / OTP commands (when OTP_BULK=0). If OTP is selected (OTP_MEM = 1): 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 If ICE is selected (OTP_MEM = 0): 00 = Page 2 01 = Page 3 10 = Page 4 11 = Reserved

Table 27 OTP Memory Control

14.5 OTP / ICE INTERRUPTS

The OTP and ICE memories are associated with two Interrupt event flags.

The OTP_CMD_END_EINT interrupt is set each time an OTP / ICE Command has completed or if OTP Auto-Program has completed. (See Section 14.4 for a definition of the OTP and ICE Commands. See Section 14.6.3 for details of the OTP Auto-Program function.)

The OTP_ERR_EINT interrupt is set when an OTP / ICE Error has occurred. The errors detected include ICE Read Failure, OTP Verify Failure and attempted OTP Write to a page that has been ‘Finalised’.

Each of these secondary interrupts triggers a primary OTP Memory Interrupt, OTP_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 75.

Note that OTP_CMD_END_EINT is triggered during the normal start-up and shutdown operations, when the WM8311 accesses the OTP and/or ICE memories. For typical applications, it is recommended that the OTP_CMD_END_EINT interrupt should be masked at all times except when performing user-initiated OTP/DBE commands.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	5	OTP_CMD_END_EINT	OTP / ICE Command End interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	4	OTP_ERR_EINT	OTP / ICE Command Fail interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16410 (401Ah) Interrupt Status 2 Mask	5	IM_OTP_CMD_END_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	4	IM_OTP_ERR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 28 OTP Memory Interrupts

14.6 DCRW MEMORY CONTENTS

The DCRW is the ICE/OTP Register Window, as described in Section 14.2. Under normal operating conditions, this memory area is initialised with data from the integrated OTP or an external ICE memory. The DCRW memory addresses range from R30720 (7800h) to R30759 (7827h). The complete register map definition is described in Section 28.

The register fields in the DCRW allow the start-up configuration of the DC-DC Converters, the LDO Regulators, GPIO pins 1-6 and Status LED outputs to be programmed. The DCRW also provides control of the Battery Charger, Clocking, USB Current Limit and the Start-Up (SYSOK) voltage threshold.

Most of the DCRW contents are duplicates of control registers that exist in the main register area below the DCRW addresses. In theses cases, reading or writing to either address will have the same effect.

Some register fields are defined only in the DCRW area; a detailed description of these fields is provided in the following sub-sections.

14.6.1 DCRW PAGE 0

Page 0 of the DCRW occupies register addresses R30720 (7800h) to R30727 (7807h). This contains factory-preset data which is loaded from OTP when an ‘ON’ state transition is scheduled.

Page 0 of the DCRW contains a 128-bit unique ID. Note that these fields are Read-Only in the OTP and cannot be changed.

14.6.2 DCRW PAGE 1

Page 1 of the DCRW occupies register addresses R30728 (7808h) to R30735 (780Fh). This contains factory-preset data which is loaded from OTP when an ‘ON’ state transition is scheduled.

Page 1 of the DCRW contains trim parameters that ensure the accuracy of the voltage references and the power management RC oscillator. Note that these fields are Read-Only in the OTP and cannot be changed.

14.6.3 DCRW PAGE 2

Page 2 of the DCRW occupies register addresses R30736 (7810h) to R30743 (7817h). This contains user-programmable data.

This page of data is normally loaded from OTP when 'ON' state transition is scheduled (except in Development Mode or if RECONFIG_AT_ON = 0). This page of data can also be loaded from OTP using the OTP_READ command; it can be written to the OTP using the OTP_WRITE command.

This page of data is loaded from the first page of ICE memory (00h to 0Fh) when 'ON' state transition is scheduled in Development Mode (if RECONFIG_AT_ON = 1). This page of data can also be loaded from ICE using the ICE Read command. Note that ICE Address 00h corresponds to bits 15:8 at the start address of DCRW Page 2; ICE Address 01h corresponds to bits 7:0 at the same DCRW address.

If the WM8311 configuration data is loaded from external ICE in response to an 'ON' state transition request, and the OTP_AUTO_PROG register bit is set, then the WM8311 will program the OTP with the contents Page 2 and Page 3 of the DCRW data, after the ICE data has been loaded and confirmed as valid. The WM8311 will also perform a Margin 1 Verify as part of the auto-program function.

The programming supply voltage PROGVDD is required for the OTP_AUTO_PROG command. It is also necessary to overdrive the LDO12VOUT pin from an external supply. See Section 6 for details of the required supply voltages.

Using the auto-program function described above, the OTP will be finalised if the OTP_CUST_FINAL bit is set in the ICE data. Completion of the auto-program is indicated using the OTP interrupts, as described in Section 14.5. The auto-program completion is also indicated on the Status LED outputs, as described in Section 22.

The OTP_CUST_ID field is used to hold a Customer Identifier for the OTP data contents. Whenever an 'ON' state transition is requested, then the OTP_CUST_ID field is checked to confirm valid OTP data. If the OTP_CUST_ID field is set to zero, then the WM8311 remains in the OFF power state. A non-zero OTP_CUST_ID field is used to confirm valid OTP contents.

The OTP_CUST_FINAL bit is used to control whether the user-programmable OTP data (Page 2 and Page 3) is finalised. If OTP_CUST_FINAL is set in the OTP and also set in the DCRW, then the WM8311 prevents any further Writes to the OTP. If the DCRW has been loaded from the OTP, then the OTP_CUST_FINAL bit indicates whether any further Write operations are possible. If the DCRW has been loaded from the ICE, and the OTP auto-programming option is selected (see above), then the value of the OTP_CUST_FINAL bit will be copied from the ICE memory to the OTP memory.

The above registers are defined in Table 29.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30736 (7810h) Customer OTP ID	15	OTP_AUTO_PROG	0	If this bit is set when bootstrap data is loaded from ICE (in development mode), then the ICE contents will be programmed in the OTP.
	14:1	OTP_CUST_ID [13:0]	0000h	This field is checked when an 'ON' transition is requested. A non-zero value is used to confirm valid data.
	0	OTP_CUST_FINAL	0	If OTP_CUST_FINAL is set in the OTP and also set in the DCRW, then no further Writes are possible to the OTP.

Table 29 OTP Registers - DCRW Page 2

The remaining contents of DCRW Page 2 include the registers listed in Table 30, which are defined in other sections of this datasheet.

REGISTER	FUNCTION	REFERENCE
DC1_ON_SLOT [2:0]	DC-DC Converter 1	See Section 15.12.2
DC1_FREQ [1:0]		See Section 15.12.2
DC1_PHASE		See Section 15.12.2
DC1_ON_VSEL [6:2]		See Section 15.12.2

REGISTER	FUNCTION	REFERENCE
DC1_CAP [1:0]		See Section 15.12.2
DC2_ON_SLOT [2:0]	DC-DC Converter 2	See Section 15.12.2
DC2_FREQ [1:0]		See Section 15.12.2
DC2_PHASE		See Section 15.12.2
DC2_ON_VSEL [6:2]		See Section 15.12.2
DC2_CAP [1:0]		See Section 15.12.2
DC3_ON_SLOT [2:0]	DC-DC Converter 3	See Section 15.12.2
DC3_PHASE		See Section 15.12.2
DC3_ON_VSEL [6:2]		See Section 15.12.2
DC3_CAP [1:0]		See Section 15.12.2
LDO1_ON_SLOT [2:0]	LDO Regulator 1	See Section 15.12.4
LDO1_ON_VSEL [4:0]		See Section 15.12.4
LDO2_ON_SLOT [2:0]	LDO Regulator 2	See Section 15.12.4
LDO2_ON_VSEL [4:0]		See Section 15.12.4
LDO3_ON_SLOT [2:0]	LDO Regulator 3	See Section 15.12.4
LDO3_ON_VSEL [4:0]		See Section 15.12.4
LDO4_ON_SLOT [2:0]	LDO Regulator 4	See Section 15.12.4
LDO4_ON_VSEL [4:0]		See Section 15.12.4
LDO5_ON_SLOT [2:0]	LDO Regulator 5	See Section 15.12.4
LDO5_ON_VSEL [4:0]		See Section 15.12.4
LDO7_ON_SLOT [2:0]	LDO Regulator 7	See Section 15.12.4
LDO7_ON_VSEL [4:0]		See Section 15.12.4

Table 30 DCRW Page 2

14.6.4 DCRW PAGE 3

Page 3 of the DCRW occupies register addresses R30744 (7818h) to R30751 (781Fh). This contains user-programmable data.

This page of data is normally loaded from OTP when 'ON' state transition is scheduled (except in Development Mode or if RECONFIG_AT_ON = 0). This page of data can also be loaded from OTP using the OTP_READ command; it can be written to the OTP using the OTP_WRITE command.

This page of data is loaded from the second page of ICE memory (10h to 1Fh) when 'ON' state transition is scheduled in Development Mode (if RECONFIG_AT_ON = 1). This page of data can also be loaded from ICE using the ICE Read command. Note that ICE Address 10h corresponds to bits 15:8 at the start address of DCRW Page 3; ICE Address 11h corresponds to bits 7:0 at the same DCRW address.

The contents of DCRW Page 3 include the registers listed in Table 31.

REGISTER	FUNCTION	REFERENCE
LDO11_ON_SLOT [2:0]	LDO Regulator 11	See Section 15.12.4
LDO11_ON_VSEL [3:0]		See Section 15.12.4
EPE1_ON_SLOT [2:0]	External Power Converter Enable	See Section 15.12.5
EPE2_ON_SLOT [2:0]		See Section 15.12.5
GP1_DIR	GPIO1	See Section 21.3
GP1_PULL [1:0]		See Section 21.3
GP1_INT_MODE		See Section 21.3
GP1_PWR_DOM		See Section 21.3
GP1_POL		See Section 21.3
GP1_OD		See Section 21.3
GP1_ENA		See Section 21.3
GP1_FN [3:0]		See Section 21.3
GP2_DIR	GPIO2	See Section 21.3
GP2_PULL [1:0]		See Section 21.3

REGISTER	FUNCTION	REFERENCE
GP2_INT_MODE		See Section 21.3
GP2_PWR_DOM		See Section 21.3
GP2_POL		See Section 21.3
GP2_OD		See Section 21.3
GP2_ENA		See Section 21.3
GP2_FN [3:0]		See Section 21.3
GP3_DIR	GPIO3	See Section 21.3
GP3_PULL [1:0]		See Section 21.3
GP3_INT_MODE		See Section 21.3
GP3_PWR_DOM		See Section 21.3
GP3_POL		See Section 21.3
GP3_OD		See Section 21.3
GP3_ENA		See Section 21.3
GP3_FN [3:0]		See Section 21.3
GP4_DIR	GPIO4	See Section 21.3
GP4_PULL [1:0]		See Section 21.3
GP4_INT_MODE		See Section 21.3
GP4_PWR_DOM		See Section 21.3
GP4_POL		See Section 21.3
GP4_OD		See Section 21.3
GP4_ENA		See Section 21.3
GP4_FN [3:0]		See Section 21.3
GP5_DIR	GPIO5	See Section 21.3
GP5_PULL [1:0]		See Section 21.3
GP5_INT_MODE		See Section 21.3
GP5_PWR_DOM		See Section 21.3
GP5_POL		See Section 21.3
GP5_OD		See Section 21.3
GP5_ENA		See Section 21.3
GP5_FN [3:0]		See Section 21.3
GP6_DIR	GPIO6	See Section 21.3
GP6_PULL [1:0]		See Section 21.3
GP6_INT_MODE		See Section 21.3
GP6_PWR_DOM		See Section 21.3
GP6_POL		See Section 21.3
GP6_OD		See Section 21.3
GP6_ENA		See Section 21.3
GP6_FN [3:0]		See Section 21.3
CLKOUT_SLOT [2:0]	Clocking	See Section 13.1
CLKOUT_SRC		See Section 13.1
XTAL_ENA		See Section 13.1
XTAL_INH		See Section 13.1
FLL_AUTO_FREQ [2:0]		See Section 13.3
USB_ILIM [2:0]	USB Configuration	See Section 17.4
USB100MA_STARTUP [1:0]		See Section 17.4
CHG_ENA	Battery Charger Enable	See Section 17.7
WDOG_ENA	Watchdog Timer	See Section 25
LED1_SRC [1:0]	System Status LED Drivers	See Section 22.2
LED2_SRC [1:0]		See Section 22.2
SYSOK_THR [2:0]	Supply Voltage Monitoring	See Section 24.4

Table 31 DCRW Page 3

14.6.5 DCRW PAGE 4

Page 4 of the DCRW occupies register addresses R30752 (7820h) to R30759 (7827h).

This page of data is loaded from the third page of ICE memory (20h to 2Fh) when 'ON' state transition is scheduled in Development Mode. This page of data can also be loaded from ICE using the ICE Read command. Note that ICE Address 20h corresponds to bits 15:8 at the start address of DCRW Page 4; ICE Address 21h corresponds to bits 7:0 at the same DCRW address.

The ICE_VALID_DATA register is used to hold a validation field for the ICE data contents. If the WM8311 configuration data is loaded from the external ICE in response to an 'ON' state transition request in Development Mode, then the ICE_VALID_DATA field is checked to confirm valid ICE data.

The ICE data is deemed valid if the ICE_VALID_DATA field contains the value A596h. If the ICE is not connected or contains invalid data, then the WM8311 remains in the OFF power state until a Device Reset.

The ICE_VALID_DATA register is defined in Table 32.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30759 (7827h) ICE CHECK DATA	15:0	ICE_VALID_ DATA [15:0]	0000h	This field is checked in development mode when an 'ON' transition is requested. A value of A596h is required to confirm valid data.

Table 32 ICE Registers - DCRW Page 5

15 POWER MANAGEMENT

15.1 GENERAL DESCRIPTION

The WM8311 provides 4 DC-DC Converters and 7 LDO Regulators. The DC-DC Converters comprise 3 step-down (Buck) converters and 1 step-up (Boost) converter. The Regulators comprise general purpose LDOs (LDO1 - LDO5) and a low-noise analogue LDO (LDO7). The analogue LDO offers superior PSRR, noise and load-transient performance. LDO11 is a low power LDO intended for powering “always on” circuits connected to the WM8311; this LDO can be configured to remain enabled in the OFF state.

These power management components are designed to support application processors and associated peripherals. DC-DC1 and DC-DC2 are intended to provide power to the processor voltage domains; DC-DC3 is suitable for powering memory circuits or for use as a pre-regulator for the LDOs. The output voltage of each of the buck converters and regulators is programmable in software through control registers.

The WM8311 can execute programmable sequences of enabling and disabling the DC-DC Buck Converters and LDO Regulators as part of the transitions between the ON, OFF and SLEEP power states. The WM8311 power management circuits can also interface with configurable hardware control functions supported via GPIO pins. These include GPIO inputs for selecting alternate voltages or operating modes, and GPIO outputs for controlling external power management circuits.

The configuration of the power management circuits, together with some of the GPIO pins and other functions, may be stored in the integrated OTP memory. This avoids any dependence on a host processor to configure the WM8311 at start-up. See Section 14 for details of the OTP memory.

15.2 DC-DC CONVERTER AND LDO REGULATOR CONTROL

The integrated DC-DC Converters and LDO Regulators can each be enabled in the ON or SLEEP power states by setting the DC*m*_ENA or LDO*n*_ENA bits as defined in Section 15.12.1. Note that setting the DC*m*_ENA or LDO*n*_ENA bits in the OFF state will not enable the DC-DC Converters or LDO Regulators. These bits should not be written to when the WM8311 is in the OFF state; writing to these bits in the OFF state may cause a malfunction.

In many applications, there will be no need to write to the DC*m*_ENA or LDO*n*_ENA bits, as these bits are controlled by the WM8311 when a power state transition is scheduled. Dynamic, run-time control of the DC-DC Converters or LDO Regulators is also possible by writing to these registers. Note that the DC-DC4 Boost Converter cannot be configured as part of the power state transitions; this Converter must always be enabled by writing to the DC4_ENA bit.

The DC-DC Converters and LDO Regulators can be assigned to a Hardware Enable (GPIO) input for external enable/disable control. In this case, the converter or regulator is not affected by the associated DC*m*_ENA or LDO*n*_ENA bits. See Section 15.3 for further details.

The WM8311 can also control other circuits, including external DC-DC Converters or LDO Regulators using the External Power Enable (EPE) outputs. The External Power Enable outputs are alternate functions supported via GPIO - see Section 21. The External Power Enable outputs can be controlled in the same way as the internal DC-DC Converters and LDO Regulators. The associated control bits are EPE1_ENA and EPE2_ENA, as defined in Section 15.12.1.

LDO Regulator 11 is a Low Power LDO Regulator, which is configured differently to the other LDOs. It is a low-power LDO intended for “Always-On” functions external to the WM8311 and can be enabled when the WM8311 is in the OFF power state.

When LDO11_FRCENA is set, then LDO11 is enabled at all times in the OFF, ON and SLEEP states. Note that LDO11 is always disabled in the BACKUP and NO POWER states. See Section 15.12.4 for the definition of LDO11_FRCENA.

The current commanded state of each of the DC-DC Converters, LDO Regulators and EPE outputs is indicated in the DC*m*_STS, LDO*n*_STS and EPE*n*_STS register bits.

If a fault condition causes any converter or regulator to be disabled, then the associated _ENA and _STS fields are reset to 0.

15.3 TIMESLOT CONTROL AND HARDWARE ENABLE (GPIO) CONTROL

The DC-DC Converters 1-3 and LDO Regulators 1-5, 7 and 11 may be programmed to switch on in a selected timeslot within the ON sequence using the DC*m*_ON_SLOT or LDO*n*_ON_SLOT fields. These register fields are defined in Section 15.12.2 and Section 15.12.4. Alternatively, these fields can be used to assign a converter / regulator to one of the Hardware Enable Inputs. (The Hardware Enable Inputs are alternate functions supported via GPIO - see Section 21.)

Converters / regulators which are assigned to one of the Hardware Enable Inputs are enabled or disabled according to the logic level of the respective GPIO input in the ON or SLEEP power states. The Hardware Enable Inputs are effective from the end of the ON sequence until the start of the OFF sequence. Note that the GPIO Hardware Enable function is not the same as the GPIO Hardware Control function.

Any converters / regulators which are assigned to timeslots within the ON sequence will be disabled in the reverse sequence when an OFF sequence is scheduled. Any converters / regulators which are not assigned to timeslots, or are assigned to Hardware Enable Inputs, will be disabled immediately at the start of the OFF sequence.

Each of the converters / regulators may also be programmed to be disabled in a selected timeslot within the SLEEP sequence using the DC*m*_SLP_SLOT or LDO*n*_SLP_SLOT fields. In the case of converters / regulators which are not disabled by the SLEEP sequence, these fields determine in which timeslot each converter or regulator enters its SLEEP configuration.

Any converters / regulators which are disabled as part of the SLEEP sequence will be enabled in the reverse sequence when a WAKE transition is scheduled.

By default, the OFF sequence is the reverse of the ON sequence. Similarly, the WAKE sequence is the reverse of the SLEEP sequence. If a different behaviour is required, this can be achieved by writing to the _ON_SLOT or _SLP_SLOT registers between transitions in order to re-define the sequences.

Any converters / regulators which are assigned to Hardware Enable Inputs will remain under control of the Hardware Enable Inputs in the SLEEP power state. In this case, the DC*m*_SLP_SLOT or LDO*n*_SLP_SLOT fields determine in which timeslot the converter / regulator enters its SLEEP configuration.

The WM8311 will control the DC*m*_ENA or LDO*n*_ENA bit (see Section 15.2) for any converter / regulator that is enabled or disabled during the power state transitions. In the case of a converter / regulator assigned to a Hardware Enable (GPIO) input, the DC*m*_ENA or LDO*n*_ENA bit is not controlled and the converter / regulator is not affected by this bit.

The DC-DC converters include a soft-start feature that limits in-rush current at start-up. However, in order to further reduce supply in-rush current, it is recommended that the individual converters are programmed to start up in different time slots within the start-up sequence, as described in Section 11.3.

Similarly, it is recommended that the individual LDO regulators are programmed to start up in different time slots within the start-up sequence, as described in Section 11.3.

Note that the DC-DC4 Boost Converter cannot be configured as part of the power state transitions; this Converter must always be enabled by writing to the DC4_ENA bit.

The External Power Enable (EPE) outputs, EPE1 and EPE2, may also be assigned to timeslots in the ON / SLEEP sequences or assigned to Hardware Enable inputs using the EPE*n*_ON_SLOT and EPE*n*_SLP_SLOT fields described in 15.12.5.

Note that a transition from the SLEEP state to the OFF state is not a controlled transition. If an ‘OFF’ event occurs whilst in the SLEEP state, then the WM8311 will select the OFF state, but all the enabled converters and regulators will be disabled immediately; the time-controlled sequence is not implemented in this case. See Section 11.3 for details of the WM8311 ‘OFF’ events.

15.4 OPERATING MODE CONTROL

15.4.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

The DC-DC (Buck) Converters DC-DC1, DC-DC2 and DC-DC3 can be configured to operate in four different operating modes. The operating modes are summarised in Table 33. For more detailed information on the DC-DC (Buck) Converter operating modes, see Section 15.15.2.

DC-DC CONVERTER OPERATING MODE	DESCRIPTION
Forced Continuous Conduction Mode (FCCM)	High performance mode for all static and transient load conditions.
Auto Mode: Continuous / Discontinuous Conduction with Pulse-Skipping Mode (CCM/DCM with PS)	High efficiency mode for all static and transient load conditions. Performance may be less than FCCM mode for heavy load transients.
Hysteretic Mode	High efficiency mode for light static and light transient loads only. Maximum load current is restricted; output voltage ripple is increased.
LDO Mode	Power saving mode for light loads only. High efficiency for ultra light loads. Low current soft-start control.

Table 33 DC-DC Synchronous Buck Converters Operating Modes

The operating mode of the DC-DC Converters in the ON power state is selected using the DC*m*_ON_MODE register fields. The operating mode of the DC-DC Converters in the SLEEP power state is selected using the DC*m*_SLP_MODE register fields.

When changing the operating mode of the DC-DC Converters in preparation for an increased load, a set-up time of 100μs should be allowed for the operating mode to be established before applying the new load.

Note that the operating mode of the DC-DC Converters may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.9 for details of Hardware Control.

Note that, for minimum DC-DC3 quiescent current in LDO mode, the converter must first be enabled in FCCM, CCM/DCM with PS or Hysteretic mode, before LDO mode is selected.

15.4.2 DC-DC BOOST CONVERTERS

The DC-DC4 Boost Converter is enabled by setting the DC4_ENA bit as described in Section 15.2. Note that this Converter cannot be enabled automatically under timeslot control in the ON transition. However, the Converter can either be disabled or unchanged in the SLEEP transition, as determined by DC4_SLPENA.

The Boost Converter is intended to be used as a power supply for either of the Current Sinks, ISINK1 or ISINK2 (see Section 16). The Boost Converter must be configured for the applicable Current Sink using the DC4_FBSRC bit.

When the DC-DC4 Boost Converter is enabled, its output voltage is regulated in such a way that the selected ISINK voltage (at ISINK1 or ISINK2) is 0.5V. Output voltages of up to 30V can be generated in order to support the current that has been selected for the ISINK. The required voltage range must be set using the DC4_RANGE field in order to ensure stable operation.

If the Boost Converter is used to provide a supply for both ISINKs simultaneously, then the DC4_RANGE and DC4_FBSRC bits should be set according to whichever of the ISINKs requires the higher supply voltage.

15.4.3 LDO REGULATORS

The LDO Regulators LDO1 - LDO5 and LDO10 can be configured to operate in Normal operating mode or in Low Power mode.

The operating mode of the LDO Regulators in the ON power state is selected using the LDO*n*_ON_MODE register fields. The operating mode of the LDO Regulators in the SLEEP power state is selected using the LDO*n*_SLP_MODE register fields.

For the standard LDOs, LDO1 - LDO5, two different Low Power modes are provided, offering limited load current capability and reduced quiescent current. When Low Power mode is selected in the ON or SLEEP power states, then the LDO*n*_LP_MODE register bits determine which Low Power mode is selected.

Note that the operating mode and output voltage of the LDO Regulators may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.9 for details of Hardware Control.

15.5 OUTPUT VOLTAGE CONTROL

15.5.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

The output voltage of the DC-DC Converters 1-3 in the ON power state is selected using the DC*m*_ON_VSEL register fields. The output voltage of these converters in the SLEEP power state is selected using the DC*m*_SLP_VSEL register fields.

DC-DC Converters 1 and 2 support two different switching frequencies, as described in Section 15.6. Note that the supported output voltage range for these converters is restricted in the 4MHz mode; for output voltages greater than 1.4V, the 2MHz mode must be used.

The DC-DC Converters are dynamically programmable - the output voltage may be adjusted in software at any time. These converters are step-down converters; their output voltage can therefore be lower than the input voltage, but cannot be higher.

Note that the output voltage of DC-DC Converters 1 and 2 may also be controlled using the Dynamic Voltage Scaling features described in Section 15.6. Software control (using register writes) and hardware control (using the Hardware DVS Control inputs supported via GPIO) is supported.

Note that the output voltage of the DC-DC Converters may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.9 for details of Hardware Control.

When changing the output voltage of DC-DC Converters 1 and 2, the GPIO output “DC-DC*m* DVS Done” can be used to confirm the DVS Control has completed; see Section 15.6 for details.

15.5.2 DC-DC BOOST CONVERTERS

The output voltage of the DC-DC4 Boost Converter is set as described in Section 15.4.3. The voltage is not commanded directly, but is regulated automatically by the WM8311 in order to support the current that has been commanded for the selected Current Sink (ISINK).

15.5.3 LDO REGULATORS 1-5 AND LDO7

The output voltage of the LDO Regulators 1-5 and 7 in the ON power state is selected using the LDO*n*_ON_VSEL register fields. The output voltage of the LDO Regulators in the SLEEP power state is selected using the LDO*n*_SLP_VSEL register fields.

The LDO Regulators are dynamically programmable - the output voltage may be adjusted in software at any time.

Note that the output voltage of the LDO Regulators may also be controlled by the Hardware Control inputs. The Hardware Control inputs are alternate functions supported via GPIO. See Section 15.9 for details of Hardware Control.

15.5.4 LDO REGULATOR 11

The output voltage of LDO11 can be set in two ways - it can be commanded directly, or it can be commanded to follow the DC-DC Converter 1 output voltage.

When LDO11_VSEL_SRC = 0, then the output voltage of LDO11 is set by LDO11_ON_VSEL (in the ON state) or by LDO11_SLP_VSEL (in the SLEEP state) in the same way as the other LDOs.

When LDO11_VSEL_SRC = 1, the output voltage of LDO11 follows the output voltage of DC-DC Converter 1. This enables both domains to be changed at the same time, eg. the processor core and processor 'alive' domains. In this case, the LDO11 output voltage follows DC1_ON_VSEL or DC1_SLP_VSEL in the ON state or SLEEP state respectively.

Note that, when LDO11_VSEL_SRC = 1, the LDO11 regulator adopts the nearest achievable output voltage, which may not be identical to the DC-DC1 voltage, due to the more limited range and resolution of LDO11 - the output voltage of LDO11 is in the range 0.8V to 1.55V in 50mV steps; the output voltage of DC-DC1 is in the range 0.6V to 1.8V in 12.5mV steps. If DC-DC1 is disabled, then the LDO11 voltage tracking feature is not supported, and the LDO11 output voltage will be 0.8V.

15.6 DC-DC SYNCHRONOUS BUCK CONVERTER CONTROL

Soft-Start control is provided for each of the DC-DC synchronous buck converters, using the DC*m*_SOFT_START register fields. When a DC-DC Converter is switched on, the soft-start circuit will apply current limiting in order to control the in-rush current. For DC-DC1 and DC-DC2, the current limit is increased through up to 8 stages to the full load condition. The DCm_SOFT_START registers select the duration of these stages. (Note that, under light loads, the full start-up may be achieved in fewer than 8 stages.) A similar function is provided for DC-DC3, but only 3 intermediate stages are implemented for this converter.

When DC-DC3 is operating in Hysteretic Mode, the maximum DC output current can be set using the DC3_STNBY_LIM register. See Section 15.4.1 for details of the DC-DC3 operating modes.

To ensure stable operation, the register fields DC*m*_CAP must be set for each of the DC-DC Converters according to the output capacitance. (Note that these fields are set via OTP/ICE settings only; they cannot be changed by writing to the control register.) The choice of output capacitor is described in Section 30.3.

When a DC-DC Converter is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using DC*m*_FLT.

DC-DC Converters 1 and 2 also support selectable switching frequency. This can either be 2MHz or 4MHz, according to the DC*m*_FREQ register field. (Note that these fields are set via OTP/ICE settings only; they cannot be changed by writing to the control register.) The switching frequency of DC-DC3 is fixed at 2MHz.

Note that the supported output voltage range for DC-DC Converters 1 and 2 is restricted in the 4MHz mode; for output voltages greater than 1.4V, the 2MHz mode must be used.

The switching phase of each DC-DC converter can be set using the DC*m*_PHASE bits. Where two converters are operating at the same switching frequency, the supply current ripple can be minimised by selecting a different switching phase for each converter.

The Dynamic Voltage Scaling (DVS) feature on DC-DC1 and DC-DC2 enables hardware or software selection of an alternate output voltage, DC*m*_DVS_VSEL. This may be useful if a short-term variation in output voltage is required.

The DVS voltage (set by DC*m*_DVS_VSEL) may be selected by setting DC*m*_DVS_SRC = 01. Alternatively, the DVS voltage may be selected under control of one of the Hardware DVS Control inputs supported via the GPIO pins. See Section 21 for details of configuring the GPIO pins as Hardware DVS Control inputs.

Whenever the DVS voltage is selected by any method, the DVS selection takes precedence over the ON, SLEEP or Hardware Control (HWC) configuration. See Section 15.9 for details of Hardware Control options.

The output voltage ramp rate is selectable for DC-DC Converters 1 and 2. The DC*m*_RATE field selects the rate of change of output voltage, whether this is in response to an operating mode transition, or any hardware or software command. Note that the DC*m*_RATE field is accurate in Forced Continuous Conduction Mode (FCCM); in other modes, the actual slew rate may be longer in the case of a decreasing output voltage selection, especially under light load conditions.

The WM8311 can indicate the status of the Dynamic Voltage Scaling via a GPIO pin configured as a “DC-DC1 DVS Done” or “DC-DC2 DVS Done” output (see Section 21). When a GPIO pin is configured to indicate the DVS status, this signal is temporarily de-asserted during a DVS transition on the associated DC-DC Converter, and is subsequently asserted to indicate the transition has completed.

Note that the GPIO DVS outputs indicate the progress of all output voltage slews; they are not limited to transitions associated with DC*m*_DVS_SRC; the GPIO DVS output also indicates the status of a slew caused by a write to the DC*m*_ON_VSEL register, or a slew to the DC*m*_SLP_VSEL voltage. Note also that the GPIO DVS outputs are indicators of the DVS control mechanism only; they do not confirm the output voltage accuracy. The output voltage can be checked using the voltage status bits if required (see Section 15.2).

15.7 DC-DC BOOST CONVERTER CONTROL

The DC-DC4 Boost Converter is designed as a power source for the Current Sinks described in Section 16. The associated control registers for DC-DC4 are described in Section 15.4.2.

The Boost Converter uses one or other of the Current Sinks to provide voltage feedback in order to control the converter output voltage. The selected Current Sink is determined by the DC4_FBSRC register bit. If the Boost Converter is used to provide a supply for both ISINKs simultaneously, then the DC4_RANGE and DC4_FBSRC bits should be set according to whichever of the ISINKs requires the higher supply voltage.

It is important to follow the recommended control sequences for switching on/off the Boost Converter and Current Sinks. These sequences are described in Section 16.

The maximum current that can be supported by the Boost Converter varies with the output voltage, as noted in the Electrical Characteristics (see Section 7.2).

The Current Sinks are suited to controlling LED backlight circuits. At low output voltages (eg. 5V), the DC-DC4 boost converter is capable of supporting currents which exceed the maximum current rating of the Current Sinks. Please contact Wolfson Applications support if further guidance is required on configuring DC-DC4 for higher current than is supported by the Current Sinks.

15.8 LDO REGULATOR CONTROL

The LDO Regulators 1-5 and 7 can be configured to act as Current Limited Switches by setting the LDO*n*_SWI field. When this bit is selected, there is no voltage regulation and the operating mode and output voltage controls of the corresponding LDO are ignored. In Switch mode, the switch is enabled (closed) and disabled (opened) by enabling or disabling the LDO.

Note that Switch mode cannot be selected via the OTP memory settings, and must be configured after the WM8311 has entered the ON state.

When the LDO Regulator is disabled (and Switch mode is not selected), the output pin can be configured to be floating or to be actively discharged. This is selected using LDO*n*_FLT.

15.9 HARDWARE CONTROL (GPIO)

The DC-DC Converters, LDO Regulators and EPE outputs may be controlled by the Hardware Control inputs supported via the GPIO pins. The DC*m*_HWC_SRC, LDO*n*_HWC_SRC or EPE*n*_HWC_SRC fields determine which of these Hardware Control inputs is effective.

See Section 21 for details of configuring the GPIO pins as Hardware Control inputs. Note that the GPIO Hardware Control function is not the same as the GPIO Hardware Enable function.

Hardware Control is only possible when the applicable DC*m*_ENA, LDO*n*_ENA or EPE*n*_ENA control bit is set (see Section 15.2), or if a Hardware Enable has been assigned to the relevant function and is asserted.

The action taken in response to the selected Hardware Control inputs is configurable for each DC-DC Converter, LDO Regulator or EPE output. The available options are described below.

When a Hardware Control input is assigned to a DC-DC Buck Converter (DC-DC1, DC-DC2 or DC-DC3), and is asserted, the operating mode and output voltage of the relevant DC-DC Converter is determined by the DC*m*_HWC_VSEL and DC*m*_HWC_MODE fields; this takes precedence over the normal ON or SLEEP settings.

Note that the Hardware Control input can be used to disable a DC-DC Buck Converter if required, by setting DC*m*_HWC_MODE = 01.

When a Hardware Control input is assigned to the DC-DC4 Boost Converter, and is asserted, the Converter is controlled as determined by the DC4_HWC_MODE field; this takes precedence over the normal ON or SLEEP settings. The available options are to disable the Converter, or to remain under control of DC4_ENA.

When a Hardware Control input is assigned to LDO Regulators 1-10, and is asserted, the operating mode and output voltage of the relevant LDO Regulators is determined by the LDO*n*_HWC_VSEL and LDO*n*_HWC_MODE fields; this takes precedence over the normal ON or SLEEP settings.

Note that, for the standard LDOs (LDO1 - LDO5), when Low Power Mode is selected (LDO*n*_HWC_MODE = 00 or 10), then the Low Power mode type is determined by the LDO*n*_LP_MODE register bits.

When a Hardware Control input is assigned to the External Power Enable (EPE) outputs, and is asserted, the relevant EPE outputs are controlled as determined by the EPE*n*_HWC_ENA field; this takes precedence over the normal ON or SLEEP settings. The available options are to de-assert the EPE, or for the EPE to remain under control of EPE*n*_ENA.

15.10 FAULT PROTECTION

Each of the DC-DC Buck Converters (1 to 3) is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the output voltage falls below the required level by more than the applicable undervoltage margin, as specified in Section 7.1.

The DC-DC4 Boost Converter is monitored for voltage accuracy and fault conditions. The voltage at ISINK1 or ISINK2 is monitored as an indicator of an overcurrent condition.

Each LDO Regulator (1 to 5 and 7) is monitored for voltage accuracy and fault conditions. An undervoltage condition is set if the output voltage falls below the required level by more than the undervoltage margin, as specified in Section 7.4.

The DC*m*_ERR_ACT and LDO*n*_ERR_ACT fields configure the fault response to an Undervoltage condition. An Interrupt is always triggered under this condition (see Section 15.13); additional action can also be selected independently for each converter / regulator. The options are to ignore the fault, shut down the converter, or to shut down the system. To prevent false alarms during short current surges, faults are only signalled if the fault condition persists.

If a fault condition is detected, and the selected response is to shut down the converter or regulator, then the associated _ENA and _STS fields are reset to 0, as described in Section 15.2.

If a fault condition is detected, and the selected response is to shut down the system, then a Device Reset is triggered, as described in Section 24.1, forcing a transition to the OFF state. The WM8311 will automatically return to the ON state after performing the Device Reset.

Note that, if the fault condition persists, then a maximum of 6 Device Resets will be attempted to initiate the start-up sequence. If the sequence fails more than 6 times, the WM8311 will remain in the OFF state until the next valid ON state transition event occurs.

Note that the DC-DC4 Boost Converter will not be automatically enabled following a Device Reset; this must be re-enabled using the DC4_ENA bit if required.

Note that DC-DC1 and DC-DC2 overvoltage and high current conditions can be detected and reported as described in Section 15.11. The DC*m*_ERR_ACT fields have no relation to these conditions.

The DC-DC3 Buck Converter has a selectable overvoltage protection feature, controlled by DC3_OVP. This affects the converter response when DC3 is enabled or when its output voltage is increased. When the overvoltage protection is enabled, there is less overshoot in the output voltage, but some oscillation may occur as the voltage settles. This function should only be enabled if steep load transients are present on the output of DC-DC3 and if the voltage overshoot is critical.

15.11 MONITORING AND FAULT REPORTING

Each of the DC-DC Converters (1 to 4) and LDOs (1 to 5 and 7) is monitored for voltage accuracy and fault conditions. An undervoltage condition is detected if the voltage falls below the required level by more than a pre-determined tolerance. If an undervoltage condition occurs, then this is indicated using the corresponding status bit(s) defined in Section 15.12.6. An undervoltage condition also triggers an Undervoltage Interrupt (see Section 15.13). Additional actions to shut down the converter or perform a Device Reset may also be selected.

The Internal LDO (LDO13) is also monitored for voltage accuracy and fault conditions. An undervoltage condition in LDO13 is indicated using the INTLDO_UV_STS bit. This undervoltage condition also causes an OFF transition to be scheduled, as described in Section 11.3.

DC-DC Converters 1 and 2 are monitored for overvoltage conditions. An overvoltage condition is set if the voltage is more than 100mV above the required level. If an overvoltage condition occurs, then this is indicated using the corresponding status bit(s). Note that there is no Interrupt or other selectable response to an overvoltage condition.

The current draw on DC-DC Converters 1 and 2 can be monitored against user-programmable thresholds in order to detect a high current condition. This feature is enabled using DC*m*_HC_IND_ENA and the current threshold is set using DC*m*_HC_THR. Note that the high current threshold is not the same as the maximum current capability of the DC-DC Converters, but is set according to the application requirements. If a high current condition occurs, then this is indicated using the corresponding status bit(s). A high current condition also triggers a High Current Interrupt (see Section 15.13).

15.12 POWER MANAGEMENT REGISTER DEFINITIONS

15.12.1 DC-DC CONVERTER AND LDO REGULATOR ENABLE

The Enable and Status register bits for the DC-DC Converters and LDO Regulators are defined in Table 34.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16464 (4050h) DCDC Enable	3:0	DC*m*_ENA	0	DC-DC*m* Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC*m*_STS)
R16465 (4051h) LDO Enable	10:0	LDO*n*_ENA	0	LDO*n* Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO*n*_STS)
R16466 (4052h) DCDC Status	3:0	DC*m*_STS	0	DC-DC*m* Status 0 = Disabled 1 = Enabled
R16467 (4053h) LDO Status	10:0	LDO*n*_STS	0	LDO*n* Status 0 = Disabled 1 = Enabled

Notes:

1. *n* is a number (1-5, 7, 11) that identifies the individual LDO Regulator.
2. *m* is a number between 1 and 4 that identifies the individual DC-DC Converter.

Table 34 DC-DC Converter and LDO Regulator Control

The Enable and Status register bits for the External Power Enable (EPE) Controls are defined in Table 35.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16464 (4050h) DCDC Enable	7	EPE2_ENA	0	EPE2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE2_STS)
	6	EPE1_ENA	0	EPE1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE1_STS)
R16466 (4052h) DCDC Status	7	EPE2_STS	0	EPE2 Status 0 = Disabled 1 = Enabled
	6	EPE1_STS	0	EPE1 Status 0 = Disabled 1 = Enabled

Table 35 External Power Enable (EPE) Control

15.12.2 DC-DC SYNCHRONOUS BUCK CONVERTER CONTROL

The register controls for configuring the DC-DC synchronous buck converters 1-3 are defined in Table 36.

Note that the DC*m*_ON_SLOT fields and the 5 MSBs of DC*m*_ON_VSEL may also be stored in the integrated OTP memory. See Section 14 for details.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16470 (4056h) DC1 Control 1	15:14	DC1_RATE [1:0]	10	DC-DC1 Voltage Ramp rate 00 = 1 step every 32us 01 = 1 step every 16us 10 = 1 step every 8us 11 = Immediate voltage change
	12	DC1_PHASE	0	DC-DC1 Clock Phase Control 0 = Normal 1 = Inverted
	9:8	DC1_FREQ [1:0]	00	DC-DC1 Switching Frequency 00 = Reserved 01 = 2.0MHz 10 = Reserved 11 = 4.0MHz
	7	DC1_FLT	0	DC-DC1 Output float 0 = DC-DC1 output discharged when disabled 1 = DC-DC1 output floating when disabled
	5:4	DC1_SOFT_START [1:0]	00	DC-DC1 Soft-Start Control (Duration in each of the 8 startup current limiting steps.) 00 = 32us steps 01 = 64us steps 10 = 128us steps 11 = 256us steps

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	DC1_CAP	00	DC-DC1 Output Capacitor 00 = 4.7uF to 20uF 01 = Reserved 10 = 22uF to 47uF 11 = Reserved
R16471 (4057h) DC1 Control 2	15:14	DC1_ERR_ACT [1:0]	00	DC-DC1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.
	12:11	DC1_HWC_SRC [1:0]	00	DC-DC1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	10	DC1_HWC_VSEL	0	DC-DC1 Hardware Control Voltage select 0 = Set by DC1_ON_VSEL 1 = Set by DC1_SLP_VSEL
	9:8	DC1_HWC_MODE [1:0]	11	DC-DC1 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode
	6:4	DC1_HC_THR [2:0]	000	DC-DC1 High Current threshold 000 = 125mA 001 = 250mA 010 = 375mA 011 = 500mA 100 = 625mA 101 = 750mA 110 = 875mA 111 = 1000mA
	0	DC1_HC_IND_ENA	0	DC-DC1 High Current detect enable 0 = Disabled 1 = Enabled
R16472 (4058h) DC1 ON Config	15:13	DC1_ON_SLOT [2:0]	000	DC-DC1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	9:8	DC1_ON_MODE [1:0]	00	DC-DC1 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode
	6:2	DC1_ON_VSEL [6:2]	00000	DC-DC1 ON Voltage select DC1_ON_VSEL[6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. DC1_ON_VSEL[6:2] also exist in ICE/OTP memory, controlling the voltage in 50mV steps. DC1_ON_VSEL[6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).
	1:0	DC1_ON_VSEL [1:0]	00	
R16473 (4059h) DC1 SLEEP Control	15:13	DC1_SLP_SLOT [2:0]	000	DC-DC1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.
	9:8	DC1_SLP_MODE [1:0]	00	DC-DC1 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:0	DC1_SLP_VSEL [6:0]	000_0000	DC-DC1 SLEEP Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).
R16474 (405Ah) DC1 DVS Control	12:11	DC1_DVS_SRC [1:0]	00	DC-DC1 DVS Control Source 00 = Disabled 01 = Enabled 10 = Controlled by Hardware DVS1 11 = Controlled by Hardware DVS2
	6:0	DC1_DVS_VSEL [6:0]	000_0000	DC-DC1 DVS Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).
R16475 (405Bh) DC2 Control 1	15:14	DC2_RATE [1:0]	10	*Same as DC-DC1*
	12	DC2_PHASE	0	*Same as DC-DC1*
	9:8	DC2_FREQ [1:0]	00	*Same as DC-DC1*
	7	DC2_FLT	0	*Same as DC-DC1*
	5:4	DC2_SOFT_START [1:0]	00	*Same as DC-DC1*
	1:0	DC2_CAP	00	*Same as DC-DC1*
R16476 (405Ch) DC2 Control 2	15:14	DC2_ERR_ACT [1:0]	00	*Same as DC-DC1*
	12:11	DC2_HWC_SRC [1:0]	00	*Same as DC-DC1*
	10	DC2_HWC_VSEL	0	*Same as DC-DC1*
	9:8	DC2_HWC_MODE [1:0]	11	*Same as DC-DC1*
	6:4	DC2_HC_THR [2:0]	000	*Same as DC-DC1*
	0	DC2_HC_IND_ENA	0	*Same as DC-DC1*
R16477 (405Dh) DC2 ON Config	15:13	DC2_ON_SLOT [2:0]	000	*Same as DC-DC1*
	9:8	DC2_ON_MODE [1:0]	00	*Same as DC-DC1*

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:2	DC2_ON_VSEL [6:2]	00000	*Same as DC-DC1*
	1:0	DC2_ON_VSEL [1:0]	00	
R16478 (405Eh) DC2 SLEEP Control	15:13	DC2_SLP_SLOT [2:0]	000	*Same as DC-DC1*
	9:8	DC2_SLP_MODE [1:0]	00	*Same as DC-DC1*
	6:0	DC2_SLP_VSEL [6:0]	000_0000	*Same as DC-DC1*
R16479 (405Fh) DC2 DVS Control	12:11	DC2_DVS_SRC [1:0]	00	*Same as DC-DC1*
	6:0	DC2_DVS_VSEL [6:0]	000_0000	*Same as DC-DC1*
R16480 (4060h) DC3 Control 1	12	DC3_PHASE	0	*Same as DC-DC1*
	7	DC3_FLT	0	*Same as DC-DC1*
	5:4	DC3_SOFT_START [1:0]	01	DC-DC3 Soft-Start Control (Duration in each of the 3 intermediate startup current limiting steps.) 00 = Immediate start-up 01 = 512us steps 10 = 4.096ms steps 11 = 32.768ms steps
	3:2	DC3_STNBY_LIM [1:0]	01	DC-DC3 Current Limit Sets the maximum DC output current in Hysteretic Mode. Typical values shown below. 00 = 100mA 01 = 200mA 10 = 400mA 11 = 800mA *Protected by user key*
	1:0	DC3_CAP	00	DC-DC3 Output Capacitor 00 = 10uF to 20uF 01 = 10uF to 20uF 10 = 22uF to 45uF 11 = 47uF to 100uF
R16481 (4061h) DC3 Control 2	15:14	DC3_ERR_ACT [1:0]	00	*Same as DC-DC1*
	12:11	DC3_HWC_SRC [1:0]	00	*Same as DC-DC1*
	10	DC3_HWC_VSEL	0	*Same as DC-DC1*
	9:8	DC3_HWC_MODE [1:0]	11	*Same as DC-DC1*
	7	DC3_OVP	0	DC-DC3 Overvoltage Protection 0 = Disabled 1 = Enabled
R16482 (4062h) DC3 ON Config	15:13	DC3_ON_SLOT [2:0]	000	*Same as DC-DC1*
	9:8	DC3_ON_MODE [1:0]	00	*Same as DC-DC1*
	6:2	DC3_ON_VSEL [6:2]	00000	DC-DC3 ON Voltage select

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1:0	DC3_ON_VSEL [1:0]	00	DC3_ON_VSEL[6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. DC3_ON_VSEL[6:2] also exist in ICE/OTP memory, controlling the voltage in 100mV steps. DC3_ON_VSEL[6:0] is coded as follows: 00h = 0.85V 01h = 0.875V … 65h = 3.375V 66h to 7Fh = 3.4V
R16483 (4063h) DC3 SLEEP Control	15:13	DC3_SLP_SLOT [2:0]	000	*Same as DC-DC1*
	9:8	DC3_SLP_MODE [1:0]	00	*Same as DC-DC1*
	6:0	DC3_SLP_VSEL [6:0]	000_0000	DC-DC3 SLEEP Voltage select 0.85V to 3.4V in 25mV steps 00h = 0.85V 01h = 0.875V … 65h = 3.375V 66h to 7Fh = 3.4V

Table 36 DC-DC (Buck) Converter Control

15.12.3 DC-DC BOOST CONVERTER CONTROL

The register controls for configuring the DC-DC4 boost converter are defined in Table 37.

Note that the DC4_RANGE control register is locked by the WM8311 User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16484 (4064h) DC4 Control	15:14	DC4_ERR_ACT [1:0]	00	DC-DC4 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.
	12:11	DC4_HWC_SRC[1:0]	00	DC-DC4 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	8	DC4_HWC_MODE	1	DC-DC4 Hardware Control Operating Mode 0 = DC-DC4 is controlled by DC4_ENA 1 = DC-DC4 is disabled when Hardware Control Source is asserted

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:2	DC4_RANGE[1:0]	01	Selects the voltage range for DC-DC4 00 = 20V < VOUT <= 30V 01 = 10V < VOUT <= 20V 10 = 6.5V < VOUT <= 10V 11 = Reserved *Protected by user key*
	0	DC4_FBSRC	0	DC-DC4 Voltage Feedback source 0 = ISINK1 1 = ISINK2
R16485 (4065h) DC4 SLEEP Control	8	DC4_SLPENA	0	DC-DC4 SLEEP Enable 0 = Disabled 1 = Controlled by DC4_ENA

Table 37 DC-DC (Boost) Converter Control

15.12.4 LDO REGULATOR CONTROL

The register controls for configuring the LDO Regulators 1-5 are defined in Table 38.

Note that the LDO*n*_ON_SLOT and LDO*n*_ON_VSEL fields may also be stored in the integrated OTP memory. See Section 14 for details.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16488 (4068h) LDO1 Control	15:14	LDO1_ERR_ACT [1:0]	00	LDO1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.
	12:11	LDO1_HWC_SRC [1:0]	00	LDO1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	10	LDO1_HWC_VSEL	0	LDO1 Hardware Control Voltage select 0 = Set by LDO1_ON_VSEL 1 = Set by LDO1_SLP_VSEL
	9:8	LDO1_HWC_MODE	10	LDO1 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO1_ON_MODE
	7	LDO1_FLT	0	LDO1 Output float 0 = LDO1 output discharged when disabled 1 = LDO1 output floating when disabled
	6	LDO1_SWI	0	LDO1 Switch Mode 0 = LDO mode 1 = Switch mode
	0	LDO1_LP_MODE	0	LDO1 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16489 (4069h) LDO1 ON Control	15:13	LDO1_ON_SLOT [2:0]	000	LDO1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	8	LDO1_ON_MODE	0	LDO1 ON Operating Mode 0 = Normal mode 1 = Low Power mode
	4:0	LDO1_ON_VSEL [4:0]	00000	LDO1 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V
R16490 (406Ah) LDO1 SLEEP Control	15:13	LDO1_SLP_SLOT [2:0]	000	LDO1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.
	8	LDO1_SLP_MODE	0	LDO1 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode
	4:0	LDO1_SLP_VSEL [4:0]	00000	LDO1 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V
R16491 (406Bh)	15:14	LDO2_ERR_ACT [1:0]	00	*Same as LDO1*

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
LDO2 Control	12:11	LDO2_HWC_SRC [1:0]	00	*Same as LDO1*
	10	LDO2_HWC_VSEL	0	*Same as LDO1*
	9:8	LDO2_HWC_MODE	10	*Same as LDO1*
	7	LDO2_FLT	0	*Same as LDO1*
	6	LDO2_SWI	0	*Same as LDO1*
	0	LDO2_LP_MODE	0	*Same as LDO1*
R16492 (406Ch) LDO2 ON Control	15:13	LDO2_ON_SLOT [2:0]	000	*Same as LDO1*
	8	LDO2_ON_MODE	0	*Same as LDO1*
	4:0	LDO2_ON_VSEL [4:0]	00000	*Same as LDO1*
R16493 (406Dh) LDO2 SLEEP Control	15:13	LDO2_SLP_SLOT [2:0]	000	*Same as LDO1*
	8	LDO2_SLP_MODE	0	*Same as LDO1*
	4:0	LDO2_SLP_VSEL [4:0]	00000	*Same as LDO1*
R16494 (406Eh) LDO3 Control	15:14	LDO3_ERR_ACT [1:0]	00	*Same as LDO1*
	12:11	LDO3_HWC_SRC [1:0]	00	*Same as LDO1*
	10	LDO3_HWC_VSEL	0	*Same as LDO1*
	9:8	LDO3_HWC_MODE	10	*Same as LDO1*
	7	LDO3_FLT	0	*Same as LDO1*
	6	LDO3_SWI	0	*Same as LDO1*
	0	LDO3_LP_MODE	0	*Same as LDO1*
R16495 (406Fh) LDO3 ON Control	15:13	LDO3_ON_SLOT [2:0]	000	*Same as LDO1*
	8	LDO3_ON_MODE	0	*Same as LDO1*
	4:0	LDO3_ON_VSEL [4:0]	00000	*Same as LDO1*
R16496 (4070h) LDO3 SLEEP Control	15:13	LDO3_SLP_SLOT [2:0]	000	*Same as LDO1*
	8	LDO3_SLP_MODE	0	*Same as LDO1*
	4:0	LDO3_SLP_VSEL [4:0]	00000	*Same as LDO1*
R16497 (4071h) LDO4 Control	15:14	LDO4_ERR_ACT [1:0]	00	*Same as LDO1*
	12:11	LDO4_HWC_SRC [1:0]	00	*Same as LDO1*
	10	LDO4_HWC_VSEL	0	*Same as LDO1*
	9:8	LDO4_HWC_MODE	10	*Same as LDO1*
	7	LDO4_FLT	0	*Same as LDO1*
	6	LDO4_SWI	0	*Same as LDO1*

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	LDO4_LP_MODE	0	*Same as LDO1*
R16498 (4072h) LDO4 ON Control	15:13	LDO4_ON_SLOT [2:0]	000	*Same as LDO1*
	8	LDO4_ON_MODE	0	*Same as LDO1*
	4:0	LDO4_ON_VSEL [4:0]	00000	*Same as LDO1*
R16499 (4073h) LDO4 SLEEP Control	15:13	LDO4_SLP_SLOT [2:0]	000	*Same as LDO1*
	8	LDO4_SLP_MODE	0	*Same as LDO1*
	4:0	LDO4_SLP_VSEL [4:0]	00000	*Same as LDO1*
R16500 (4074h) LDO5 Control	15:14	LDO5_ERR_ACT [1:0]	00	*Same as LDO1*
	12:11	LDO5_HWC_SRC [1:0]	00	*Same as LDO1*
	10	LDO5_HWC_VSEL	0	*Same as LDO1*
	9:8	LDO5_HWC_MODE	10	*Same as LDO1*
	7	LDO5_FLT	0	*Same as LDO1*
	6	LDO5_SWI	0	*Same as LDO1*
	0	LDO5_LP_MODE	0	*Same as LDO1*
R16501 (4075h) LDO5 ON Control	15:13	LDO5_ON_SLOT [2:0]	000	*Same as LDO1*
	8	LDO5_ON_MODE	0	*Same as LDO1*
	4:0	LDO5_ON_VSEL [4:0]	00000	*Same as LDO1*
R16502 (4076h) LDO5 SLEEP Control	15:13	LDO5_SLP_SLOT [2:0]	000	*Same as LDO1*
	8	LDO5_SLP_MODE	0	*Same as LDO1*
	4:0	LDO5_SLP_VSEL [4:0]	00000	*Same as LDO1*

Table 38 LDO Regulators 1-5 Control

The register controls for configuring the LDO Regulator 7 are defined in Table 39.

Note that the LDO7_ON_SLOT and LDO7_ON_VSEL fields may also be stored in the integrated OTP memory. See Section 14 for details.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16506 (407Ah) LDO7 Control	15:14	LDO7_ERR_ACT [1:0]	00	LDO7 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.
	12:11	LDO7_HWC_SRC [1:0]	00	LDO7 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10	LDO7_HWC_VSEL	0	LDO7 Hardware Control Voltage select 0 = Set by LDO7_ON_VSEL 1 = Set by LDO7_SLP_VSEL
	9:8	LDO7_HWC_MODE	00	LDO7 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO7_ON_MODE
	7	LDO7_FLT	0	LDO7 Output float 0 = LDO7 output discharged when disabled 1 = LDO7 output floating when disabled
	6	LDO7_SWI	0	LDO7 Switch Mode 0 = LDO mode 1 = Switch mode
R16507 (407Bh) LDO7 ON Control	15:13	LDO7_ON_SLOT [2:0]	000	LDO7 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	8	LDO7_ON_MODE	0	LDO7 ON Operating Mode 0 = Normal mode 1 = Low Power mode
	4:0	LDO7_ON_VSEL [4:0]	00000	LDO7 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V … 0Ch = 1.60V 0Dh = 1.70V … 1Eh = 3.40V 1Fh = 3.50V

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16508 (407Ch) LDO7 SLEEP Control	15:13	LDO7_SLP_ SLOT [2:0]	000	LDO7 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO7 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.
	8	LDO7_SLP_ MODE	0	LDO7 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode
	4:0	LDO7_SLP_ VSEL [4:0]	00000	LDO7 SLEEP Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V … 0Ch = 1.60V 0Dh = 1.70V … 1Eh = 3.40V 1Fh = 3.50V

Table 39 LDO Regulator 7 Control

The register controls for configuring the LDO Regulator 11 are defined in Table 40.

Note that the LDO11_ON_SLOT and LDO11_ON_VSEL fields may also be stored in the integrated OTP memory. See Section 14 for details.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16519 (4087h) LDO11 ON Control	15:13	LDO11_ON_ SLOT [2:0]	000	LDO11 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	12	LDO11_FRC ENA	0	LDO11 Force Enable (forces LDO11 to be enabled at all times in the OFF, ON and SLEEP states) 0 = Disabled 1 = Enabled
	7	LDO11_VSE L_SRC	0	LDO11 Voltage Select source 0 = Normal (LDO11 settings) 1 = Same as DC-DC Converter 1

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:0	LDO11_ON_ VSEL [3:0]		LDO11 ON Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V … Eh = 1.50V Fh = 1.55V
R16520 (4088h) LDO11 SLEEP Control	15:13	LDO11_SLP _SLOT [2:0]	000	LDO11 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO11 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.
	3:0	LDO11_SLP _VSEL [3:0]		LDO11 SLEEP Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V … Eh = 1.50V Fh = 1.55V

Table 40 LDO Regulator 11 Control

15.12.5 EXTERNAL POWER ENABLE (EPE) CONTROL

The register controls for configuring the External Power Enable (EPE) outputs are defined in Table 41.

Note that the EPE1_ON_SLOT and EPE2_ON_SLOT fields may also be stored in the integrated OTP memory. See Section 14 for details.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16486 (4066h) EPE1 Control	15:13	EPE1_ON_SLOT [2:0]	000	EPE1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2
	12:11	EPE1_HWC_SRC [1:0]	00	EPE1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2
	8	EPE1_HWCENA	0	EPE1 Hardware Control Enable 0 = EPE1 is controlled by EPE1_ENA (Hardware Control input(s) are ignored) 1 = EPE1 is controlled by HWC inputs (Hardware Control input(s) force EPE1 to be de-asserted)
	7:5	EPE1_SLP_SLOT [2:0]	000	EPE1 SLEEP Slot select 000 = No action 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = No action 111 = No action
R16487 (4067h) EPE2 Control	15:13	EPE2_ON_SLOT [2:0]	000	*Same as EPE1*
	12:11	EPE2_HWC_SRC [1:0]	00	*Same as EPE1*
	8	EPE2_HWCENA	0	*Same as EPE1*
	7:5	EPE2_SLP_SLOT [2:0]	000	*Same as EPE1*

Table 41 External Power Enable (EPE) Control

15.12.6 MONITORING AND FAULT REPORTING

The overvoltage, undervoltage and high current status registers are defined in Table 42.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16468 (4054h) DCDC UV Status	13	DC2_OV_STS	0	DC-DC2 Overvoltage Status 0 = Normal 1 = Overvoltage
	12	DC1_OV_STS	0	DC-DC1 Overvoltage Status 0 = Normal 1 = Overvoltage
	9	DC2_HC_STS	0	DC-DC2 High Current Status 0 = Normal 1 = High Current
	8	DC1_HC_STS	0	DC-DC1 High Current Status 0 = Normal 1 = High Current
	3:0	DC*m*_UV_STS	0	DC-DC*m* Undervoltage Status 0 = Normal 1 = Undervoltage
R16469 (4055h) LDO UV Status	15	INTLDO_UV_STS	0	LDO13 (Internal LDO) Undervoltage Status 0 = Normal 1 = Undervoltage
	9:0	LDO*n*_UV_STS	0	LDO*n* Undervoltage Status 0 = Normal 1 = Undervoltage
Note: *n* is a number (1-5, 7) that identifies the individual LDO Regulator. **Note:** *m* is a number between 1 and 4 that identifies the individual DC-DC Converter.				

Table 42 DC Converter and LDO Regulator Status

15.13 POWER MANAGEMENT INTERRUPTS

Undervoltage monitoring is provided on all DC-DC Converters and LDO Regulators, as described in Section 15.11. The associated interrupt flags indicate an undervoltage condition in each individual DC-DC Converter or LDO Regulator. Each of these secondary interrupts triggers a primary Undervoltage Interrupt, UV_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 43.

Current monitoring is provided on DC-DC1 and DC-DC2, as described in Section 15.11. The interrupt flags HC_DC1_EINT and HC_DC2_EINT indicate a high current condition in DC-DC1 and DC-DC2 respectively. Each of these secondary interrupts triggers a primary High Current Interrupt, HC_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 43.

The high current thresholds are programmable; these are set by DC1_HC_THR and DC2_HC_THR for DC-DC1 and DC-DC2 respectively. See Section 15.12.2 for details of these register fields. Note that these functions are for current monitoring; they do not equate to the DC-DC Converter maximum current limit.

ADDRESS	BIT	LABEL	DESCRIPTION
R16403 (4013h) Interrupt Status 3	9:0	UV_LDO*n*_EINT	LDO*n* Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16404 (4014h) Interrupt Status 4	9	HC_DC2_EINT	DC-DC2 High current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	8	HC_DC1_EINT	DC-DC1 High current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	3:0	UV_DC*m*_EINT	DC-DC*m* Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16411 (401Bh) Interrupt Status 3 Mask	9:0	IM_UV_LDO*n*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
R16412 (401Ch) Interrupt Status 4 Mask	9	IM_HC_DC2_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	8	IM_HC_DC1_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	3:0	IM_UV_DC*m*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Notes:

1. *n* is a number (1-5, 7) that identifies the individual LDO Regulator.
2. *m* is a number between 1 and 4 that identifies the individual DC-DC Converter.

Table 43 Power Management Interrupts

15.14 POWER GOOD INDICATION

The WM8311 can indicate the status of the DC-DC Converters and LDO Regulators via a GPIO pin configured as a “PWR_GOOD” output (see Section 21).

Each DC-DC Converter and LDO Regulator to be monitored in this way must be individually enabled as an input to the PWR_GOOD function using the register bits defined in Table 44.

When a GPIO pin is configured as a “PWR_GOOD” output, this signal is asserted when all selected DC-DC Converters and LDO Regulators are operating correctly. If any of the enabled DC-DC Converters or LDO Regulators is undervoltage, then the PWR_GOOD will be de-asserted. In this event, the host processor should read the Undervoltage Interrupt fields to determine which DC-DC Converter or LDO Regulator is affected.

Note that an Undervoltage condition may lead to a Converter being switched off automatically. In this case, the disabled Converter will not indicate the fault condition via PWR_GOOD. Accordingly, the PWR_GOOD signal may not be a reliable output in cases where the WM8311 is configured to shut down any Converters automatically under Undervoltage conditions. It is recommended that the host processor should read the Undervoltage Interrupts in response to PWR_GOOD being de-asserted. The host processor can then initiate the most appropriate response.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16526 (408Eh) Power Good Source 1	3	DC4_OK	0	DC-DC4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	2	DC3_OK	1	DC-DC3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	1	DC2_OK	1	DC-DC2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	0	DC1_OK	1	DC-DC1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
R16527 (408Fh) Power Good Source 2	6	LDO7_OK	1	LDO7 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	4	LDO5_OK	1	LDO5 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	3	LDO4_OK	1	LDO4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	2	LDO3_OK	1	LDO3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	1	LDO2_OK	1	LDO2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled
	0	LDO1_OK	1	LDO1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled

Table 44 PWR_GOOD (GPIO) Configuration

15.15 DC-DC CONVERTER OPERATION

15.15.1 OVERVIEW

The WM8311 provides four DC-DC switching converters. Three of these are synchronous buck (step-down) converters; the fourth of these is a boost (step-up) converter. The principal characteristics of each DC-DC converter are shown below.

	DC-DC1 / DC-DC2	DC-DC3	DC-DC4
Converter Type	Buck (step-down)	Buck (step-down)	Boost (step-up)
Input Voltage Range	2.7V to 5.5V (connect to SYSVDD supply)		
Output Voltage Range	0.6V to 1.8V	0.85V to 3.4V	5V to 30V
Load Current Rating	Up to 1200mA	Up to 1000mA	Up to 25mA @ 30V Up to 40mA @ 20V Up to 90mA @ 8V
Switching Frequency	2MHz or 4MHz	2MHz	1MHz

Table 45 DC-DC Converter Overview

15.15.2 DC-DC SYNCHRONOUS BUCK CONVERTERS

DC-DC Converters 1, 2 and 3 are synchronous buck converters which deliver high performance and high efficiency across a wide variety of operating conditions.

The high switching frequency, together with the current mode architecture, delivers exceptional transient performance suitable for supplying processor power domains and similar applications requiring high stability through fast-changing load (or line) conditions.

The current mode architecture enables extended bandwidth of the control loop, allowing the DC-DC converter to adapt for changes in input or output conditions more rapidly than can be achieved using other feedback mechanisms. This improves the converter's performance under transient load conditions.

The flexible design of the DC-DC Converters allows a selection of different operating configurations, which can be chosen according to the performance, efficiency, space or external component cost requirements.

The DC-DC Converter design achieves high performance with a small inductor component. This is highly advantageous in size-critical designs for portable applications. In the case of DC-DC1 and DC-DC2, the switching frequency is selectable (2MHz or 4MHz). The higher frequency supports best transient performance and the smallest external inductor, whilst the lower rate supports best power efficiency. It should be noted that the supported output voltage range is restricted in the 4MHz mode; for output voltages greater than 1.4V, the 2MHz mode must be used.

The DC-DC Converters are compatible with a range of external output capacitors. A larger capacitor (eg. 47μF) will deliver best transient performance, whilst a smaller capacitor (eg. 4.7μF) may be preferred for size or cost reasons.

Four different operating modes can be selected, allowing the user to configure the converter performance and efficiency according to different demands. This includes power-saving modes for light load conditions and a high performance mode for best transient load performance. A low power LDO Regulator mode is also provided. The DC-DC Converters maintain output voltage regulation when switching between operating modes.

Forced Continuous Conduction Mode (FCCM)

This mode delivers the best load transient performance across the entire operating load range of the converter. It also provides the best EMI characteristics due to the fixed, regular switching pattern.

For normal DC-DC buck converter operation, there is an inductor charging phase followed by a discharging phase. Under light load conditions, the inductor current may be positive or negative during this cycle. (Note that the load current corresponds to the average inductor current.) The negative portion of the cycle corresponds to inefficient operation, as the output capacitor is discharged unnecessarily by the converter circuit. Accordingly, this mode is not optimally efficient for light load conditions.

This mode offers excellent performance under transient load conditions. It exceeds the performance of the other operating modes in the event of a decreasing current demand or a decreasing voltage selection. This is because FCCM mode can actively pull down the output voltage to the required level, whilst other modes rely on the load to pull the converter voltage down under these conditions.

Another important benefit of this mode is that the switching pattern is fixed, regardless of load conditions. This provides best compatibility with noise-sensitive circuits where the noise frequency spectrum must be well-defined.

Although this mode is not optimally efficient for light loads, it delivers the best possible transient load performance and fixed frequency switching. This mode should be selected when best performance is required, delivering minimum output voltage ripple across all static or transient load conditions.

Auto Mode: Continuous / Discontinuous Conduction with Pulse-Skipping (CCM/DCM with PS)

This is an automatic mode that selects different control modes according to the load conditions. The converter supports the full range of load conditions in this mode, and automatically selects power-saving mechanisms when the load conditions are suitable. Under light load conditions, the efficiency in this mode is superior to the FCCM mode. The transient load performance may be slightly worse than FCCM mode.

The converter operates in Continuous Conduction Mode (CCM) for heavy load conditions, and Discontinuous Conduction Mode (DCM) under lighter loads. Discontinuous conduction is when the inductor current falls to zero during the discharge phase, and the converter disables the synchronous rectifier transistor in order that the inductor current remains at zero until the next charge phase. Negative inductor current is blocked in this mode, eliminating the associated losses, and improving efficiency.

The transient response in this mode varies according to the operating conditions; it differs from FCCM in the case of a decreasing current demand or a decreasing voltage, as the converter uses the load to pull the output voltage down to the required level. A light load will result in a slow response time.

A minimum inductor charge time is applied in DCM mode; this leads to a minimum average inductor current when operating as described above. Under very light load conditions, pulse skipping is used to reduce the average inductor current to the level required by the load. In pulse-skipping mode, the charge phase of selected cycles is not scheduled, and the load is supported by the output capacitor over more than one cycle of the switching frequency. As well as supporting very light load current conditions, this mechanism offers power savings, as the switching losses associated with the skipped pulses are eliminated. A disadvantage of this is that the transient response is degraded even further with respect to DCM. When the pulse-skipping behaviour is invoked, an increased output voltage ripple may be observed under some load conditions.

This mode is suitable for a wide range of operating conditions. It supports the full range of load currents, and offers efficiency savings under light load conditions.

Hysteretic Mode

Hysteretic mode is a power-saving mode. It does not support the full load capability of the DC-DC converter, but offers efficiency improvements over the FCCM and Auto (CCM/DCM with PS) modes.

The control circuit in Hysteretic mode operates very differently to the Pulse-Skipping mode that is available in Auto mode. In Pulse-Skipping mode, selected switching cycles are dropped in order to reduce the output current to match a light load condition, whilst maintaining good output voltage ripple as far as possible. In Hysteretic mode, the converter uses switched operation on an adaptive intermittent basis to deliver the required average current to the load.

In the switched operation portion of the Hysteretic mode, the converter drives the output voltage up; this is followed by a power-saving period in which the control circuit is largely disabled whilst the load pulls the output voltage down again over a period of many switching cycles. The duration of the fixed frequency bursts and the time between bursts is adapted automatically by the output voltage monitoring circuit.

In this mode, the power dissipation is reduced to a very low level by disabling parts of the control circuitry for the duration of selected switching cycles. This improves the overall efficiency, but also leads to output voltage ripple and limited performance. This mode produces a larger output voltage ripple than the Pulse-Skipping mode. In order to limit the degradation of the DC-DC converter performance in Hysteretic mode, the control circuit is designed for a restricted range of load conditions only. Note that the irregular switching pattern also results in degraded EMI behaviour.

Hysteretic mode and Pulse Skipping mode are both Pulse Frequency Modulation (PFM)-type modes, where the switching pulse frequency is adjusted dynamically according to the load requirements. A consequence of this frequency modulation is that the circuit’s EMI characteristics are less predictable. In Hysteretic mode in particular, the EMI effects arising from the DC-DC switching are present across a wider frequency band than is the case in CCM and DCM. It is more difficult to effectively suppress the wide band interference, and this factor may result in Hysteretic mode being unsuitable for some operating conditions.

Hysteretic mode is suitable for light load conditions only, and only suitable for operating modes that are not sensitive to wide band RF/EMI effects. The output voltage ripple (and frequency) is load dependent, and is generally worse than Pulse-Skipping operation in the Auto mode. Provided that the EMI and voltage ripple can be tolerated, the Hysteretic mode offers an efficiency advantage over the Auto (CCM/DCM with PS) mode.

LDO Mode

In this mode, there is no FET switching at all, and the converter operates as a Low Drop-Out (LDO) regulator. In this mode, the FET switching losses are eliminated, as is the power consumption of the DC-DC control circuit. Under suitable operating conditions, this provides the most efficient option for light loads, without any of the EMI or voltage ripple limitations of Hysteretic mode.

As with any LDO, the output voltage is constant, and there is no internal source of voltage ripple. Unlike the switching modes, the power efficiency of the LDO mode is highly dependent on the input and output voltages; the LDO is most efficient when the voltage drop between input and output is small. The power dissipated as heat loss by an LDO increases rapidly as the input - output voltage difference increases.

LDO mode is suitable for light loads, and provides a ripple-free output. The LDO mode features a very low start-up current; this mode can be used to avoid the higher in-rush current that occurs in the switching converter modes. The efficiency is dependent on the input - output voltage configuration; the LDO mode can be highly efficient, but may also be unacceptably inefficient. If an improvement in power efficiency is required, then Hysteretic mode may be the preferred choice or, for better EMI and voltage ripple, the Auto (CCM/DCM with PS) mode may be the optimum selection.

Operating Mode Summary

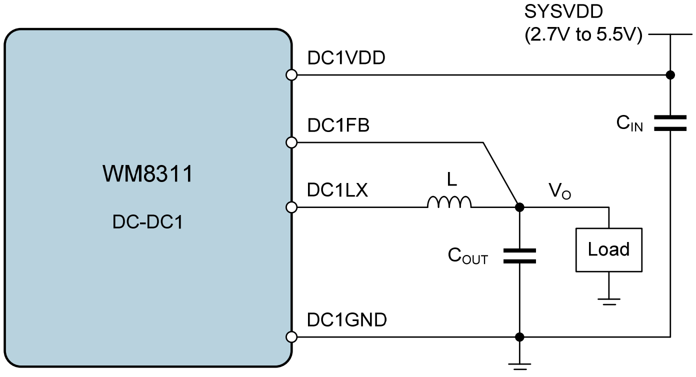
MODE	DESCRIPTION	APPLICATION
Forced Continuous Conduction Mode (FCCM)	Buck converter operation where inductor current is continuous at all times.	High performance for all static and transient load conditions. Fixed frequency switching offers best compatibility with sensitive circuits.
Auto Mode: Continuous / Discontinuous Conduction with Pulse-Skipping Mode (CCM/DCM with PS)	Buck converter operation where inductor current may be discontinuous under reduced loads; pulse-skipping also enabled under lighter loads.	High efficiency for all static and transient load conditions. Performance may be less than FCCM mode for heavy load transients.
Hysteretic Mode	The converter uses a hysteretic control scheme with pulsed switching operation. The control circuitry is disabled intermittently for power saving.	High efficiency for light static and light transient loads only. Maximum load current is restricted; output voltage ripple is increased.
LDO Mode	No FET switching at all; linear regulator operation.	Power saving mode for light loads only. High efficiency for ultra light loads. Low current soft-start control.

Table 46 DC-DC Synchronous Buck Converter Operating Modes Summary

Typical Connections

The typical connections to DC-DC Converter 1 are illustrated in Figure 20. The equivalent circuit applies to DC-DC Converters 2 and 3 also.

The input voltage connection to DC-DC Converters 1, 2 and 3 is provided on DC1VDD, DC2VDD and DC3VDD respectively; these are typically connected to the SYSVDD voltage node. Note that the internal supply pins PVDD1 and PVDD2 must be connected to the same supply voltage as the DC-DC Converters (ie. SYSVDD).



Note: Equivalent circuit applies for DC-DC2 and DC-DC3

Figure 20 DC-DC Synchronous Buck Converter Connections

The recommended output capacitor C_{OUT} varies according to the required transient response. Note that the DC*m*_CAP register field must be set according to the output capacitance on each DC-DC Converter in order to achieve best performance.

In the case of DC-DC1 and DC-DC2, the recommended inductor component varies according to the DC*m*_FREQ register field. This register supports a choice of different switching frequencies.

See Section 30.3 for details of specific recommended external components.

15.15.3 DC-DC STEP UP CONVERTER

DC-DC Converter 4 is a step-up DC-DC Converter designed to deliver high power efficiency across full load conditions. It is designed to provide a voltage which is determined by the selected current of either Current Sink 1 or Current Sink 2 through an external load - typically a string of LEDs.

DC-DC Converter 4 is designed with fixed frequency current mode architecture. The clock frequency is set by an internal RC oscillator, which provides a 1MHz clock.

The typical connections to DC-DC Converter 4 are illustrated in Figure 21. The DC4_FBSRC register field can select either ISINK1 or ISINK2 as input to the feedback circuit.

The input voltage connection, DC4VDD, is typically connected to the SYSVDD voltage node. Note that the internal supply pins PVDD1 and PVDD2 should also be connected to SYSVDD.

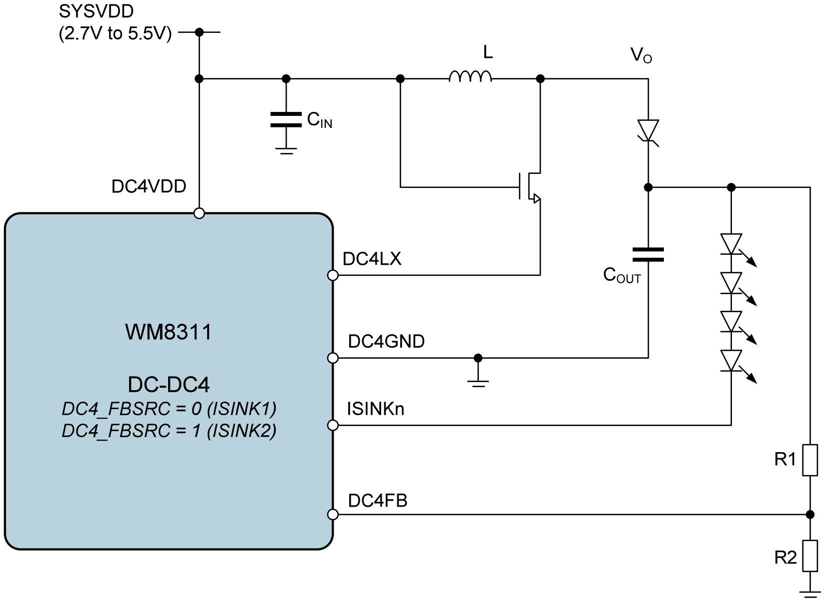


Figure 21 DC-DC Boost Converter Connections

Note that the recommended output capacitor C_{OUT} varies according to the required output voltage. The DC4_RANGE register field must be set according to the required output voltage.

See Section 30.4 for details of specific recommended external components.

15.16 LDO REGULATOR OPERATION

15.16.1 OVERVIEW

The WM8311 provides 7 LDO Regulators. One of these (LDO7) is a low-noise analogue LDO. One of the LDO Regulators (LDO11) can be configured to be enabled even when the WM8311 is in the OFF state. The principal characteristics of the LDO Regulators are shown below.

	LDO1	LDO2, 3	LDO4, 5	LDO7	LDO11
Converter Type	General Purpose	General Purpose	General Purpose	Analogue	General Purpose
Input Voltage Range	1.5V to 5.5V (must be ≤ SYSVDD voltage)			1.71V to 5.5V	1.8V to 5.5V
Output Voltage Range	0.9V to 3.3V	0.9V to 3.3V	0.9V to 3.3V	1.0V to 3.5V	0.8V to 1.55V
Load Current Rating	Up to 300mA	Up to 200mA	Up to 100mA	Up to 200mA	Up to 25mA
Pass device impedance @ 2.5V	1Ω	1Ω	2Ω	1Ω	n/a

Table 47 LDO Regulator Overview

15.16.2 LDO REGULATORS

The LDO Regulators are configurable circuits which generate accurate, low-noise supply voltages for various system components. The LDO Regulators are dynamically programmable and can be re-configured at any time. Two low power modes are provided for the general purpose LDOs 1-5; a single low power mode is provided for the analogue LDO7; this enables the overall device power consumption to be minimised at all times.

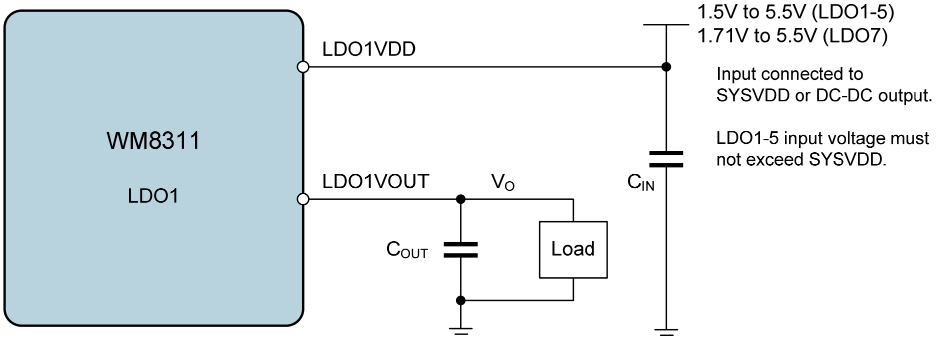
The LDOs (1-5, 7) can also operate as current-limited switches, with no voltage regulation; this is useful for ‘Hot Swap’ outputs, i.e. supply rails for external devices that are plugged in when the system is already powered up - the current-limiting function prevents the in-rush current into the external device from disturbing other system power supplies.

The input voltage to these LDOs is provided on pin LDO*n*VDD for each of LDO1-5, 7 respectively.

The LDO input supply pins are typically connected to the SYSVDD voltage node, or else can be connected to the output pin of one of the DC-DC buck converters. Note that the internal supply pins PVDD1 and PVDD2 should also be connected to SYSVDD.

LDO11 is a configurable LDO intended for 'always-on' functions external to the WM8311. The WM8311 contains a further two non-configurable LDOs which support internal functions only.

The connections to LDO Regulator 1 are illustrated in Figure 22. The equivalent circuit applies to LDO2, LDO3, LDO4, LDO5 and LDO7.



Note: Equivalent circuit applies for LDO2, 3, 4, 5, 7.

Figure 22 LDO Regulator Connections

An input and output capacitor are recommended for each LDO Regulator, as illustrated above.

See Section 30.5 for details of specific recommended external components.

16 CURRENT SINKS

16.1 GENERAL DESCRIPTION

The WM8311 provides two Current Sinks, ISINK1 and ISINK2. These are programmable constant-current sinks designed to drive strings of serially connected LEDs, including white LEDs used in display backlight applications.

The WM8311 Boost Converter, DC-DC4, is designed as a power source for LED strings. Driving LEDs in this way is particularly power efficient because no series resistor is required. The Boost Converter can generate voltages higher than the Battery, Wall or USB supply, producing the necessary combined forward voltages of long LED strings. See Section 15.15.3 for details of DC-DC4 operation.

16.2 CURRENT SINK CONTROL

The configuration of the Current Sinks is described in the following sections.

16.2.1 ENABLING THE SINK CURRENT

In the ON power state, the Current Sinks ISINK1 and ISINK2 can be enabled in software using the CS1_ENA and CS2_ENA register fields as defined in Table 48. When the Current Sinks are enabled, the drive current is controlled by the CS1_DRIVE and CS2_DRIVE bits. Note that the Current Sinks permit current flow only when the applicable CS*n*_ENA and CS*n*_DRIVE bits are both set.

The WM8311 Boost Converter, DC-DC4, is the recommended power source for the Current Sinks. The recommended switch-on sequence is as follows:

- Enable Current Sink and Current Drive (CS*n*_ENA = 1; CS*n*_DRIVE = 1)
- Enable Boost Converter (DC4_ENA = 1)

The status of the Current Sinks in the SLEEP power state are controlled by CS1_SLPENA and CS2_SLPENA, as described in Table 48. The Current Sinks may either be disabled in SLEEP or remain under control of the applicable CS*n*_ENA register bit.

If a Current Sink is disabled in SLEEP, then the applicable CS*n*_DRIVE bit is automatically reset to 0 as part of the SLEEP transition sequence. Note that the CS*n*_DRIVE bit will remain reset at 0 following a WAKE transition; the Current Sink can only be re-enabled by writing to the applicable CS*n*_DRIVE register bit.

If both Current Sinks are disabled in SLEEP, then DC4 can also be disabled in SLEEP, by setting DC4_SLPENA = 0, as described in Section 15.4.2. If DC4 is not disabled, then it is important that CS*n*_ENA also remains set in the SLEEP power state.

The recommended switch-off sequence for DC-DC4 and the Current Sinks is as follows:

- Disable Current Drive (CS*n*_DRIVE = 0)
- Disable Boost Converter (DC4_ENA = 0)
- Disable Current Sink (CS*n*_ENA = 0)

Note that this switch-off sequence is important in order to avoid forward-biasing on-chip ESD protection diodes.

When the Current Sinks output drive is enabled or disabled using CS1_DRIVE or CS2_DRIVE, the current ramps up or down at a programmable rate. The ramp durations are programmed using the register bits defined in Section 16.2.3. If the current ramp is not required when switching off DC-DC4 and the Current Sinks, then the following switch-off sequence may be used:

- Disable Boost Converter (DC4_ENA = 0)
- Disable Current Sink and Current Drive (CS*n*_ENA = 0; CS*n*_DRIVE = 0)

When the Current Sinks are enabled, the status of each is indicated using the CSn_STS bits. If the Current Sinks are unable to sink the demanded current (eg. if the power source is too low or if the load is open circuit), then the respective CSn_STS bit will be set to 1. When the Current Sink circuit is correctly regulated, then the respective CSn_STS bits are set to 0.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16462 (404Eh) Current Sink 1	15	CS1_ENA	0	Current Sink 1 Enable (ISINK1 pin) 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.
	14	CS1_DRIVE	0	Current Sink 1 output drive enable 0 = Disabled 1 = Enabled
	13	CS1_STS	0	Current Sink 1 status 0 = Normal 1 = Sink current cannot be regulated
	12	CS1_SLPENA	0	Current Sink 1 SLEEP Enable 0 = Disabled 1 = Controlled by CS1_ENA
R16463 (404Fh) Current Sink 2	15	CS2_ENA	0	Current Sink 2 Enable (ISINK2 pin) 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.
	14	CS2_DRIVE	0	Current Sink 2 output drive enable 0 = Disabled 1 = Enabled
	13	CS2_STS	0	Current Sink 2 status 0 = Normal 1 = Sink current cannot be regulated
	12	CS2_SLPENA	0	Current Sink 2 SLEEP Enable 0 = Disabled 1 = Controlled by CS2_ENA

Table 48 Enabling ISINK1 and ISINK2

16.2.2 PROGRAMMING THE SINK CURRENT

The sink currents for ISINK1 and ISINK2 can be independently programmed by writing to the CS1_ISEL and CS2_ISEL register bits. The current steps are logarithmic to match the logarithmic light sensitivity characteristic of the human eye. The step size is 1.51dB (i.e. the current doubles every four steps).

Note that the maximum programmable sink current is 27.6mA. The maximum current that can be supported by the DC-DC4 Boost Converter varies with the output voltage; the maximum ISINK current that can be supported by the Boost Converter will depend upon the forward voltage required by the current sink load(s).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16462 (404Eh) Current Sink 1	5:0	CS1_ISEL	00 0000	ISINK1 current. Current = 2.0µA × 2^(CS1_ISEL/4), where CS1_ISEL is an unsigned binary number. Alternatively, CS1_ISEL = 13.29 x LOG(current/2.0µA) 00_0000 = 2.0µA 11_0111 = 27.6mA Values greater than 11_0111 will result in the maximum current of approx 27.6mA.
R16463 (404Fh) Current Sink 2	5:0	CS2_ISEL	00 0000	ISINK2 current. Current = 2.0µA × 2^(CS2_ISEL/4), where CS2_ISEL is an unsigned binary number. Alternatively, CS2_ISEL = 13.29 x LOG(current/2.0µA) 00_0000 = 2.0µA 11_0111 = 27.6mA Values greater than 11_0111 will result in the maximum current of approx 27.6mA.

Table 49 Controlling the Sink Current for ISINK1 and ISINK2

16.2.3 ON/OFF RAMP TIMING

When the Current Sinks output drive is enabled or disabled using CS1_DRIVE or CS2_DRIVE, the current ramps up or down at a programmable rate. This can be used in order to switch the LEDs on or off gradually. The ramp durations are programmed using the register bits defined in Table 50.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16462 (404Eh) Current Sink 1	11:10	CS1_OFF_RAMP	01	ISINK1 Switch-Off ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.
	9:8	CS1_ON_RAMP	01	ISINK1 Switch-On ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16463 (404Fh) Current Sink 2	11:10	CS2_OFF_RAMP	01	ISINK2 Switch-Off ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.
	9:8	CS2_ON_RAMP	01	ISINK2 Switch-On ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.

Table 50 Configuring On/Off Ramp Timing for ISINK1 and ISINK2

16.3 CURRENT SINK INTERRUPTS

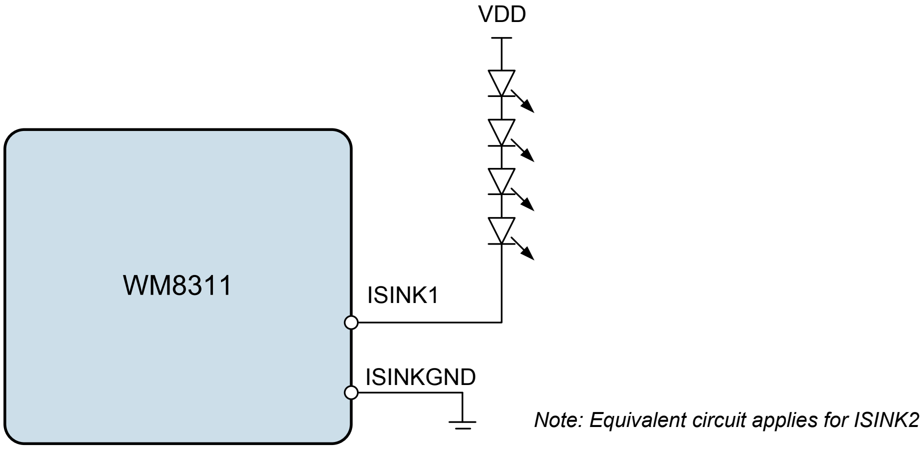
The Current Sinks are associated with two Interrupt event flags, which indicate if the Current Sinks are unable to sink the demanded current (eg. if the power source is too low or if the load is open circuit). Each of these secondary interrupts triggers a primary Current Sink Interrupt, CS_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 51.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	7	CS2_EINT	Current Sink 2 interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	6	CS1_EINT	Current Sink 1 interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16410 (401Ah) Interrupt Status 2 Mask	7	IM_CS2_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	6	IM_CS1_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 51 Current Sink Interrupts

16.4 LED DRIVER CONNECTIONS

The recommended connections for LEDs on ISINK1 and ISINK2 are illustrated in Figure 23.



Note: Equivalent circuit applies for ISINK2

Figure 23 LED Connections to ISINK1 and ISINK2

The ground connection associated with these two Current Sinks is the ISINKGND pin. The DC-DC4 Boost Converter can be used to provide the VDD supply for ISINK1 or ISINK2. It is also possible to drive ISINK1 and ISINK2 simultaneously from the DC-DC4 Boost Converter. See Section 15.4.2 for details of configuring DC-DC4 correctly according to whether it is supplying ISINK1 or ISINK2.

17 POWER SUPPLY CONTROL

17.1 GENERAL DESCRIPTION

The WM8311 can take its power supply from a Wall adaptor, a USB interface or from a single-cell lithium battery. The WM8311 autonomously chooses the most appropriate power source available, and supports hot-swapping between sources (ie. the system can remain in operation while different sources are connected and disconnected).

Comparators within the WM8311 identify which power supplies are available and select the power source in the following order of preference:

- Wall adaptor (WALLVDD)
- USB power rail (USBVDD)
- Battery (BATTVDD)

Note that the Wall supply is normally the first choice of supply, provided that it is within the operating limits quoted in Section 6. The WM8311 can operate with any combination of these power supplies, or with just a single supply.

When WALLVDD or USBVDD is selected as the power source, this may be used to charge the Battery, using the integrated battery charger circuit.

The recommended connections between the WM8311 and the WALL, USB and Battery supplies are illustrated in Figure 24. Note that the external FET components may be omitted in some applications, as described later in this section.

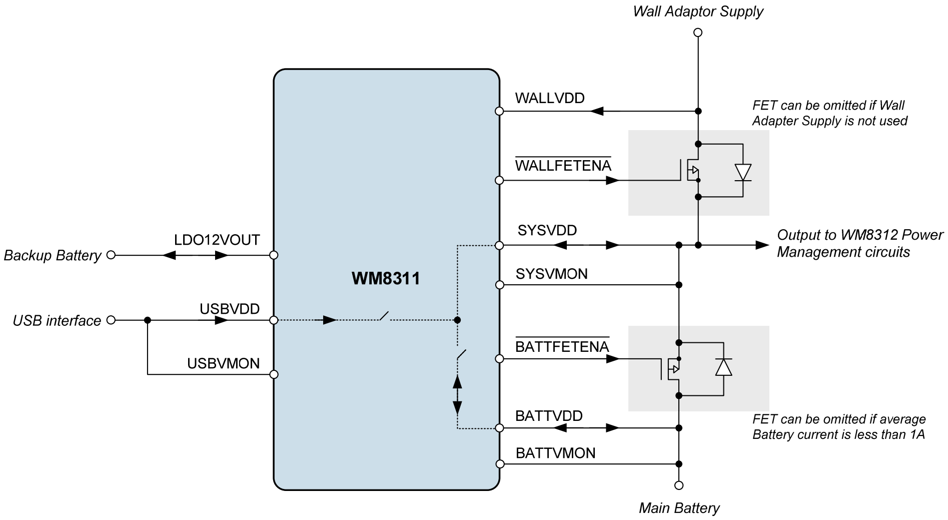


Figure 24 WM8311 Power Supply Connections

SYSVDD is primarily an output from the WM8311; this output is the preferred supply, where the WM8311 has arbitrated between the Wall, Battery and USB connections. This output is suitable for supplying power to the other blocks of the WM8311, including the DC-DC Converters and LDO Regulators. SYSVDD is also an input under some conditions, such as battery charging from the Wall supply. The voltage at the SYSVDD load connection point is sensed using the SYSVMON pin.

All loads connected to the WM8311 should be connected to the SYSVDD pin. The inputs to the DC-DC Converters and LDOs are typically connected to the SYSVDD pin. The inputs to the LDOs may, alternatively, be connected to the outputs of the DC-DCs if desired.

Note that connecting the BATTVDD pin directly to a load is not recommended; this may lead to incorrect behaviour of the battery charger. A filter capacitor between BATTVDD and GND is recommended to ensure best performance of the battery charger; for specific recommendations, refer to the WM8311 evaluation board users manual.

The Wall Adaptor supply connects to SYSVDD via a FET switch as illustrated in Figure 24. The FET switch is necessary in order to provide isolation between the Wall supply and the Battery/USB supplies. The Wall Adapter voltage is sensed directly on the WALLVDD pin; this allows the WM8311 to determine the preferred supply, including when the Wall FET is switched off.

The gate connection to the Wall FET is driven by the $\overline{\text{WALLFETENA}}$ pin. The drive strength of this pin can be selected using the WALL_FET_ENA_DRV_STR register bit as described in Section 17.3.

Note that, when the Wall Adapter is the preferred power supply, the Battery will be used if necessary to supplement the current provided at SYSVDD.

If the Wall Adapter power source is not used, then the associated FET may be omitted, as illustrated in Figure 24.

The main battery connects directly to the BATTVDD pin. The voltage at the battery is sensed using the BATTVMON pin.

It is highly recommended that an external FET is connected between BATTVDD and SYSVDD as illustrated in Figure 24. Under battery-powered operation, this FET controls the current flow from the battery to SYSVDD. By using this external path, the power losses under heavy load conditions are reduced, and power efficiency is increased. When this FET is not present, all the system current flows internally from BATTVDD to SYSVDD, which can lead to unnecessary thermal losses. The external Battery FET should always be used for average loads in excess of 1A.

The gate connection to the Battery FET is driven by the $\overline{\text{BATTFETENA}}$ pin. The functionality of this pin is enabled by setting the BATT_FET_ENA register bit, as described in Section 17.2.

If the average load drawn from the Battery is less than 1A, then the associated FET may be omitted, as illustrated in Figure 24. Note that the external FET is open during battery charging.

The USB interface connects directly to the USBVDD pin. The WM8311 can use this pin as an input to power the device and/or to charge a battery connected to the BATTVDD pin. The voltage at the USB supply is sensed using the USBVMON pin.

Note that, when USB is the preferred power supply, the Battery will be used if necessary to supplement the current drawn from the USBVDD pin.

A backup power source can be supported using a coin cell, super/gold capacitor, or else a standard capacitor, connected to the LDO12VOUT pin. When no other supply is available, the backup source provides power to maintain the RTC memory whilst in the BACKUP power state. At other times, the LDO12VOUT pin provides a constant-voltage output to maintain the backup power source. See Section 17.6 for more details of Backup Power.

The status of the Wall and USB power supplies is indicated in the System Status register, as described in Table 52. When PWR_WALL or PWR_USB is set, this indicates that the corresponding power source is available for powering the WM8311.

If the status of either these power supplies changes, indicating a connection, disconnection, or a voltage that is outside the required limits, the Power Path Source interrupt, PPM_PWR_SRC_EINT, is set (see Section 17.5). Note that this interrupt does not indicate the availability of the battery power source.

The PWR_SRC_BATT bit indicates when the battery is supplying current to the WM8311. This includes when the battery is supplementing the Wall or USB power supply sources.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16397 (400Dh) System Status	10	PWR_SRC_BATT	0	Battery Power Source status 0 = Battery is not supplying current 1 = Battery is supplying current
	9	PWR_WALL	0	Wall Adaptor status 0 = Wall Adaptor voltage not present 1 = Wall Adaptor voltage is present
	8	PWR_USB	0	USB status 0 = USB voltage not present 1 = USB voltage is present

Table 52 Power Source Status Registers

17.2 BATTERY POWERED OPERATION

The WM8311 selects Battery power via BATTVDD when the battery voltage is higher than the WALLVDD and USBVDD supply voltages. In practical usage, this means the Battery is used when the Wall and USB supplies are both disconnected.

The battery will be used to supplement the USB or Wall Adaptor supplies when required.

If the WALLVDD or USBVDD supply becomes available during battery operation, then the selected power source is adjusted accordingly.

When an external FET is provided between BATTVDD and SYSVDD, as described in Section 17.1, the $\overline{\text{BATTFETENA}}$ pin functionality must be enabled by setting BATT_FET_ENA as described in Table 53.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16390 (4006h) Reset Control	12	BATT_FET_ENA	0	Enables the FET gate functionality on the BATTFETENA pin. (Note this pin is Active Low.) 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.

Table 53 Configuring the Battery Power Operation

17.3 WALL ADAPTOR POWERED OPERATION

The WM8311 selects Wall Adaptor power whenever this supply is within the normal operating limits of 4.3V to 5.5V and WALLVDD is higher than BATTVDD. The Wall adaptor power source is also selected below 4.3V if USBVDD is less than 4.3V and WALLVDD is higher than BATTVDD.

Note that USBVDD supply is not used when WALLVDD is within its normal operating limits, even if the USBVDD supply is higher than the WALLVDD supply.

When the WALLVDD supply is selected and a Battery is connected, then battery charging is possible in the ON or SLEEP power states; see Section 17.7.

The drive strength of the Wall FET gate connection, $\overline{\text{WALLFETENA}}$, can be selected using the WALL_FET_ENA_DRV_STR register bit as described in Table 54.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16390 (4006h) Reset Control	13	WALL_FET_ENA_DRV_STR	0	Sets the drive strength of the WALLFETENA pin. (Note this pin is Active Low.) 0 = Weak drive (500kOhm) 1 = Strong drive (50kOhm)

Table 54 Configuring the Wall Adaptor Power Operation

17.4 USB POWERED OPERATION

The WM8311 selects USB power via the USBVDD pin when this supply is within the normal USB operating limits of 4.3V to 5.5V, and WALLVDD is less than 4.3V and USBVDD is the highest supply source available. USB power is also selected below 4.3V if WALLVDD is less than 3.4V and USBVDD is the highest supply available.

The maximum current drawn from the USB supply is determined by the USB_ILIM register field. Currents ranging from 0mA to 1800mA may be selected. See also Section 7 for the limits of the USB Current switch. If the system current demand is greater than the limit set by USB_ILIM, then this is indicated via the USB_CURR_STS bit and by setting the PPM_USB_CURR_EINT interrupt (see Section 17.5).

The USB power source will be supplemented by battery power, when available, in order to maintain the USB current within the applicable limit. If there is no battery connected, or there is insufficient capacity to support the system demands, then the supply rails may drop as the WM8311 attempts to meet the USB current limit.

If a suitable WALLVDD supply becomes available during USB operation, then this will be selected as the preferred power source.

When the USBVDD supply is selected and a Battery is connected, then battery charging is possible in the ON or SLEEP power states, provided that sufficient current capacity is available. See Section 17.7 for details of the Battery Charger.

Note that, when the USBVDD supply is selected by the WM8311, and an 'ON' state transition is requested, the USB current limit must be set to 100mA or higher. If a lower current limit is selected, then the 'ON' state transition event may fail. This requirement is also applicable when a battery is available to provide supplementary power. There is no requirement to set USB_ILIM for start-up when the WALLVDD supply is selected.

The user-configurable OTP memory contains the USB_ILIM register field. This allows users to program their chosen USB current limit on start-up. (Note that the current limit can still be updated during normal operation.) If the WM8311 is powered up with USBVDD as the selected power source, and the applicable USB current limit is 100mA, then the start-up behaviour is determined by the USB100MA_STARTUP field, as defined in Table 55.

When starting up in 100mA USB mode, the normal or soft-start process can be selected. The soft-start option controls the DC-DC converters and LDO Regulators in order to reduce the start-up current demand. In 100mA USB soft-start operation, the DC-DC Converters are initially enabled in LDO mode in order that the in-rush current does not exceed the USB limit. The LDO Regulators are also current-limited during the soft start-up.

Care is required when using the 100mA soft-start; if the LDOs or DC-DCs present an excessive load, then the WM8311 may be unable to power up; it must be ensured that the connected load is compatible with the 100mA current limit. In particular, it is important that the loads on the DC-DC Converters do not exceed the capacity of their LDO operating modes. (See Section 7.1 for the maximum current in LDO mode.)

It is also possible to delay the USB start-up if the battery voltage is less than a selectable threshold; in these cases, the WM8311 enables the battery trickle charge mode (provided that CHG_ENA = 1), and delays the start-up request until the battery voltage threshold has been met. See also Section 27.1 for specific external component requirements relating to the USB100MA_STARTUP register setting.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16387 (4003h) Power State	5:4	USB100MA_STARTUP [1:0	00	Sets the device behaviour when starting up under USB power, when USB_ILIM = 010 (100mA) 00 = Normal 01 = Soft-Start 10 = Only start if BATTVDD > 3.1V 11 = Only start if BATTVDD > 3.4V In the 1X modes, if the battery voltage is less than the selected threshold, then the device will enable trickle

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				charge mode instead of executing the start-up request. The start-up request is delayed until the battery voltage threshold has been met. Note that trickle charge is only possible when CHG_ENA=1.
	3	USB_CURR_STS	0	Indicates if the USB current limit has been reached 0 = Normal 1 = USB current limit
	2:0	USB_ILIM	010	Sets the USB current limit 000 = 0mA (USB switch is open) 001 = 2.5mA 010 = 100mA 011 = 500mA 100 = 900mA 101 = 1500mA 110 = 1800mA 111 = 550mA Note that, when starting up the WM8311 with the USBVDD supply selected, the USB_ILIM register must be set to 100mA or higher.

Table 55 Configuring the USB Power Operation

17.5 POWER PATH MANAGEMENT INTERRUPTS

The Power Path Management circuit is associated with three Interrupt event flags.

The PPM_SYSLO_EINT interrupt bit is set when the internal signal SYSLO is asserted. This indicates a SYSVDD undervoltage condition, described in Section 24.4.

The PPM_PWR_SRC_EINT interrupt bit is set whenever the status of the Wall or USB supplies changes, indicating a connection, disconnection, or a voltage. See Section 17.1.

The PPM_USB_CURR_EINT interrupt bit is set whenever the permitted USB current limit has been reached. See Section 17.4.

Each of these secondary interrupts triggers a primary Power Path Management Interrupt, PPM_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 56.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	15	PPM_SYSLO_EINT	Power Path SYSLO interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	14	PPM_PWR_SRC_EINT	Power Path Source interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	13	PPM_USB_CURR_EINT	Power Path USB Current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	15	IM_PPM_SYSLO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

ADDRESS	BIT	LABEL	DESCRIPTION
	14	IM_PPM_PWR_SRC_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	13	IM_PPM_USB_CURR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 56 Power Path Management Interrupts

17.6 BACKUP POWER

As an option, a backup power source can be provided for the WM8311. This is provided using a coin cell, super/gold capacitor, or else a standard capacitor, connected to the LDO12VOUT pin.

Note that a 22kΩ series resistor should also be connected to the backup power source.

The LDO12VOUT pin provides a constant-voltage output for charging the backup power source whenever the SYSVDD power domain is available.

The purpose of the backup is to power the always-on functions such as the crystal oscillator, RTC and ALARM control registers. The backup power also maintains a ‘software scratch’ memory area in the register map - see Section 12.6. Maintaining these functions at all times provides system continuity even when the main battery is removed and no other power supply is available.

The backup duration will vary depending upon the backup power source characteristics. A typical coin cell can provide power to the WM8310 in BACKUP mode for a month or more whilst also maintainingthe RTC and the ‘software scratch’ register.

If a standard capacitor is used as the backup power source, then it is particularly important to minimise the device power consumption in the BACKUP state. A 22μF capacitor will maintain the device settings for up to 5 minutes in ‘unclocked’ mode, where power consumption is minimised by stopping the RTC in the BACKUP state. The RTC is unclocked in the BACKUP state if the XTAL_BKUPENA register field is set to 0, as described in Section 20.5.

17.7 BATTERY CHARGER

17.7.1 GENERAL DESCRIPTION

The WM8311 incorporates a battery charger which is designed for charging single-cell lithium batteries. The battery charger can operate from either the Wall or USB power sources. The battery charger implements constant-current (CC) and constant-voltage (CV) charge methods, and can run automatically without any intervention required by the host processor.

The battery charger voltage and current are programmable. Trickle charging and fast charging modes are supported. In both modes, the SYSVDD voltage is monitored to ensure the power supply capacity or USB current limit is not exceeded. If the SYSVDD voltage drops to 3.9V, (eg. if the USB current limit has been reached), then the battery charge current is automatically reduced to try and prevent further voltage drop at SYSVDD.

Under high operating load conditions, the battery may be required to supplement the USB or Wall Adaptor power sources. Note that this capability is supported even when battery charging is enabled; in this case, the battery provides power to the system when required, and the charger resumes when sufficient current capacity is available.

Typical connections for the WM8311 battery charger are illustrated in Figure 25.

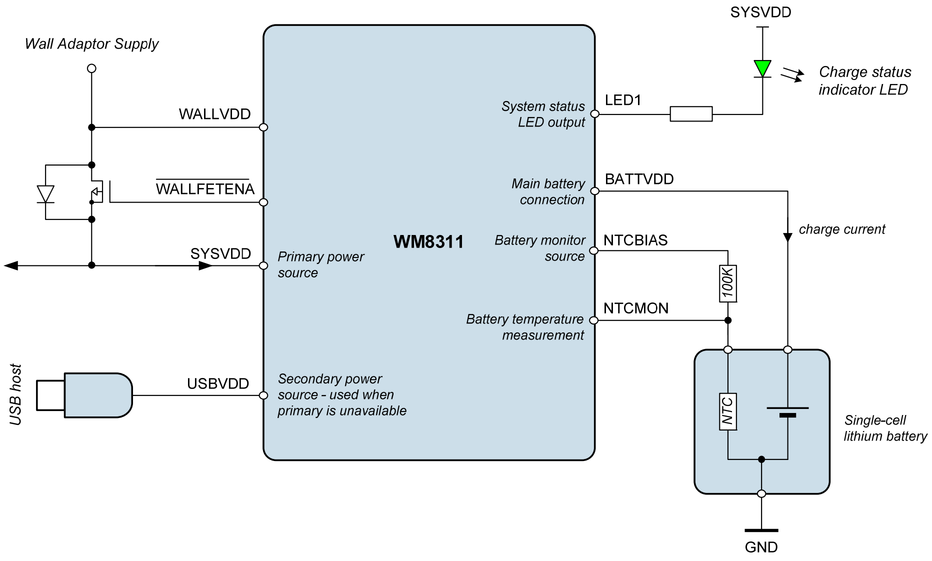


Figure 25 Typical Connections for WM8311 Battery Charger

The main battery terminal is connected to BATTVDD. The WM8311 also incorporates a battery temperature monitoring circuit, which monitors the NTC thermistor that is typically incorporated within a rechargeable battery pack. The NTCMON pin allows the charger to detect a hot or cold battery condition that may be outside the battery's usable operating conditions. Battery removal is also detected using the NTCMON pin.

The bias resistor connected between NTCBIAS and NTCMON should be a 1% tolerance resistor with a nominal value equal to the value of the battery's NTC thermistor at 25°C.

The temperature monitoring circuit can be disabled by shorting NTCMON to LDO12VOUT. This is only recommended if there is no NTC thermistor incorporated in the battery pack or if battery temperature monitoring is provided by other methods. Note that the short between NTCMON and LDO12VOUT is only sensed during start-up; the temperature monitoring circuit cannot be enabled / disabled dynamically in the ON or SLEEP power states.

See Section 17.7.7 for more details of the battery temperature monitoring function.

A typical battery charge cycle is illustrated in Figure 26. This shows both the trickle charge and fast charge processes.

The trickle charge mode is a constant current mode. The small charge current in this mode is suitable for pre-conditioning a deeply discharged battery, or when only limited power is available for battery charging. When the charger is enabled and the conditions for fast charging are not met, then trickle charging is selected. (Note that fast charging is not permitted if the battery voltage is below the defective battery threshold voltage.) Trickle charging is disabled when the charger enters the fast charging stage, or when the charge current drops to a programmable 'End of Charge' threshold level at the end of the constant voltage charge phase.

The fast charge mode is also a constant current mode, but higher charge currents are possible in this mode. In the fast charge phase, the WM8311 drives a programmable constant current into the battery through the BATTVDD pin. During this phase, the battery voltage rises until the battery reaches the target voltage.

When the battery reaches the target voltage (through trickle charge and/or fast charge), the charger enters the constant voltage charge phase, in which the WM8311 regulates BATTVDD to the target voltage. During this phase of the charge process, the charge current decreases over time as the battery approaches its fully charged state. Battery charging is terminated when the current falls to a programmable 'End of Charge' threshold level at the end of the constant voltage charge phase.

Note that, at any time during trickle charging or fast charging, the battery may be required to supplement the USB or Wall Adaptor power source. In this case, the battery voltage may drop while it is providing power to the system. The charger resumes operation automatically as soon as sufficient current capacity is available from the main power source.

After the battery has been fully charged and the charge process has been terminated, battery charging will automatically re-start if the battery voltage falls below the charger re-start threshold.

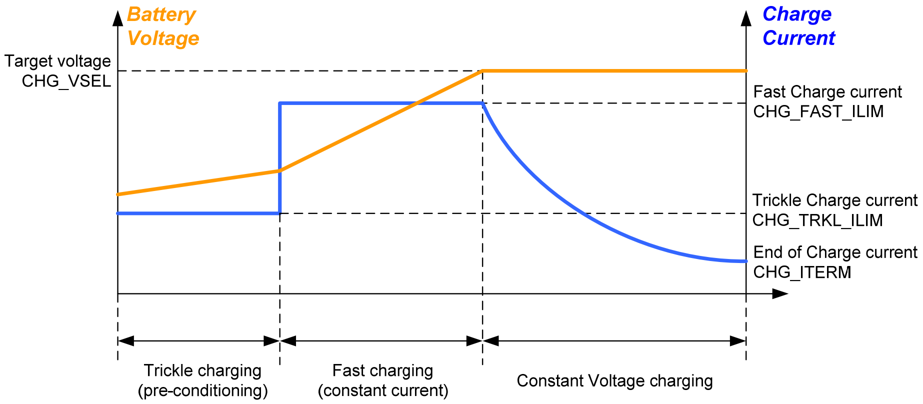


Figure 26 A Typical Charge Cycle

17.7.2 BATTERY CHARGER ENABLE

The battery charger may be enabled when the WM8311 is in the ON or SLEEP power states. Note that battery charging is only possible when the selected power source is within normal operating limits. See Section 17.7.8 for further details of battery charging in the SLEEP power state.

The battery charger is enabled when the CHG_ENA register bit is set to 1. When enabled, it checks if the conditions for charging are fulfilled and it controls the charging processes accordingly. The status of the battery charger can be read from the CHG_ACTIVE register bit.

The target voltage for the battery is set by the CHG_VSEL field, as defined in Table 57. It is important that this field is correctly set according to the type of battery that is connected. Incorrect setting of this register may lead to a safety hazard condition.

The trickle charge current is selected using the CHG_TRKL_ILIM field. This is the maximum trickle charge current - the actual charge current will be reduced if the battery is fully charged, or if the system supply, SYSVDD, drops as described in Section 17.7.1.

When the battery reaches the target voltage, the charger enters the constant voltage charge phase, in which the WM8311 regulates BATTVDD to the target voltage. When the charger is in the constant voltage charge phase, then the CHG_TOPOFF bit will be set to indicate that the charge is approaching completion.

The WM8311 incorporates thermal sensors to detect excessive temperatures within the device and to provide self-protection (see Section 26). By default, the battery charger will be disabled if the Thermal Warning condition occurs, and will be re-enabled after the condition has cleared. This response can be disabled by setting CHG_CHIP_TEMP_MON = 0, allowing the battery charge to continue. The Thermal Warning threshold is the lower of the two device temperature thresholds; the Thermal Shutdown threshold is the higher threshold. Note that the Thermal Shutdown condition cannot be ignored; this event causes a System Reset and a termination of battery charging.

If the WM8311 is commanded to the OFF state for any reason, then battery charging will be terminated. The CHG_OFF_MASK bit can be used to prevent certain OFF transitions whilst the battery charger is active. Setting the CHG_OFF_MASK bit causes a ‘Software OFF request’, ‘ON pin request’ or GPIO OFF request to be ignored whilst the charger is active. See Section 11.3 for a full list of OFF transition events.

The register control fields for trickle charging are described in Table 57. See Section 17.7.4 for details of battery charge termination.

Note that the Battery Charger control registers are locked by the WM8311 User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16456 (4048h) Charger Control 1	15	CHG_ENA	0	Battery Charger Enable 0 = Disable 1 = Enable *Protected by user key*
	0	CHG_CHIP_TEMP_ MON	1	Battery Charger Thermal warning select 0 = Thermal Warning is ignored 1 = Thermal Warning pauses Battery Charger *Protected by user key*
R16457 (4049h) Charger Control 2	14	CHG_OFF_MASK	0	Battery Charger OFF mask select 0 = OFF requests not masked 1 = OFF requests masked during Charging *Protected by user key*
	7:6	CHG_TRKL_ILIM [1:0]	00	Battery Trickle Charge current limit 00 = 50mA 01 = 100mA 10 = 150mA 11 = 200mA *Protected by user key*
	5:4	CHG_VSEL [1:0]	00	Battery Charger target voltage 00 = 4.05V 01 = 4.10V 10 = 4.15V 11 = 4.20V Note that incorrect setting of this register may lead to a safety hazard condition. *Protected by user key*
R16458 (404Ah) Charger Status	9	CHG_TOPOFF	0	Battery Charger constant-voltage charge mode status 0 = Constant-voltage mode not active 1 = Constant-voltage mode is active
	8	CHG_ACTIVE	0	Battery Charger status 0 = Not charging 1 = Charging

Table 57 Battery Charger Control

The Battery Charger is associated with a number of Interrupt flags. Whenever the Battery Charger state changes, the CHG_MODE_EINT interrupt is set (see Section 17.7.8). This interrupt is set whenever charging starts, charging stops, fast charge is selected, fast charge is de-selected, an overtemperature condition occurs, or if the charger detects a battery failure. The CHG_START_EINT interrupt is also set whenever Battery Charging commences, including after pause due to USB limit or over-temperature condition.

17.7.3 FAST CHARGING

Fast charging provides a faster way to charge the battery than is possible with trickle charge. See Section 17.7.1 for a description of fast charging.

Fast charging mode is only possible under certain conditions. It is only possible when the selected power source is Wall or when the USB current limit is set to 500mA or more. It is also required that the battery voltage is above the fast charge voltage threshold; this ensures that fast charging is not applied to a heavily discharged battery.

Fast charging is enabled by setting the CHG_FAST register bit, provided that the conditions for fast charging are satisfied. The fast charge current limit is selected using the CHG_FAST_ILIM field.

The battery charge current is automatically controlled, up to a maximum set by CHG_FAST_ILIM. The current is automatically limited when required if the battery is fully charged, or if the system supply, SYSVDD, drops as described in Section 17.7.1.

The fast charge mode comprises two phases, as described in Section 17.7.1. When the charger is in the constant voltage charge phase, the CHG_TOPOFF bit will be set to indicate that the charge is approaching completion.

When the battery reaches the target voltage, the charger enters the constant voltage charge phase, in which the WM8311 regulates BATTVDD to the target voltage. When the charger is in the constant voltage charge phase, then the CHG_TOPOFF bit will be set (see Section 17.7.2) to indicate that the charge is approaching completion.

The register control fields for fast charging are described in Table 58. Note that the Battery Charger control registers are locked by the WM8311 User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16456 (4048h) Charger Control 1	15	CHG_FAST	0	Battery Fast Charge Enable 0 = Disable 1 = Enable *Protected by user key*
R16457 (4049h) Charger Control 2	3:0	CHG_FAST_ILIM [3:0]	0010	Battery Fast Charge current limit 0000 = 0mA 0001 = 50mA 0010 = 100mA 0011 = 150mA 0100 = 200mA 0101 = 250mA 0110 = 300mA 0111 = 350mA 1000 = 400mA 1001 = 450mA 1010 = 500mA 1011 = 600mA 1100 = 700mA 1101 = 800mA 1110 = 900mA 1111 = 1000mA *Protected by user key*

Table 58 Fast Charge Control

17.7.4 CHARGER TIMEOUT AND TERMINATION

Fast charging and trickle charging is terminated under any of the following conditions:

- Charge current falls below the ‘End of Charge’ threshold
- Charger timeout
- Battery fault or overvoltage condition (see Section 17.7.6)
- Chip overtemperature condition (see Section 17.7.2)
- Transition to the OFF power state

The End of Charge current threshold can be set using the CHG_ITERM register field, as defined in Table 59. Charging is terminated when the charge current is below the CHG_ITERM threshold, provided also that the battery voltage has reached the target voltage CHG_VSEL at the end of the constant voltage charge phase.

If the battery charger current is reduced or paused due to a drop in SYSVDD voltage (as described in Section 17.7.1.), then the End of Charge current threshold does not cause battery charging to be terminated, as the charge current is not indicative of the battery charge status in this case.

The battery charger has a programmable safety timer to control the battery charge duration. The timer is started when either fast charging or trickle charging commences, including charging that is triggered as a result of the battery voltage dropping to the charger re-start threshold. The timer is re-started if the charging mode is changed (eg. between fast charge and trickle charge modes). The timeout period may be set by writing to the CHG_TIME register field; this allows charge times of up to 510mins (8.5 hours) to be selected.

When the timeout period completes, the battery charge cycle is terminated. In this event, the charger will not re-start until the charger has been disabled (CHG_ENA = 0) and then re-enabled (CHG_ENA = 1). Note that the charger re-start threshold is ignored in this case, and the charger will not re-start automatically.

The elapsed battery charge time can be read from the CHG_TIME_ELAPSED register field. This field is reset whenever the charger timer is started (ie. by starting charging, stopping charging, or changing charging modes).

If charging is paused due to a battery temperature or chip temperature condition, then the charge timer is paused until charging resumes.

Battery charging is terminated if removal of the battery is detected via the NTC monitor connections (see Section 17.7.2).

The register control fields for battery charger termination are described in Table 59. Note that the Battery Charger control registers are locked by the WM8311 User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16456 (4048h) Charger Control 1	12:10	CHG_ITERM [2:0]	000	Battery End of Charge current threshold 000 = 20mA 001 = 30mA 010 = 40mA 011 = 50mA 100 = 60mA 101 = 70mA 110 = 80mA 111 = 90mA *Protected by user key*

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16457 (4049h) Charger Control 2	11:8	CHG_TIME [3:0]	0110	Battery charger timeout 0000 = 60min 0001 = 90min 0010 = 120min 0011 = 150min 0100 = 180min 0101 = 210min 0110 = 240min 0111 = 270min 1000 = 300min 1001 = 330min 1010 = 360min 1011 = 390min 1100 = 420min 1101 = 450min 1110 = 480min 1111 = 510min *Protected by user key*
R16458 (404Ah) Charger Status	7:0	CHG_TIME_ELAPSED [7:0]	00h	Battery charger elapsed time 00h = 0min 01h = 2min 02h = 4min 03h = 6min ... FFh = 510min

Table 59 Battery Charger Termination

The Battery Charger is associated with a number of Interrupt flags, as described in Section 17.7.8. If battery charging is terminated due to the End of Charge current threshold being reached, then the CHG_END_EINT interrupt is set. If battery charging is terminated due to the charge timeout, then the charger will set the CHG_TO_EINT interrupt.

17.7.5 BATTERY CHARGE CURRENT MONITORING

The battery charge current can be monitored externally or internally. When the CHG_IMON_ENA bit is set, then the WM8311 sources an output current at AUXADCIN1 which is proportional to the battery charger current.

When a resistor is connected between AUXADCIN1 and GND, then the charge monitor current is converted to a voltage which can be measured by the Auxiliary ADC. The recommended value of the resistor is 10kΩ. Larger resistors may also be used in order to improve the measurement resolution, but the voltage at AUXADCIN1 must not exceed 2.5V.

Note that the CHG_IMON_ENA register is locked by the WM8311 User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16456 (4048h) Charger Control 1	2	CHG_IMON_ENA	0	Enable battery charge current monitor at AUXADCIN1. 0 = Disabled 1 = Enabled (Note - a resistor is required between AUXADCIN1 and GND in order to measure the charge current using the AUXADC. The recommended resistor value is 10k.) *Protected by user key*

Table 60 Battery Charge Current Monitoring

The AUXADCIN1 monitor output current is equal to the battery charge current divided by 12500. The battery charge current can be determined by measuring the voltage at the AUXADCIN1 pin, as described in the following equations.

$$\text{Monitor Current } I_M = \frac{\text{Charge Current } I_C}{12500} = \frac{V_{AUXADCIN1}}{R}$$

$$\text{Charge Current } I_C = \frac{V_{AUXADCIN1} \text{ x } 12500}{10000} \quad \textit{(assuming 10k resistor, R)}$$

For example, a measurement of 0.72V at AUXADCIN1 would indicate that the battery charge current is 900mA.

Note that the integrated Auxiliary ADC can be used to perform this measurement if required. In this case, the digitised AUXADC measurement (AUX_DATA) represents the battery charge current in accordance with the following equation.

$$\text{Charge Current } I_C \text{ (mA)} = \frac{\text{AUX\_DATA x 1.465 x 12500}}{10000} \quad \textit{(assuming 10k resistor, R)}$$

See Section 18 for further details of the Auxiliary ADC.

17.7.6 BATTERY FAULT / OVERVOLTAGE CONDITIONS

The battery is monitored to detect an overvoltage or failure condition. These features are incorporated to prevent malfunction of the battery charger or of the WM8311 system.

The BATT_OV_STS bit indicates if an overvoltage condition has been detected. The overvoltage threshold is defined in Section 7.7. If a battery overvoltage condition is detected, then charging is terminated and the CHG_OV_EINT interrupt flag is set (see Section 17.7.8).

The battery charger also detects if the battery is faulty. This is detected if the battery voltage does not reach the fast charge threshold voltage within the defective battery timeout period (see Section 7.7), or within a quarter of the charging time CHG_TIME (whichever is the longer time).

The battery failure condition is cleared if the battery voltage rises above the defective battery threshold, or if any of the WM8311 power sources (including the battery) is removed and re-connected. When the failure condition is cleared, the charger then reverts back to its initial state, and may re-start if the conditions for charging are fulfilled.

If the battery failure condition is detected in fast charge mode, then the charger reverts to trickle charging mode. If the fault persists, then trickle charging stops as described above.

If battery failure condition is detected, then charging is terminated and the CHG_BATT_FAIL_EINT interrupt is set (see Section 17.7.8).

The battery overvoltage bit is defined in Table 61.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16458 (404Ah) Charger Status	15	BATT_OV_STS	0	Battery Overvoltage status 0 = Normal 1 = Battery Overvoltage

Table 61 Battery Overvoltage Status

17.7.7 BATTERY TEMPERATURE MONITORING

As described in Section 17.7.1, the WM8311 is designed to monitor battery temperature using a standard NTC thermistor component which is typically incorporated within the battery pack. This allows the battery charger to detect a hot or cold battery condition that may be outside the battery's usable operating conditions. (Note that the temperature monitoring circuit also detects if the NTC circuit is not connected, in order to mask any erroneous fault indications.)

The BATT_HOT_STS and BATT_COLD_STS register bits indicate if a hot battery or cold battery temperature condition has been detected. If a battery temperature fault condition is detected, then charging is paused temporarily and the CHG_BATT_HOT_EINT or CHG_BATT_COLD_EINT interrupt is set (see Section 17.7.8).

Under typical circuit configurations, the hot and cold temperature conditions are designed to be +40°C and 0°C respectively. These temperatures can be adjusted by the use of different resistor components, as described in the applications information in Section 30.6.

Battery removal is also detected using the NTC circuit. This is used to terminate battery charging if a battery is removed during charging.

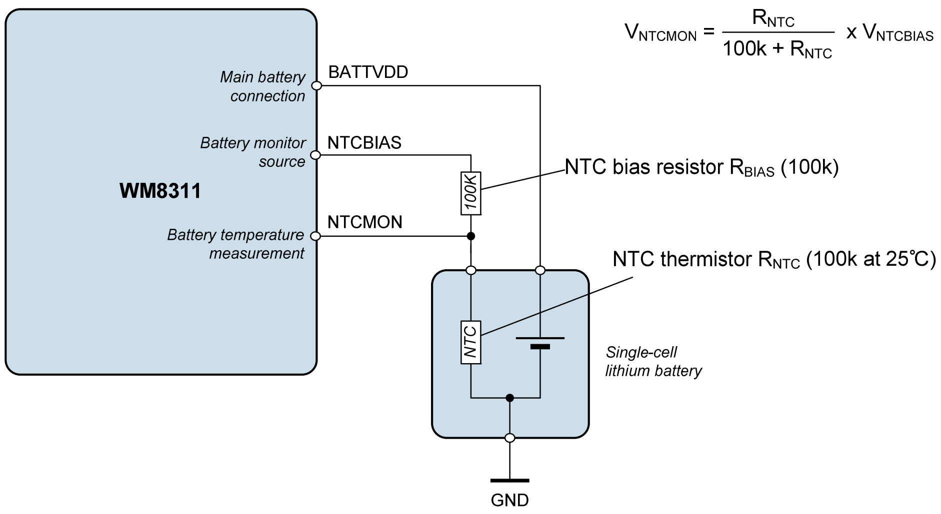
The temperature monitoring circuit can be disabled by shorting NTCMON to LDO12VOUT. This is only recommended if there is no NTC thermistor incorporated in the battery pack or if battery temperature monitoring is provided by other methods. Note that the short between NTCMON and LDO12VOUT is only sensed during start-up; the temperature monitoring circuit cannot be enabled / disabled dynamically in the ON or SLEEP power states.

The battery temperature status bits are described in Table 62.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16458 (404Ah) Charger Status	11	BATT_HOT_STS	0	Battery Hot status 0 = Normal 1 = Battery Hot
	10	BATT_COLD_STS	0	Battery Cold status 0 = Normal 1 = Battery Cold

Table 62 Battery Temperature Status

Battery temperature monitoring is configured as illustrated in Figure 27. The principle of operation is that a temperature change in the battery pack causes a change in resistance of the NTC thermistor, which results in a voltage change at the NTCMON pin.



$$V_{NTCMON} = \frac{R_{NTC}}{100k + R_{NTC}} \times V_{NTCBIAS}$$

Figure 27 Battery Temperature Monitoring

For information on how to set the hot and cold temperature limits, see the Applications Information in Section 30.6.

17.7.8 BATTERY CHARGER INTERRUPTS

The Battery Charger is associated with a number of Interrupt event flags, described in Table 63. Each of these secondary interrupts triggers a primary Battery Charger Interrupt, CHG_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 63.

If any Battery Charger interrupt event occurs while in the SLEEP power state, then a WAKE transition request is generated. Note that this behaviour is not affected by any of the interrupt mask bits. See Section 11.3 for a description of the WM8311 power state transitions.

If any of the Battery Charger Interrupts is asserted when a SLEEP transition is requested, then the transition will be unsuccessful and the WM8311 will remain in the ON power state.

If battery charging is commenced in the SLEEP power state, the WM8311 will transition to the ON power state, as a result of the CHG_START_EINT interrupt. Battery charging in the SLEEP power state is only possible by clearing the CHG_START_EINT interrupt before commanding the transition into the SLEEP power state.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	15	CHG_BATT_HOT_EINT	Battery Hot interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	14	CHG_BATT_COLD_EINT	Battery Cold interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	13	CHG_BATT_FAIL_EINT	Battery Fail interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	12	CHG_OV_EINT	Battery Overvoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	11	CHG_END_EINT	Battery Charge End interrupt (End of Charge Current threshold reached) (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	10	CHG_TO_EINT	Battery Charge Timeout interrupt (Charger Timer has expired) (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	9	CHG_MODE_EINT	Battery Charge Mode interrupt (Charger Mode has changed) (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	8	CHG_START_EINT	Battery Charge Start interrupt (Charging has started) (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16410 (401Ah) Interrupt Status 2 Mask	15	IM_CHG_BATT_HOT_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	14	IM_CHG_BATT_COLD_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

ADDRESS	BIT	LABEL	DESCRIPTION
	13	IM_CHG_BATT_FAIL_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	12	IM_CHG_OV_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	11	IM_CHG_END_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	10	IM_CHG_TO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	9	IM_CHG_MODE_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	8	IM_CHG_START_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 63 Battery Charger Interrupts

17.7.9 BATTERY CHARGER STATUS

The status of the Battery Charger can be read from various registers and interrupts noted in the above sections. The Battery Charger status can also be read from the CHG_STATE register field, as defined in Table 64.

Note that the LED Status outputs can also be configured to indicate the Battery Charger status - see Section 22.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16458 (404Ah) Charger Status	14:12	CHG_STATE [2:0]	000	Battery Charger state 000 = Off 001 = Trickle Charge 010 = Fast Charge 011 = Trickle Charge overtemperature 100 = Fast Charge overtemperature 101 = Defective 110 = Reserved 111 = Reserved

Table 64 Battery Charger State

18 AUXILIARY ADC

18.1 GENERAL DESCRIPTION

The WM8311 incorporates a 12-bit Auxiliary ADC (AUXADC). This can be used to perform a number of system measurements (including supply voltages and battery temperature) and can also be used to measure analogue voltages from external sources and sensors.

External inputs to the AUXADC should be connected to the pins AUXADCIN1, AUXADCIN2, AUXADCIN3 and AUXADCIN4. The maximum voltage that can be measured is determined by the power domain associated with each (see Section 3). In the case of AUXADCIN 1-3, the maximum voltage is SYSVDD; in the case of AUXADCIN4, the maximum voltage is TPVDD. Note that SYSVDD varies according to the voltage of the preferred power source (WALLVDD, USBVDD or BATTVDD).

The AUXADC can also measure the voltage on WALLVDD, USBVDD and BATTVDD. Internal resistor dividers enable voltages higher than SYSVDD to be measured by the AUXADC - voltages up to 6V can be measured on these pins.

18.2 AUXADC CONTROL

The AUXADC is enabled by setting the AUX_ENA register bit. By default, the AUXADC is not enabled in the SLEEP state, but this can be selected using the AUX_SLPENA field.

The AUXADC measurements can be initiated manually or automatically. For automatic operation, the AUX_RATE register is set according to the required conversion rate, and conversions are enabled by setting the AUX_CVT_ENA bit. For manual operation, the AUX_RATE register is set to 00h, and each manual conversion is initiated by setting the AUX_CVT_ENA bit. In manual mode, the AUX_CVT_ENA bit is reset by the WM8311 after each conversion. (Note that the conversion result is not available for readback until the AUXADC Interrupt is asserted, as described in Section 18.5.)

Note that the AUXADC measurements are interleaved with the Touch Panel measurements, when both are enabled. If a Touch Panel measurement set is already in progress at the time when an AUXADC measurement is due, then the AUXADC measurement will be delayed until after the Touch Panel measurement set has completed. This applies equally to Manual and to Automatic AUXADC modes.

The AUXADC has 10 available input sources. Each of these inputs is enabled by setting the respective bit in the AuxADC Source Register (R16431).

For each AUXADC measurement event (in Manual or Automatic modes), the WM8311 selects the next enabled input source. Any number of inputs may be selected simultaneously; the AUXADC will measure each one in turn. Note that only a single AUXADC measurement is made on any Manual or Automatic trigger.

For example, if the AUX1, BATT and USB voltages are enabled for AUXADC measurement, then AUX1 would be measured in the first instance, and BATT then USB would be measured on the next manual or automatic AUXADC triggers. In this case, a total of three manual or automatic AUXADC triggers would be required to measure all of the selected inputs.

The control fields associated with initiating AUXADC measurements are defined in Table 65.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16430 (402Eh) AuxADC Control	15	AUX_ENA	0	AUXADC Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.
	14	AUX_CVT_ENA	0	AUXADC Conversion Enable 0 = Disabled 1 = Enabled In automatic mode, conversions are enabled by setting this bit. In manual mode (AUX_RATE = 0), setting this bit will initiate a conversion; the bit is reset automatically after each conversion.
	12	AUX_SLPENA	0	AUXADC SLEEP Enable 0 = Disabled 1 = Controlled by AUX_ENA
	5:0	AUX_RATE [5:0]	00_0000	AUXADC Conversion Rate 0 = Manual 1 = 2 samples/s 2 = 4 samples/s 3 = 6 samples/s … 31 = 62 samples/s 32 = Reserved 33 = 16 samples/s 34 = 32 samples/s 35 = 48 samples/s … 63 = 496 samples/s
R16431 (402Fh) AuxADC Source	9	AUX_WALL_SEL	0	AUXADC WALL input select 0 = Disable WALLVDD measurement 1 = Enable WALLVDD measurement
	8	AUX_BATT_SEL	0	AUXADC BATT input select 0 = Disable BATTVDD measurement 1 = Enable BATTVDD measurement
	7	AUX_USB_SEL	0	AUXADC USB input select 0 = Disable USBVDD measurement 1 = Enable USBVDD measurement
	6	AUX_SYSVDD_SEL	0	AUXADC SYSVDD input select 0 = Disable SYSVDD measurement 1 = Enable SYSVDD measurement
	5	AUX_BATT_TEMP_SEL	0	AUXADC Battery Temp input select 0 = Disable Battery Temp measurement 1 = Enable Battery Temp measurement
	4	AUX_CHIP_TEMP_SEL	0	AUXADC Chip Temp input select 0 = Disable Chip Temp measurement 1 = Enable Chip Temp measurement
	3	AUX_AUX4_SEL	0	AUXADCIN4 input select 0 = Disable AUXADCIN4 measurement 1 = Enable AUXADCIN4 measurement
	2	AUX_AUX3_SEL	0	AUXADCIN3 input select 0 = Disable AUXADCIN3 measurement 1 = Enable AUXADCIN3 measurement

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	1	AUX_AUX2_SEL	0	AUXADCIN2 input select 0 = Disable AUXADCIN2 measurement 1 = Enable AUXADCIN2 measurement
	0	AUX_AUX1_SEL	0	AUXADCIN1 input select 0 = Disable AUXADCIN1 measurement 1 = Enable AUXADCIN1 measurement

Table 65 AUXADC Control

18.3 AUXADC READBACK

Measured data from the AUXADC is read via the AuxADC Data Register (R16429), which contains two fields. The AUXADC Data Source is indicated in the AUX_DATA_SRC field; the associated measurement data is contained in the AUX_DATA field.

Reading from the AuxADC Data Register returns a 12-bit code which represents the most recent AUXADC measurement on the associated channel. It should be noted that every time an AUXADC measurement is written to the AuxADC Data Register, the previous data is overwritten - the host processor should ensure that data is read from this register before it is overwritten. The AUXADC interrupts can be used to indicate when new data is available - see Section 18.5.

The 12-bit AUX_DATA field can be equated to the actual voltage (or temperature) according to the following equations, where AUX_DATA is regarded as an unsigned integer:

$$\text{Voltage (mV)} = \text{AUX\_DATA} \times 1.465$$

$$\text{Chip Temp } (^\circ\text{C}) = \frac{498 - \text{AUX\_DATA}}{1.09}$$

Battery Temperature measurement varies according to the selected NTC thermistor component.

In a typical application, it is anticipated that the AUXADC Interrupts would be used to control the AUXADC readback - the host processor should read the AUXADC Data Register in response to the AUXADC Interrupt event. See Section 18.5 for details of AUXADC Interrupts. In Automatic AUXADC mode, the processor should complete this action before the next measurement occurs, in order to avoid losing any AUXADC samples. In Manual conversion mode, the interrupt signal provides confirmation that the commanded measurement has been completed.

The control fields associated with initiating AUXADC readback are defined in Table 66.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16429 (402Dh) AuxADC Data	15:12	AUX_DATA_SRC [3:0]	000	AUXADC Data Source 0 = Reserved 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage 8 = USB voltage 9 = BATT voltage 10 = WALL voltage 11 = Reserved 12 = Reserved 13 = Reserved 14 = Reserved 15 = Reserved
	11:0	AUX_DATA [11:0]	000h	AUXADC Measurement Data Voltage (mV) = AUX_DATA x 1.465 ChipTemp (°C) = (498 - AUX_DATA) / 1.09 BattTemp (°C) = (value is dependent on NTC thermistor)

Table 66 AUXADC Readback

18.4 DIGITAL COMPARATORS

The WM8311 has four digital comparators which may be used to compare AUXADC measurement data against programmable threshold values. Each comparator has a status bit, and also an associated interrupt flag (described in Section 18.5), which indicates that the associated data is beyond the threshold value.

The digital comparators are enabled using the DCMPn_ENA register bits as described in Table 65.

After an AUXADC conversion, the measured value is compared with the threshold level of any associated comparator(s). Note that this comparison is only performed following a conversion.

The source data for each comparator is selected using the DCMP*n*_SRC register bits; this selects one of eight possible AUXADC channels for each comparator. If required, the same AUXADC channel may be selected for more than one comparator; this would allow more than one threshold to be monitored on the same AUXADC channel. Note that the coding of the 000b value of the DCMP*n*_SRC fields differs between the four comparators.

The DCMP*n*_GT register bits select whether the status bit and associated interrupt flag will be asserted when the measured value is above the threshold or when the measured value is below the threshold. The output of the most recent threshold comparison is indicated in the DCOMP*n*_STS fields.

The threshold DCMP*n*_THR is a 12-bit code for each comparator. This field follows the same voltage or temperature coding as the associated AUXADC channel source (see Section 18.3).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16432 (4030h) Comparator Control	11	DCOMP4_STS	0	Digital Comparator 4 status 0 = Comparator 4 threshold not detected 1 = Comparator 4 threshold detected (Trigger is controlled by DCMP4_GT)

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	10	DCOMP3_STS	0	Digital Comparator 3 status 0 = Comparator 3 threshold not detected 1 = Comparator 3 threshold detected (Trigger is controlled by DCMP3_GT)
	9	DCOMP2_STS	0	Digital Comparator 2 status 0 = Comparator 2 threshold not detected 1 = Comparator 2 threshold detected (Trigger is controlled by DCMP2_GT)
	8	DCOMP1_STS	0	Digital Comparator 1 status 0 = Comparator 1 threshold not detected 1 = Comparator 1 threshold detected (Trigger is controlled by DCMP1_GT)
	3	DCMP4_ENA	0	Digital Comparator 4 Enable 0 = Disabled 1 = Enabled
	2	DCMP3_ENA	0	Digital Comparator 3 Enable 0 = Disabled 1 = Enabled
	1	DCMP2_ENA	0	Digital Comparator 2 Enable 0 = Disabled 1 = Enabled
	0	DCMP1_ENA	0	Digital Comparator 1 Enable 0 = Disabled 1 = Enabled
R16433 (4031h) Comparator 1	15:13	DCMP1_SRC [2:0]	000	Digital Comparator 1 source select 0 = USB voltage 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage
	12	DCMP1_GT	0	Digital Comparator 1 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP1_THR	000h	Digital Comparator 1 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)
R16434 (4032h) Comparator 2	15:13	DCMP2_SRC [2:0]	000	Digital Comparator 2 source select 0 = WALL voltage 1 = AUXADCIN1 2 = AUXADCIN2

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
				3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage
	12	DCMP2_GT	0	Digital Comparator 2 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP2_THR	000h	Digital Comparator 2 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)
R16435 (4033h) Comparator 3	15:13	DCMP3_SRC [2:0]	000	Digital Comparator 3 source select 0 = BATT voltage 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage
	12	DCMP3_GT	0	Digital Comparator 3 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP3_THR	000h	Digital Comparator 3 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)
R16436 (4034h) Comparator 4	15:13	DCMP4_SRC [2:0]	000	Digital Comparator 4 source select 0 = Reserved 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage
	12	DCMP4_GT	0	Digital Comparator 4 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than or equal to threshold
	11:0	DCMP4_THR	000h	Digital Comparator 4 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)

Table 67 AUXADC Digital Comparator Control

18.5 AUXADC INTERRUPTS

The AUXADC is associated with a number of Interrupt event flags to indicate when new AUXADC data is ready, or to indicate that one or more of the digital comparator thresholds has been crossed. Each of these secondary interrupts triggers a primary AUXADC Interrupt, AUXADC_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 68.

Note that AUXADC_DATA_EINT is not cleared by reading the measured AUXADC data, it can only be cleared by writing ‘1’ to the AUXADC_DATA_EINT register.

The AUXADC interrupts can be programmed using bits in Table 68.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	8	AUXADC_DATA_EINT	AUXADC Data Ready interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	7:4	AUXADC_DCOMP*n*_EINT	AUXADC Digital Comparator *n* interrupt (Trigger is controlled by DCMP*n*_GT) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	8	IM_AUXADC_DATA_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	7:4	IM_AUXADC_DCOMP*n*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Note: *n* is a number between 1 and 4 that identifies the individual Comparator.			

Table 68 AUXADC Interrupts

19 TOUCH PANEL CONTROLLER

19.1 GENERAL DESCRIPTION

The WM8311 incorporates a Touch Panel controller interface, supporting standard resistive 4-wire and 5-wire panel types. The controller supports X, Y co-ordinate measurement and Pen Down detection. The 4-wire configuration also supports Touch Pressure (Z-axis) measurement.

The Touch Panel interfaces via GPIO pins 13-16. (In 5-wire mode, the AUXADCIN4 pin is also used.) The controller provides high resolution digitiser measurements, using the same 12-bit AUXADC as described in Section 18. Touch Panel conversion requests are interleaved with AUXADC measurement requests.

The Touch Panel can be enabled or disabled in the SLEEP state; Pen Down detection can be used to issue a WAKE request, including when the Touch Panel is disabled.

Touch Panel Interrupts can be generated on completion of a set of measurements, or on Pen Down detection. Read access to the Touch Panel measurement data is controlled in order to ensure the host always reads a complete set of data, and does not read mixed data that relates to separate measurement events.

An overview of Touch Panel operating principles is provided in Section 19.6.

19.2 TOUCH PANEL CONFIGURATION

The Touch Panel interface uses GPIO pins 13-16. When the Touch Panel is enabled, the GPIO functionality on these pins must be disabled by tri-stating the GPIO using the GPn_ENA register bits (see Section 21.3).

When the Touch Panel is enabled, then TPVDD should be connected to the LDO13VOUT (INTVDD) power domain. It is important that TPVDD is not connected to a higher voltage than this. Note that, due to the ratiometric measurement method, the accuracy of the supply voltage does not affect the measurement accuracy.

The 5-wire Touch Panel interface also uses the AUXADCIN4 pin; in this case, the AUXADCIN4 input is not available to the AUXADC function.

The Touch Panel pin configuration differs between 4-wire and 5-wire modes as follows:

PIN NAME	4-WIRE FUNCTION	5-WIRE FUNCTION
GPIO13	Right contact	Bottom Right contact
GPIO14	Top contact	Top Right contact
GPIO15	Left contact	Top Left contact
GPIO16	Bottom contact	Bottom Left contact
AUXADCIN4	n/a	Wiper Contact

Table 69 Touch Panel Pin Configuration

The Touch Panel 4-wire or 5-wire mode is selected using the TCH_5WIRE bit.

Pressure measurement (4-wire mode only) uses a constant current source to measure the resistance between the top and bottom sheets of the touch panel. The current is selectable using TCH_ISEL, to suit different types of touch panel.

Pen Down detection sensitivity can be controlled using TCH_RPU. Decreasing the resistance makes the touch panel less sensitive; increasing the resistance makes the touch panel more sensitive.

The Touch Panel configuration register bits are defined in Table 70.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16425 (4029h) Touch Control 2	12	TCH_5WIRE	0	Touch Panel control mode 0 = 4-wire 1 = 5-wire
	8	TCH_ISEL	0	Pressure measurement current select 0 = 200uA 1 = 400uA Note - this applies to 4-wire mode only
	3:0	TCH_RPU [3:0]	0111	Pen-Down sensitivity (pull-up resistor) 0000 = 64k (most sensitive) 0001 = 64k / 2 0010 = 64k / 3 0011 = 64k / 4 …. 1111 = 64k / 16 (least sensitive)

Table 70 Touch Panel Configuration

19.3 TOUCH PANEL CONTROL

The Touch Panel is enabled by setting the TCH_ENA register bit. By default, the Touch Panel is not enabled in the SLEEP state, but this can be selected using the TCH_SLPENA field.

The Touch Panel can be configured to issue a WAKE request when the ‘Pen Down’ is detected by setting the TCH_PD_WK bit. This function is only supported when TCH_ENA = 1. Note that the WAKE request may be generated regardless of the TCH_SLPENA setting.

The Touch Panel measurements can be initiated manually or automatically. For automatic operation, the TCH_RATE register is set according to the required conversion rate, and measurements are enabled by setting the TCH_CVT_ENA bit. For manual operation, the TCH_RATE register is set to 00h, and a set of measurements is initiated by setting the TCH_CVT_ENA bit. In manual mode, the TCH_CVT_ENA bit is reset by the WM8311 after each set of measurements. (Note that the measurement results are not available for readback until the Touch Panel Data interrupt is asserted, as described in Section 19.5.)

Note that the Touch Panel measurements are interleaved with the AUXADC measurements, when both are enabled. If an AUXADC measurement set is already in progress at the time when an Touch Panel measurement is due, then the Touch Panel measurement will be delayed until after the AXUADC measurement set has completed. This applies equally to Manual and to Automatic Touch Panel modes.

The Touch Panel ‘Pen Down’ detection can be used to control measurements in automatic mode. When TCH_PDONLY is set, then automatic conversions will only be scheduled when ‘Pen Down’ is detected. In this mode, automatic conversions are suspended after a measurement has been made for which ‘Pen Down’ is not detected. Automatic measurements are resumed when ‘Pen Down’ is detected. Note that manual conversion commands are not affected by TCH_PDONLY.

For each Touch Panel measurement event (in Manual or Automatic modes), the WM8311 performs a set of measurements encompassing all enabled input sources; the X-axis, Y-axis and Z-axis measurements are enabled using the TCH_X_ENA, TCH_Y_ENA and TCH_Z_ENA register bits respectively. To allow settling time between consecutive measurements, a programmable delay is applied between the X, Y and Z-axis measurements; this is set using the TCH_DELAY field.

The control fields associated with initiating Touch Panel measurements are defined in Table 71.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16424 (4028h) Touch Control 1	15	TCH_ENA	0	Touch Panel Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.
	14	TCH_CVT_ENA	0	Touch Panel Conversion Enable 0 = Disabled 1 = Enabled In automatic mode, conversions are enabled by setting this bit. In manual mode (TCH_RATE = 0), setting this bit will initiate a set of conversion; the bit is reset automatically after each set of measurements.
	12	TCH_SLPENA	0	Touch Panel SLEEP Enable 0 = Disabled 1 = Controlled by TCH_ENA
	10	TCH_Z_ENA	0	Enables Z-axis touch panel measurements. (Z-axis is the pressure axis - 4-wire only.) 0 = Disabled 1 = Enabled
	9	TCH_Y_ENA	0	Enables Y-axis touch panel measurements 0 = Disabled 1 = Enabled
	8	TCH_X_ENA	0	Enables X-axis touch panel measurements 0 = Disabled 1 = Enabled
	7:5	TCH_DELAY [2:0]	010	Settling time between X, Y and Z measurements. (Nominal timing only; typically +/-20% of quoted values.) 000 = 30us 001 = 60us 010 = 120us 011 = 240us 100 = 480us 101 = 960us 110 = 1920us 111 = 3840us
	4:0	TCH_RATE [4:0]	0_0000	Touch-panel Conversion Rate 0 = Manual 1 = 16 packets/s 2 = 32 packets/s 3 = 48 packets/s … 31 = 496 packets/s
R16425 (4029h) Touch Control 2	13	TCH_PD_WK	0	WAKE transition select for Pen Down event 0 = Disabled 1 = Enabled

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	11	TCH_PDONLY	0	Select Automatic conversions only when Pen Down is detected. (No effect on Manual conversion.) 0 = Normal 1 = Pen-Down only

Table 71 Touch Panel Control

19.4 TOUCH PANEL READBACK

Measured data from the Touch Panel controller is read via the Touch Data registers. The X-axis, Y-axis and Z-axis (pressure) measurements are provided in the TCH_X, TCH_Y and TCH_Z registers respectively. The TCH_PD1, TCH_PD2 and TCH_PD3 bits indicate whether the Pen Down status was asserted when the measurement set was made.

To read a set of Touch Panel measurements, the host processor must access each of the applicable Touch Data registers. (Note that Z-axis measurement is applicable to 4-wire mode only.) When the host processor starts to read these registers, the WM8311 will inhibit any new touch panel measurements until the host processor has read all of the applicable registers. This ensures that the data read by the host processor all relates to the same set of measurements.

The touch panel inhibit (preventing new touch panel measurements) commences when any of the Touch Data registers is read. The touch panel inhibit ceases when all selected Touch Data registers have been read, or if a read/write operation is made to any other register.

If all 3 touch panel channels are selected (using TCH_X_ENA, TCH_Y_ENA and TCH_Z_ENA as described in Section 19.3), then all 3 Touch Data registers must be read before further measurements are permitted. If fewer channels are selected, then only those selected channels need to be read before touch panel measurements are enabled again.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16426 (402Ah) Touch Data X	15	TCH_PD1	0	Pen down status (indicates if the Pen Down was detected prior to the TP measurement) 0 = Pen Down not detected 1 = Pen Down detected
	11:0	TCH_X [11:0]	000h	Touch panel X-axis data
R16427 (402Bh) Touch Data Y	15	TCH_PD2	0	Pen down status (indicates if the Pen Down was detected prior to the TP measurement) 0 = Pen Down not detected 1 = Pen Down detected
	11:0	TCH_Y [11:0]	000h	Touch panel Y-axis data
R16428 (402Ch) Touch Data Z	15	TCH_PD3	0	Pen down status (indicates if the Pen Down was detected prior to the TP measurement) 0 = Pen Down not detected 1 = Pen Down detected
	11:0	TCH_Z [11:0]	000h	Touch panel Z-axis data

Table 72 Touch Panel Readback

19.5 TOUCH PANEL INTERRUPTS

Touch panel events are associated with two Interrupt event flags.

The TCHDATA_EINT interrupt bit is set when new Touch Panel data is available. This secondary interrupt triggers a primary Interrupt, TCHDATA_INT (see Section 23). This can be masked by setting the IM_TCHDATA_EINT mask bit as described in Table 73.

The TCHPD_EINT interrupt bit is set when a Touch Panel 'Pen Down' event is detected. This secondary interrupt triggers a primary Interrupt, TCHPD_INT (see Section 23). This can be masked by setting the IM_TCHPD_EINT mask bit as described in Table 73.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	10	TCHDATA_EINT	Touch panel Data interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	9	TCHPD_EINT	Touch panel Pen Down interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16409 (4019h) Interrupt Status 1 Mask	10	IM_TCHDATA_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	9	IM_TCHPD_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 73 Touch Panel Interrupts

19.6 TOUCH PANEL OPERATING PRINCIPLES

A typical resistive Touch Panel comprises two conductive sheets, connected via a switch matrix to the Touch Panel supply voltage. When the Touch Panel is touched (usually with a pen-style pointer), an electrical contact is made between the two sheets. The switch matrix is used to determine the position of the pen contact by establishing a potential divider on one of the conductive sheets in either the X-axis or Y-axis, and measuring the voltage on the other sheet.

Separate configuration is required for each axis measurement; these are configured one after the other to determine the X and Y co-ordinate positions. Note that, due to the ratiometric measurement method, the accuracy of the supply voltage does not affect the measurement accuracy in either axis.

Pen Down detection and Z-axis (pressure) measurements are achieved in a similar fashion, by configuring the switch matrix and taking the appropriate voltage measurement via an ADC. Note that Z-axis measurement is only supported in 4-wire configuration.

The standard operating principles of 4-wire and 5-wire Touch Panels are each described in the following pages.

19.6.1 4-WIRE TOUCH PANEL OPERATION

In 4-wire operation, the Touch Panel interface connects to the Left / Right sides of one sheet and to the Top / Bottom sides of the other sheet. The illustrations show the top sheet for X-axis and the bottom sheet for Y-axis, but the reverse is also possible.

X-axis measurement is performed by applying a potential difference between the Left and Right sides of the touch panel. When contact is made between the two sheets, the voltage present on the Top or Bottom connections is a measure of the X-axis position of the contact. The configuration is illustrated in Figure 28.

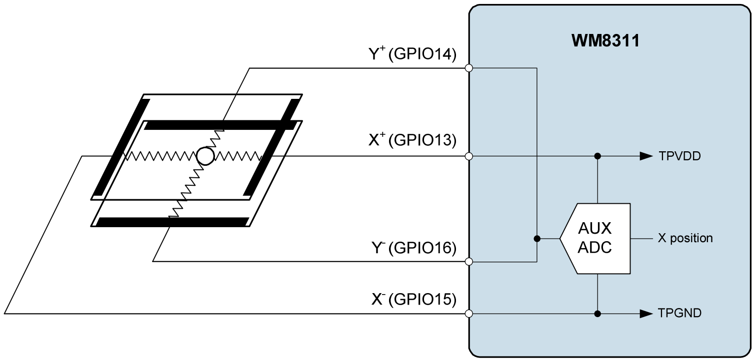


Figure 28 X-axis Measurement on 4-wire Touch Panel

Y-axis measurement is performed by applying a potential difference between the Top and Bottom sides of the touch panel. When contact is made between the two sheets, the voltage present on the Left or Right connections is a measure of the Y-axis position of the contact. The configuration is illustrated in Figure 29.

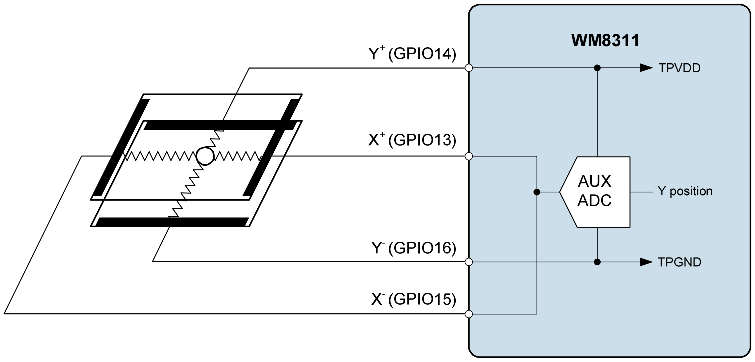


Figure 29 Y-axis Measurement on 4-wire Touch Panel

‘Pen Down’ detection uses a zero-power comparator with an internal, programmable pull-up resistor. When the touch panel is not being touched, no current flows between the touch panel sheets, and the comparator output is low. When the touch panel is touched, current flows through the panel and through the pull-up resistor, and the comparator output goes high. The sensitivity of the circuit can be adjusted using different values of pull-up resistor; a large pull-up resistance leads to the most sensitive response. The configuration is illustrated in Figure 30.

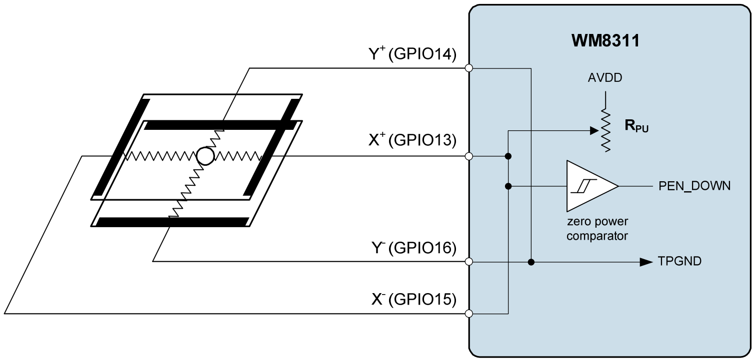


Figure 30 Pen-Down Detection on 4-wire Touch Panel

Touch pressure can only be determined indirectly, using the results of two separate measurements. A constant current is applied through the plates, and the voltage on each plate is measured. The difference between the two voltages is proportional to the resistance between the plates, which is a measure of the pressure being applied to the panel.

The configuration is illustrated in Figure 31. In this example, a constant current flows from the Top (Y^+) connection to the Left (X^-) connection. The Right (X^+) and Bottom (Y^-) points are measured in turn, and the difference, V_X - V_Y is equal to I_P x R_C, where I_P is the current applied and R_C is the resistance between the plates. The smaller the measured resistance, the greater the pressure being applied.

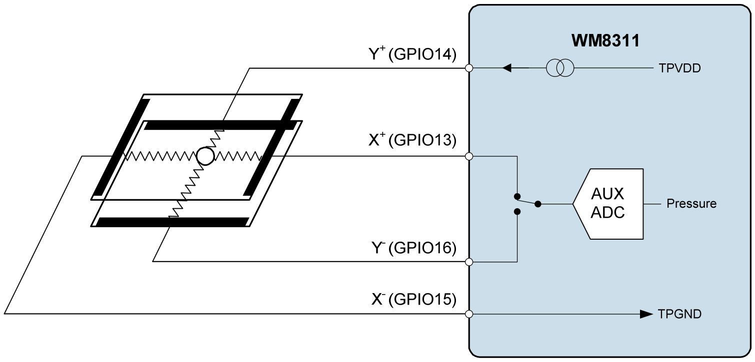


Figure 31 Z-axis (Pressure) Measurement on 4-wire Touch Panel

19.6.2 5-WIRE TOUCH PANEL OPERATION

In 5-wire operation, the Touch Panel interface connects to the four separate corners of one sheet and to a single point on the other sheet. The illustrations show the top sheet for wiper contact and the bottom sheet for corner contacts, but the reverse is also possible.

The principles of operation are the same for 5-wire and 4-wire modes, but different configuration of the switching matrix within the Touch Panel controller is required in order to implement the equivalent functionality.

X-axis measurement is performed by applying a potential difference between the Left and Right sides of the touch panel. This requires the two Left corners to be connected to one potential and the two Right corners connected to another. When contact is made between the two sheets, the voltage present on the Wiper connection is a measure of the X-axis position of the contact. The configuration is illustrated in Figure 32.

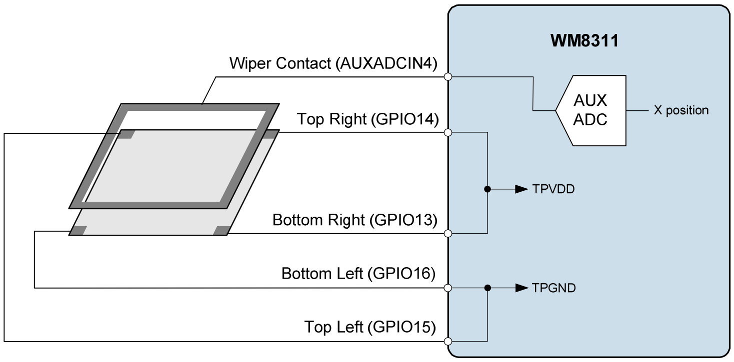


Figure 32 X-axis Measurement on 5-wire Touch Panel

Y-axis measurement is performed by applying a potential difference between the Top and Bottom sides of the touch panel. This requires the two Top corners to be connected to one potential and the two Bottom corners connected to another. When contact is made between the two sheets, the voltage present on the Wiper connection is a measure of the Y-axis position of the contact. The configuration is illustrated in Figure 33.

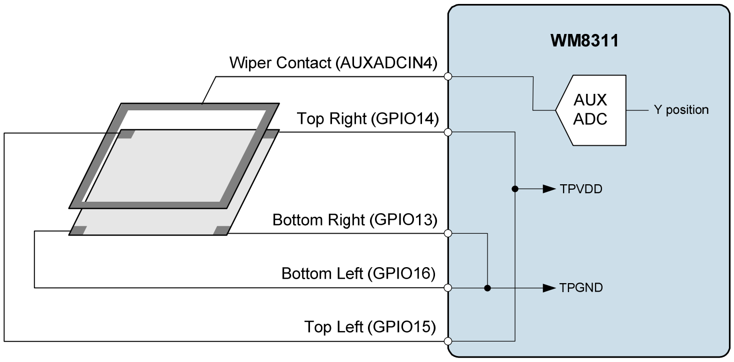


Figure 33 Y-axis Measurement on 5-wire Touch Panel

'Pen Down' detection uses a zero-power comparator with an internal, programmable pull-up resistor. When the touch panel is not being touched, no current flows between the touch panel sheets, and the comparator output is low. When the touch panel is touched, current flows through the panel and through the pull-up resistor, and the comparator output goes high. The sensitivity of the circuit can be adjusted using different values of pull-up resistor; a large pull-up resistance leads to the most sensitive response. The configuration is illustrated in Figure 34.

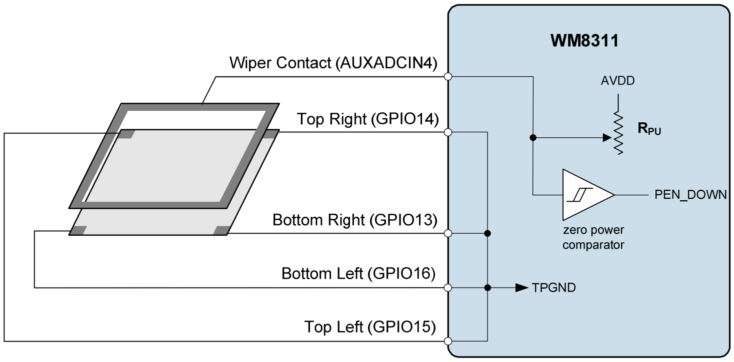


Figure 34 Pen-Down Detection on 5-wire Touch Panel

Note that Z-axis (pressure) measurement is not supported on the 5-wire Touch Panel.

20 REAL-TIME CLOCK (RTC)

20.1 GENERAL DESCRIPTION

The WM8311 provides a Real Time Clock (RTC) in the form of a 32-bit counter. The RTC uses the 32.768kHz crystal oscillator as its clock source and increments the register value once per second. (Note that a direct CMOS input may be used in place of the crystal oscillator; both options are described in Section 13.) To compensate for errors in the clock frequency, the RTC includes a frequency trim capability.

The RTC is enabled at all times, including when the WM8311 is in the BACKUP state. When required, the RTC can be maintained via a backup battery in the absence of any other power supply. In the absence of a backup battery, the RTC contents can be held (unclocked) for a limited period of up to 5 minutes via a 22μF capacitor.

The RTC incorporates an Alarm function. The Alarm time is held in a 32-bit register. When the RTC counter matches the Alarm time, a selectable response will be actioned.

For digital rights management purposes, the RTC includes security features designed to detect unauthorised modifications to the RTC counter.

20.2 RTC CONTROL

The 32-bit RTC counter value, RTC_TIME is held in two 16-bit registers, R16417 (4021h) and R16418 (4022h). The value of RTC_TIME is incremented by the WM8311 once per second. On initial power-up (from the NO POWER state), these registers will be initialised to default values. Once either of these registers has been written to, the RTC_VALID bit is set to indicate that the RTC_TIME registers contain valid data.

When RTC registers are updated, the RTC_SYNC_BUSY bit indicates that the RTC is busy. The RTC registers should not be written to when RTC_SYNC_BUSY = 1.

The RTC_WR_CNT field is provided as a security feature for the RTC. After initialisation, this field is updated on every write to R16417 (4021h) or to R16418 (4022h). This enables the host processor to detect unauthorised modifications to the RTC counter value. See Section 20.4 for more details.

For additional security, the WM8311 does not allow the RTC to be updated more than 8 times in a one-hour period. Additional write attempts will be ignored.

The RTC Alarm time is held in registers R16419 (4023h) and R16420 (4024h). The Alarm function is enabled when RTC_ALM_ENA is set. When the Alarm is enabled, and the RTC counter matches the Alarm time, the RTC Alarm Interrupt is triggered, as described in Section 20.3.

If the RTC Alarm occurs in the SLEEP power state, then a WAKE transition request is generated. If the RTC Alarm occurs in the OFF power state, then an ON transition request is generated. See Section 11.3 for details.

When updating the RTC Alarm time, it is recommended to disable the Alarm first, by setting RTC_ALM_ENA = 0. The RTC Alarm registers should not be written to when RTC_SYNC_BUSY = 1.

The RTC has a frequency trim feature to allow compensation for known and constant errors in the crystal oscillator frequency up to ±8Hz. The RTC_TRIM field is a 10-bit fixed point 2's complement number. MSB scaling = -8Hz. To compensate for errors in the clock frequency, this register should be set to the error (in Hz) with respect to the ideal (32768Hz) of the input crystal frequency.

For example, if the actual crystal frequency = 32769.00Hz, then the frequency error = +1Hz. The value of RTC_TRIM in this case is 0001_000000.

For example, if the actual crystal frequency = 32763.78Hz, then the frequency error = -4.218750Hz. The value of RTC_TRIM in this case is 1011_110010.

Note that the RTC_TRIM control register is locked by the WM8311 User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16416 (4020h) RTC Write Counter	15:0	RTC_WR_CNT	0000h	RTC Write Counter. This random number is updated on every write to the RTC_TIME registers.
R16417 (4021h) RTC Time 1	15:0	RTC_TIME [31:16]	0000h	RTC Seconds counter (MSW) RTC_TIME increments by 1 every second. This is the 16 MSBs.
R16418 (4022h) RTC Time 2	15:0	RTC_TIME [15:0]	0000h	RTC Seconds counter (LSW) RTC_TIME increments by 1 every second. This is the 16 LSBs.
R16419 (4023h) RTC Alarm 1	15:0	RTC_ALM [31:16]	0000h	RTC Alarm time (MSW) 16 MSBs of RTC_ALM
R16420 (4024h) RTC Alarm 2	15:0	RTC_ALM [15:0]	0000h	RTC Alarm time (LSW) 16 LSBs of RTC_ALM
R16421 (4025h) RTC Control	15	RTC_VALID	0	RTC Valid status 0 = RTC_TIME has not been set since Power On Reset 1 = RTC_TIME has been written to since Power On Reset
	14	RTC_SYNC_BUSY	0	RTC Busy status 0 = Normal 1 = Busy The RTC registers should not be written to when RTC_SYNC_BUSY = 1.
	10	RTC_ALM_ENA	0	RTC Alarm Enable 0 = Disabled 1 = Enabled
R16422 (4026h) RTC Trim	9:0	RTC_TRIM	000h	RTC frequency trim. Value is a 10bit fixed point <4,6> 2’s complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. *Protected by user key*

Table 74 Real Time Clock (RTC) Control

20.3 RTC INTERRUPTS

The Real Time Clock (RTC) is associated with two Interrupt event flags.

The RTC_PER_EINT interrupt is set each time a periodic timeout occurs. The periodic timeout is configured using the RTC_PINT_FREQ field described in Table 76.

The RTC_ALM_EINT interrupt is set when the RTC Alarm is triggered. The RTC Alarm time is configured as described in Section 20.2.

Each of these secondary interrupts triggers a primary Real Time Clock Interrupt, RTC_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 75.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	3	RTC_PER_EINT	RTC Periodic interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	2	RTC_ALM_EINT	RTC Alarm interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	3	IM_RTC_PER_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	2	IM_RTC_ALM_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 75 Real Time Clock (RTC) Interrupts

The frequency of the RTC periodic interrupts is set by the RTC_PINT_FREQ field, as described in Table 76.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16421 (4025h) RTC Control	6:4	RTC_PINT_FREQ [2:0]	000	RTC Periodic Interrupt timeout period 000 = Disabled 001 = 2s 010 = 4s 011 = 8s 100 = 16s 101 = 32s 110 = 64s 111 = 128s

Table 76 Real Time Clock (RTC) Periodic Interrupt Control

20.4 DIGITAL RIGHTS MANAGEMENT

The Real Time Clock (RTC) maintains a continuous record of the time; this is maintained at all times, including when the WM8311 is powered down and the RTC function is maintained by the backup supply.

It is highly desirable to be able to write to the RTC counter in order to configure it for logical translation into hours/minutes and to support calendar functions. However, for digital rights management purposes, it is important that malicious modification of the RTC is either prevented or detected.

The security measure implemented on the WM8311 is the RTC Write Counter. This register is initialised to 0000h during Power On Reset, and is updated automatically whenever a Write operation is scheduled on either of the RTC_TIME registers. Note that, when the RTC Write Counter is updated, the new value is generated at random; it is not a sequential counter.

It is assumed that legitimate updates to the RTC_TIME are only those initiated by the Application Processor (AP). When the AP makes an update to the RTC_TIME, the AP can also read the new value of the RTC Write Counter, and should store the value in non-volatile memory. If the AP detects a change in value of the RTC Write Counter, and this was not caused by the AP itself writing to the RTC_TIME, this means that an unauthorised write to the RTC_TIME registers has occurred.

In order to make it difficult for an unauthorised RTC_TIME update to be masked by simply writing to the RTC Write Counter, the RTC_WR_CNT field is generated at random by the WM8311 whenever the RTC_TIME field is updated.

For additional security, the WM8311 does not allow the RTC to be updated more than 8 times in a one-hour period. Additional write attempts will be ignored.

The RTC Control registers are described in Table 74.

20.5 BACKUP MODE CLOCKING OPTIONS

The BACKUP state is entered when the available power supplies are below the reset threshold of the device. Typically, this means that USB or Wall supplies are not present and that the main battery is either discharged or removed. Most of the device functions and registers are reset in this state.

The RTC and oscillator and a ‘software scratch’ memory area can be maintained from a backup power source in the BACKUP state. This is provided using a coin cell, super/gold capacitor, or else a standard capacitor, connected to the LDO12VOUT pin via a 22kΩ resistor. See Section 17.6 for further details.

The RTC and oscillator can be disabled in the BACKUP state by setting the XTAL_BKUPENA register bit to 0. This feature may be used to minimise the device power consumption in the BACKUP state. A 22μF capacitor connected to LDO12VOUT can maintain the RTC value, unclocked, for up to 5 minutes in BACKUP if the oscillator is disabled.

The XTAL_BKUPENA register bit is defined in Section 13.1. For more details on backup power, see Section 17.6.

21 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

21.1 GENERAL DESCRIPTION

The WM8311 has 16 general-purpose input/output (GPIO) pins, GPIO1 - GPIO16. These can be configured as inputs or outputs, active high or active low, with optional on-chip pull-up or pull-down resistors. GPIO outputs can either be CMOS driven or Open Drain configuration. Each GPIO pin can be tri-stated and can also be used to trigger Interrupts.

The function of each GPIO pin is selected individually. Different voltage power domains are selectable on a pin by pin basis for GPIOs 1-12. Input de-bounce is automatically implemented on selected GPIO functions.

21.2 GPIO FUNCTIONS

The list of GPIO functions supported by the WM8311 is contained in Table 77 (for input functions) and Table 78 (for output functions). The input functions are selected when the respective GP*n*_DIR register bit is 1. The output functions are selected when the respective GP*n*_DIR register bit is 0.

The selected function for each GPIO pin is selected by writing to the respective GP*n*_FN register bits. All functions are available on all GPIO pins. The polarity of each input or output GPIO function can be selected using the applicable GP*n*_POL register bit.

The available power domains for each pin are specific to different GPIOs.

The de-bounce time for the GPIO input functions is determined by the GPn_FN field. Some of the input functions allow a choice of de-bounce times, as detailed in Table 77.

The register controls for configuring the GPIO pins are defined in Section 21.3.

GPn_FN	GPIO INPUT FUNCTION	DESCRIPTION	DE-BOUNCE TIME
0h	GPIO	GPIO input. Logic level is read from the GPn_LVL register bits. See Section 21.3.	32μs to 64μs
1h			4ms to 8ms
2h	ON/OFF Request	Control input for requesting an ON/OFF state transition. See Section 11.3. Under default polarity (GPn_POL=1), a rising edge requests the ON state and a falling edge requests the OFF state.	32ms 64ms
3h	SLEEP/WAKE Request	Control input for requesting a SLEEP/WAKE state transition. See Section 11.3. Under default polarity (GPn_POL=1), a rising edge requests the SLEEP state and a falling edge requests the WAKE transition to the ON state.	32μs to 64μs
4h			32ms to 64ms
5h	SLEEP Request	Control input for requesting a SLEEP state transition. See Section 11.3. Under default polarity (GPn_POL=1), a rising edge requests the SLEEP state and a falling edge has no effect.	32μs to 64μs
6h	ON Request	Control input for requesting an ON state transition. See Section 11.3. Under default polarity (GPn_POL=1), a rising edge requests the ON state and a falling edge has no effect.	32μs to 64μs
7h	Watchdog Reset	Control input for resetting the Watchdog Timer. See Section 25.	32μs to 64μs
8h	Hardware DVS control 1	Control input for selecting the DVS output voltage in one or more DC-DC Converters. See Section 15.6.	None

GPn_FN	GPIO INPUT FUNCTION	DESCRIPTION	DE-BOUNCE TIME
9h	Hardware DVS control 2	Control input for selecting the DVS output voltage in one or more DC-DC Converters. See Section 15.6.	None
Ah	Hardware Enable 1	Control input for enabling one or more DC-DC Converters and LDO Regulators. See Section 15.	32μs to 64μs
Bh	Hardware Enable 2	Control input for enabling one or more DC-DC Converters and LDO Regulators. See Section 15.	32μs to 64μs
Ch	Hardware Control input 1	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32μs to 64μs
Dh	Hardware Control input 2	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32μs to 64μs
Eh	Hardware Control input 1	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32ms to 64ms
Fh	Hardware Control input 2	Control input for selecting the operating mode and/or output voltage of one or more DC-DC Converters and LDO Regulators. See Section 15.	32ms to 64ms

Table 77 List of GPIO Input Functions

Further details of the GPIO input de-bounce time are noted in Section 21.3.

GPn_FN	GPIO OUTPUT FUNCTION	DESCRIPTION
0h	GPIO	GPIO output. Logic level is set by writing to the GPn_LVL register bits. See Section 21.3.
1h	Oscillator clock	32.768kHz clock output. See Section 13.
2h	ON state	Logic output indicating that the WM8311 is in the ON state. See Section 11.5.
3h	SLEEP state	Logic output indicating that the WM8311 is in the SLEEP state. See Section 11.5.
4h	Power State Change	Logic output asserted whenever a Power On Reset, or an ON, OFF, SLEEP or WAKE transition has completed. Under default polarity (GP*n*_POL=1), the logic level is the same as the PS_INT interrupt status flag. Note that, if any of the associated Secondary interrupts is masked, then the respective event will not affect the Power State Change GPIO output. See Section 11.2 and Section 11.4.
6h	Touch Panel PenDown detected	Logic output indicating that a PenDown event has occurred. See Section 19.
7h	Touch Panel Conversion Complete	Logic output indicating that a touch panel AUXADC conversion has completed. See Section 19.
8h	DC-DC1 DVS Done	Logic output indicating that DC-DC1 buck converter DVS slew has been completed. This signal is temporarily de-asserted during voltage transitions (including non-DVS transitions). See Section 15.6.

GPn_FN	GPIO OUTPUT FUNCTION	DESCRIPTION
9h	DC-DC2 DVS Done	Logic output indicating that DC-DC1 buck converter DVS slew has been completed. This signal is temporarily de-asserted during voltage transitions (including non-DVS transitions). See Section 15.6.
Ah	External Power Enable 1	Logic output assigned to one of the timeslots in the ON/OFF and SLEEP/WAKE sequences. This can be used for sequenced control of external circuits. See Section 15.3.
Bh	External Power Enable 2	Logic output assigned to one of the timeslots in the ON/OFF and SLEEP/WAKE sequences. This can be used for sequenced control of external circuits. See Section 15.3.
Ch	System Supply Good (SYSVDD Good)	Logic output from SYSVDD monitoring circuit. This function represents the internal SYSOK signal. See Section 24.4.
Dh	Converter Power Good (PWR_GOOD)	Status output indicating that all selected DC-DC Converters and LDO Regulators are operating correctly. Only asserted in ON and SLEEP modes. See Section 15.14.
Eh	External Power Clock	2MHz clock output suitable for clocking external DC-DC Converters. This clock signal is synchronized with the WM8311 DC-DC Converters clocking signal. See Section 13. This clock output is only enabled when either of the External Power Enable signals (EPE1 or EPE2) is asserted. These signals can be assigned to one of the timeslots in the ON/OFF and SLEEP/WAKE sequences. See Section 15.3.
Fh	Auxiliary Reset	Logic output indicating a Reset condition. This signal is asserted in the OFF state. The status in SLEEP mode is configurable. See Section 11.7. Note that the default polarity for this function (GP*n*_POL=1) is "Active High". Setting GP*n*_POL=0 will select "Active Low" function.

Table 78 List of GPIO Output Functions

21.3 CONFIGURING GPIO PINS

The GPIO pins are configured using the Resister fields defined in Table 79.

The function of each GPIO is selected using the GPn_FN register field. The pin direction field GPn_DIR selects between input functions and output functions. See Section 21.2 for a summary of the available GPIO functions.

The polarity of each GPIO can be configured using the GPn_POL bits. This inversion is effective both on GPIO inputs and outputs. When GPn_POL = 1, the non-inverted 'Active High' polarity applies. The opposite logic can be selected by setting GPn_POL = 0.

The voltage power domain of GPIOs 1-12 is determined by the GPn_PWR_DOM register. Note that the available options vary between different GPIO pins, as described in Table 81.

A GPIO output may be either CMOS driven or Open Drain. This is selected using the GPn_OD bits.

Internal pull-up or pull-down resistors can be enabled on each pin using the GPn_PULL field. Both resistors are available for use when the associated GPIO is an input. When the GPIO pin is configured as an Open Drain output, the internal pull-up resistor may be required if no external pull-up resistors are present.

The GPIO pins may be enabled or tri-stated using the GPn_ENA register field. When GPn_ENA = 0, the respective pin is tri-stated. A tri-stated pin exhibits high impedance to any external circuit and is disconnected from the internal GPIO circuits. The pull-up and pull-down resistors are disabled when a GPIO pin is tri-stated.

GPIO pins can generate an interrupt (see Section 21.4). The GP*n*_INT_MODE field selects whether the interrupt occurs on a single edge only, or else on both rising and falling edges. When single edge is selected, the active edge is the rising edge (when GPn_POL = 1) or the falling edge (when GPn_POL = 0).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16440 (4038h) to R16455 (4047h)	15	GPn_DIR	1	GPIO*n* pin direction 0 = Output 1 = Input
	14:13	GPn_PULL [1:0]	01	GPIO*n* Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved
	12	GPn_INT_MODE	0	GPIO*n* Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP*n*_POL=1) or falling edge triggered (if GP*n*_POL =0) 1 = GPIO interrupt is triggered on rising and falling edges
	11	GPn_PWR_DOM	0	GPIO*n* Power Domain See Table 81.
	10	GPn_POL	1	GPIO*n* Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)
	9	GPn_OD	0	GPIO*n* Output pin configuration 0 = CMOS 1 = Open Drain
	7	GPn_ENA	0	GPIO*n* Enable control 0 = GPIO pin is tri-stated 1 = Normal operation
	3:0	GP*n*_FN [3:0]	0000	GPIO*n* Pin Function See Table 82.
Note: *n* is a number between 1 and 16 that identifies the individual GPIO. **Note:** The default values noted are valid when the WM8311 powers up to the OFF state, or if the Register Map is reset following a Device Reset or Software Reset event. In the case of GPIO pins 1 to 6, these registers are overwritten with the respective ICE or OTP memory contents when an ON transition is scheduled.				

Table 79 GPIO Pin Configuration

When the GPIO output function is selected (GPn_FN = 0h, GPn_DIR = 0), the state of a GPIO output is controlled by writing to the corresponding GP*n*_LVL register bit, as defined in Table 80.

The logic level of a GPIO input is determined by reading the corresponding GP*n*_LVL register bit. If GPn_POL is set, then the read value of the GPn_LVL field for a GPIO input is the inverse of the external signal. Note that, when the GPIO input level changes, the logic level of GPn_LVL will only be updated after the maximum de-bounce period, as listed in Table 77. An input pulse that is shorter than the minimum de-bounce period will be filtered by the de-bounce function and will be ignored.

If a GPIO is configured as a CMOS output (ie. GPn_OD = 0), then the read value of the GPn_LVL field will indicate the logic level of that output. If GP*n*_POL is set, then the read value of the GP*n*_LVL field for a GPIO output is the inverse of the level on the external pad.

If a GPIO is configured as an Open Drain output, then the read value of GPn_LVL is only valid when the internal pull-up resistor is enabled on the pin (ie. when GPn_PULL = 10). The read value is also affected by the GPn_POL bit, as described above for the CMOS case.

If a GPIO is tri-stated (GP*n*_ENA = 0), then the read value of the corresponding GPn_LVL field is invalid.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16396 (400Ch) GPIO Level	15	GP16_LVL	0	GPIO*n* level. When GP*n*_FN = 0h and GP*n*_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP*n*_POL is 0, the register contains the opposite logic level to the external pin.
	14	GP15_LVL	0	
	13	GP14_LVL	0	
	12	GP13_LVL	0	
	11	GP12_LVL	0	
	10	GP11_LVL	0	
	9	GP10_LVL	0	
	8	GP9_LVL	0	
	7	GP8_LVL	0	
	6	GP7_LVL	0	
	5	GP6_LVL	0	
	4	GP5_LVL	0	
	3	GP4_LVL	0	
	2	GP3_LVL	0	
	1	GP2_LVL	0	
	0	GP1_LVL	0	

Table 80 GPIO Level Register

The power domain for each GPIO is controlled using the GPn_PWR_DOM registers as described in Table 81. The power domain for GPIO13 - GPIO16 is fixed; these pins are referenced to TPVDD.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16440 (4038h) GPIO1 Control	11	GP1_PWR_DOM	0	GPIO1 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16441 (4039h) GPIO2 Control	11	GP2_PWR_DOM	0	GPIO2 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16442 (403Ah) GPIO3 Control	11	GP3_PWR_DOM	0	GPIO3 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16443 (403Bh) GPIO4 Control	11	GP4_PWR_DOM	0	GPIO4 Power Domain select 0 = DBVDD 1 = SYSVDD
R16444 (403Ch) GPIO5 Control	11	GP5_PWR_DOM	0	GPIO5 Power Domain select 0 = DBVDD 1 = SYSVDD
R16445 (403Dh) GPIO6 Control	11	GP6_PWR_DOM	0	GPIO6 Power Domain select 0 = DBVDD 1 = SYSVDD
R16446 (403Eh) GPIO7 Control	11	GP7_PWR_DOM	0	GPIO7 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16447 (403Fh) GPIO8 Control	11	GP8_PWR_DOM	0	GPIO8 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)
R16448 (4040h) GPIO9 Control	11	GP9_PWR_DOM	0	GPIO9 Power Domain select 0 = DBVDD 1 = VPMIC (LDO12)

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16449 (4041h) GPIO10 Control	11	GP10_PWR_DOM	0	GPIO10 Power Domain select 0 = DBVDD 1 = SYSVDD
R16450 (4042h) GPIO11 Control	11	GP11_PWR_DOM	0	GPIO11 Power Domain select 0 = DBVDD 1 = SYSVDD
R16451 (4043h) GPIO12 Control	11	GP12_PWR_DOM	0	GPIO12 Power Domain select 0 = DBVDD 1 = SYSVDD

Table 81 GPIO Power Domain Registers

The function of each GPIO is controlled using the GPn_FN registers defined in Table 82. Note that the selected function also depends on the associated GPn_DIR field described in Table 79.

See also Section 21.2 for additional details of each GPIO function, including the applicable de-bounce times for GPIO input functions.

The Touch Panel controller must be disabled if using GPIO13 to GPIO16 as GPIO functions. Note that, when the Touch Panel controller is enabled, GPIO13 to GPIO16 must be tri-stated using the GPn_ENA register bits (see Table 79).

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16440 (4038h) GPIO1 Control	3:0	GP1_FN [3:0]	0000	Input functions: 0h = GPIO input (long de-bounce) 1h = GPIO input 2h = Power On/Off request 3h = Sleep/Wake request 4h = Sleep/Wake request (long de-bounce) 5h = Sleep request 6h = Power On request 7h = Watchdog Reset input 8h = DVS1 input 9h = DVS2 input Ah = HW Enable1 input Bh = HW Enable2 input Ch = HW Control1 input Dh = HW Control2 input Eh = HW Control1 input (long de-bounce) Fh = HW Control2 input (long de-bounce) Output functions: 0h = GPIO output 1h = 32.768kHz oscillator output 2h = ON state 3h = SLEEP state 4h = Power State Change 5h = Reserved 6h = Touch Panel Pen Down 7h = Touch Panel Conversion complete
R16441 (4039h) GPIO2 Control	3:0	GP2_FN [3:0]	0000	
R16442 (403Ah) GPIO3 Control	3:0	GP3_FN [3:0]	0000	
R16443 (403Bh) GPIO4 Control	3:0	GP4_FN [3:0]	0000	
R16444 (403Ch) GPIO5 Control	3:0	GP5_FN [3:0]	0000	
R16445 (403Dh) GPIO6 Control	3:0	GP6_FN [3:0]	0000	
R16446 (403Eh) GPIO7 Control	3:0	GP7_FN [3:0]	0000	
R16447 (403Fh) GPIO8 Control	3:0	GP8_FN [3:0]	0000	
R16448 (4040h) GPIO9 Control	3:0	GP9_FN [3:0]	0000	
R16449 (4041h) GPIO10 Control	3:0	GP10_FN [3:0]	0000	
R16450	3:0	GP11_FN [3:0]	0000	

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
(4042h) GPIO11 Control				8h = DC1 DVS Done 9h = DC2 DVS Done Ah = External Power Enable1 Bh = External Power Enable2 Ch = System Supply Good (SYSOK) Dh = Converter Power Good (PWR_GOOD) Eh = External Power Clock (2MHz) Fh = Auxiliary Reset
R16451 (4043h) GPIO12 Control	3:0	GP12_FN [3:0]	0000	
R16452 (4044h) GPIO13 Control	3:0	GP13_FN [3:0]	0000	
R16453 (4045h) GPIO14 Control	3:0	GP14_FN [3:0]	0000	
R16454 (4046h) GPIO15 Control	3:0	GP15_FN [3:0]	0000	
R16455 (4047h) GPIO16 Control	3:0	GP16_FN [4:0]	0000	

Table 82 GPIO Function Select Registers

Note that GPIO input functions 2h, 3h, 4h, 5h and 6h are edge-triggered only. The associated state transition(s) are scheduled only when a rising or falling edge is detected on the respective GPIO pin. At other times, it is possible that other state transition events may cause a state transition regardless of the state of the GPIO input. See Section 11.3 for details of all the state transition events.

Note that SLEEP transitions are not possible when any of the Battery Charger Interrupts is set. If any of the Battery Charger Interrupts is asserted when a SLEEP transition is requested, then the transition will be unsuccessful and the WM8311 will remain in the ON power state. See Section 17.7.8 for details of the Battery Charger Interrupts.

21.4 GPIO INTERRUPTS

Each GPIO pin has an associated interrupt flag, GP*n*_EINT, in Register R16405 (4015h). Each of these secondary interrupts triggers a primary GPIO Interrupt, GP_INT (see Section 23). This can be masked by setting the mask bit(s) as described in Table 83.

See Section 28 and Section 29 for a definition of the register bit positions applicable to each GPIO.

ADDRESS	BIT	LABEL	DESCRIPTION
R16405 (4015h) Interrupt Status 5	15:0	GP*n*_EINT	GPIO interrupt. (Trigger is controlled by GP*n*_INT_MODE) Note: Cleared when a ‘1’ is written.
R16413 (401Dh) Interrupt Status 5 Mask	15:0	IM_GP*n*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Note: *n* is a number between 1 and 16 that identifies the individual GPIO.			

Table 83 GPIO Interrupts

22 SYSTEM STATUS LED DRIVERS

22.1 GENERAL DESCRIPTION

The WM8311 provides two System Status LED Drivers. These are digital outputs intended for driving LEDs directly. The LED outputs can be assigned to indicate OTP Program status, Power State status or Battery Charger status. They can also be commanded directly via register control, in order to provide any other required functionality.

22.2 LED DRIVER CONTROL

LED Drivers are configurable in the ON and SLEEP power states only. The functionality of the LED Drivers is controlled by the LEDn_SRC register bits, as described in Table 84.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16460 (404Ch) Status LED1	15:14	LED1_SRC [1:0]	11	LED1 Source (Selects the LED1 function.) 00 = Off 01 = Power State Status 10 = Charger Status 11 = Manual Mode Note - LED1 also indicates completion of OTP Auto Program
R16461 (404Dh) Status LED2	15:14	LED2_SRC [1:0]	11	LED2 Source (Selects the LED2 function.) 00 = Off 01 = Power State Status 10 = Charger Status 11 = Manual Mode Note - LED2 also indicates an OTP Auto Program Error condition

Table 84 System Status LED Control

22.2.1 OTP PROGRAM STATUS

The LED drivers indicate the status of the OTP Auto Program function, where the contents of the external InstantConfig™ (ICE) memory are automatically programmed into the OTP. See Section 14.6.3 for further details of the OTP Auto Program function.

When the OTP Auto Program function is executed, the System Status LED drivers follow the functionality defined in Table 85.

LED DRIVER	DESCRIPTION	DRIVE MODE	LED 'ON' TIME	ON:OFF DUTY CYCLE
LED1	OTP Auto Program Complete	Constant	n/a	n/a
LED2	OTP Auto Progam Error	Constant	n/a	n/a

Table 85 System Status LED Outputs - OTP Program Status

The OTP Program Status LED outputs will continue until a Device Reset.

Note that the OTP Program Status is always indicated via the LED outputs, regardless of the LEDn_SRC register fields.

22.2.2 POWER STATE STATUS

Setting LEDn_SRC = 01 configures the associated LED to indicate Power State status. Under this selection, four different conditions may be indicated, as defined in Table 86.

LED DRIVER	DESCRIPTION	DRIVE MODE	LED 'ON' TIME	ON:OFF DUTY CYCLE
LED1 or LED2	Power Sequence Failure	Pulsed sequence (4 pulses)	1s	1:1
	SYSVDD Low	Continuous pulsed	250ms	1:3
	ON state	Constant	n/a	n/a
	SLEEP state	Continuous pulsed	250ms	1:7

Table 86 System Status LED Outputs - Power State Status

If more than one of the conditions listed occurs simultaneously, then the LED output pattern is controlled by the condition in the highest position within the list above.

For example, if the SYSVDD Low condition occurs while in the ON or SLEEP states, then the LED output follows the pattern defined for the SYSVDD Low condition.

The SYSVDD Low indication is asserted if SYSVDD is less than the user-selectable threshold SYSLO_THR, as described in Section 24.4.

Note that, in the case of Power Sequence Failure, the transition to OFF occurs after the 4 LED pulses have been emitted.

22.2.3 CHARGER STATUS

Setting LEDn_SRC = 10 configures the associated LED to indicate Battery Charger status. Under this selection, two different conditions may be indicated, as defined in Table 87.

LED DRIVER	DESCRIPTION	DRIVE MODE	LED 'ON' TIME	ON:OFF DUTY CYCLE
LED1 or LED2	Charger Complete	Constant	n/a	n/a
	Charger On	Continuous pulsed	1s	1:2

Table 87 System Status LED Outputs - Charger Status

22.2.4 MANUAL MODE

Setting LEDn_SRC = 11 configures the associated LED to operate in Manual Mode, which is further configurable using additional register fields.

In Manual Mode, the LED output can be commanded as Off, On (Constant), Continuous Pulsed or Pulsed Sequence. The selected operation is determined by the LEDn_MODE registers as described in Table 88.

In Continuous Pulsed mode and Pulsed Sequence mode, the 'On' time and the Duty Cycle can be configured using the LEDn_DUR and LEDn_DUTY_CYC registers respectively.

In Pulsed Sequence mode, the number of pulses in the sequence can be selected using the LEDn_SEQ_LEN register. On completion of the commanded number of pulses, the LED remains off until LEDn_MODE or LEDn_SRC is changed to another value.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16460 (404Ch) Status LED1	9:8	LED1_MODE [1:0]	00	LED1 Mode (Controls LED1 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence
	5:4	LED1_SEQ_LEN [1:0]	10	LED1 Pulse Sequence Length (when LED1_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses
	3:2	LED1_DUR [1:0]	01	LED1 On time (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms
	1:0	LED1_DUTY_CYC [1:0]	10	LED1 Duty Cycle (On:Off ratio) (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2:(33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)
R16461 (404Dh) Status LED2	9:8	LED2_MODE [1:0]	00	LED2 Mode (Controls LED2 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence
	5:4	LED2_SEQ_LEN [1:0]	10	LED2 Pulse Sequence Length (when LED2_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:2	LED2_DUR [1:0]	01	LED2 On time (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms
	1:0	LED2_DUTY_CYC [1:0]	10	LED2 Duty Cycle (On:Off ratio) (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2:(33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)

Table 88 System Status LED Outputs - Manual Mode Control

22.3 LED DRIVER CONNECTIONS

The recommended connection for System Status LEDs is illustrated in Figure 35. The LED outputs are referenced to the SYSVDD power domain. A series resistor may be required, depending on the LED characteristics and the SYSVDD voltage.

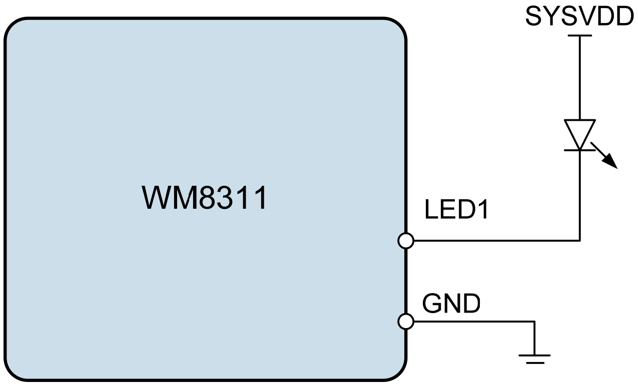


Figure 35 System Status LED Connections

23 INTERRUPT CONTROLLER

The WM8311 has a comprehensive Interrupt logic capability. The dedicated $\overline{\text{IRQ}}$ pin can be used to alert a host processor to selected events or fault conditions. Each of the interrupt conditions can be individually enabled or masked. Following an interrupt event, the host processor should read the interrupt registers in order to determine what caused the interrupt, and take appropriate action if required.

The WM8311 interrupt controller has two levels:

Secondary interrupts indicate a single event in one of the circuit blocks. The event is indicated by setting a register bit. This bit is a latching bit - once it is set, it remains at logic 1 even if the trigger condition is cleared. The secondary interrupts are cleared by writing a logic 1 to the relevant register bit. Note that reading the register does not clear the secondary interrupt.

Primary interrupts are the logical OR of the associated secondary interrupts (usually all the interrupts associated with one particular circuit block). Each of the secondary interrupts can be individually masked or enabled as an input to the corresponding primary interrupt. The primary interrupt register R16400 (4010h) is read-only.

The status of the $\overline{\text{IRQ}}$ pin reflects the logical NOR of the primary interrupts. A logic 0 indicates that one or more of the primary interrupts is asserted. Each of the primary interrupts can be individually masked or enabled as an input to the $\overline{\text{IRQ}}$ pin output.

The $\overline{\text{IRQ}}$ pin output can either be CMOS driven or Open Drain (integrated pull-up) configuration, as determined by the IRQ_OD register bit. When the $\overline{\text{IRQ}}$ pin is Open Drain, it is actively driven low when asserted; the pull-up causes a logic high output when not asserted. The Open Drain configuration enables multiple devices to share a common Interrupt line with the host processor.

The $\overline{\text{IRQ}}$ pin output can be masked by setting the IM_IRQ register bit. When the $\overline{\text{IRQ}}$ pin is masked, it is held in the logic 1 (or Open Drain) state regardless of any internal interrupt event.

Note that the secondary interrupt bits are always valid - they are set as normal, regardless of whether the bit is enabled or masked as an input to the corresponding primary interrupt. The primary interrupt bits are set and cleared as normal in response to any unmasked secondary interrupt, regardless of whether the primary interrupt bit is enabled or masked as an input to the $\overline{\text{IRQ}}$ pin output.

Note also that if any internal condition is configured to trigger an event other than an Interrupt (eg. the Watchdog timer triggers Reset), these events are always actioned, regardless of the state of any interrupt mask bits.

The $\overline{\text{IRQ}}$ pin output is configured using the register bits described in Table 89.

ADDRESS	BIT	LABEL	DESCRIPTION
R16407 (4017h) IRQ Config	1	IRQ_OD	IRQ pin configuration 0 = CMOS 1 = Open Drain (integrated pull-up)
	0	IM_IRQ	IRQ pin output mask 0 = Normal 1 = IRQ output is masked

Table 89 IRQ Pin Configuration

The interrupt logic is illustrated in Figure 36.

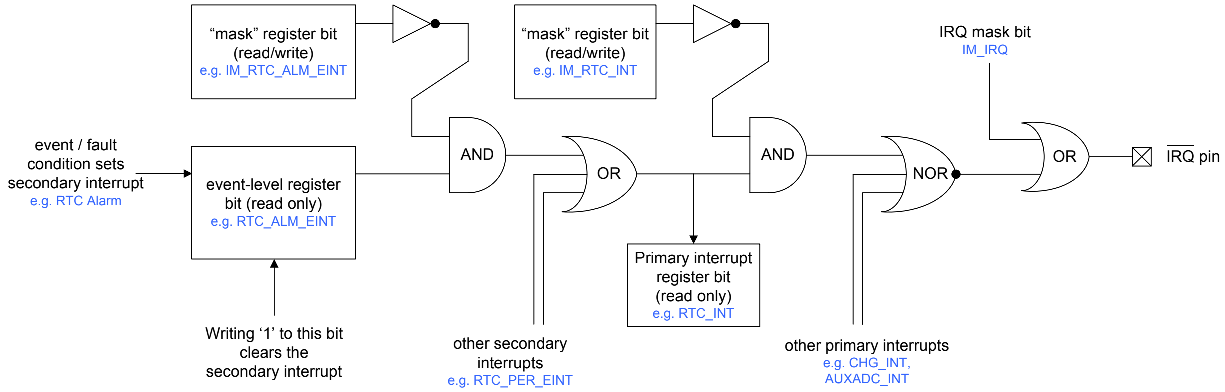


Figure 36 Interrupt Logic

Following the assertion of the $\overline{\text{IRQ}}$ pin to indicate an Interrupt event, the host processor can determine which primary interrupt caused the event by reading the primary interrupt register R16400 (4010h). This register is defined in Section 23.1.

After reading the primary interrupt register, the host processor must read the corresponding secondary interrupt register(s) in order to determine which specific event caused the $\overline{\text{IRQ}}$ pin to be asserted. The host processor clears the secondary interrupt bit by writing a logic 1 to that bit.

23.1 PRIMARY INTERRUPTS

The primary interrupts are defined in Table 90. These bits are Read Only. They are set when any of the associated unmasked secondary interrupts is set. They can only be reset when all of the associated secondary resets are cleared or masked.

Each primary interrupt can be masked. When a mask bit is set, the corresponding primary interrupt is masked and does not cause the $\overline{\text{IRQ}}$ pin to be asserted. The primary interrupt bits in R16408 (4018h) are valid regardless of whether the mask bit is set. The primary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16400 (4010h) System Interrupts	15	PS_INT	Power State primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	14	TEMP_INT	Thermal primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	13	GP_INT	GPIO primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	12	ON_PIN_INT	ON Pin primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	11	WDOG_INT	Watchdog primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	10	TCHDATA_INT	Touch Panel Data primary interrupt 0 = No interrupt 1 = Interrupt is asserted

ADDRESS	BIT	LABEL	DESCRIPTION
	9	TCHPD_INT	Touch Panel Pen Down primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	8	AUXADC_INT	AUXADC primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	7	PPM_INT	Power Path Management primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	6	CS_INT	Current Sink primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	5	RTC_INT	Real Time Clock primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	4	OTP_INT	OTP Memory primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	2	CHG_INT	Battery Charger primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	1	HC_INT	High Current primary interrupt 0 = No interrupt 1 = Interrupt is asserted
	0	UV_INT	Undervoltage primary interrupt 0 = No interrupt 1 = Interrupt is asserted
R16408 (4018h) System Interrupts Mask	15	IM_PS_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	14	IM_TEMP_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	13	IM_GP_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	12	IM_ON_PIN_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	11	IM_WDOG_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	10	IM_TCHDATA_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	9	IM_TCHPD_INT	Interrupt mask. 0 = Do not mask interrupt.

ADDRESS	BIT	LABEL	DESCRIPTION
			1 = Mask interrupt. Default value is 1 (masked)
	8	IM_AUXADC_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	7	IM_PPM_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	6	IM_CS_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	5	IM_RTC_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	4	IM_OTP_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	2	IM_CHG_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_HC_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_UV_INT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 90 Primary Interrupt Status and Mask Bits

23.2 SECONDARY INTERRUPTS

The following sections define the secondary interrupt status and control bits associated with each of the primary interrupt bits defined in Table 90.

23.2.1 POWER STATE INTERRUPT

The primary PS_INT interrupt comprises three secondary interrupts as described in Section 11.4. The secondary interrupt bits are defined in Table 91.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a PS_INT interrupt. The secondary interrupt bits in R16402 (4012h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	2	PS_POR_EINT	Power On Reset interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	1	PS_SLEEP_OFF_EINT	SLEEP or OFF interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
	0	PS_ON_WAKE_EINT	ON or WAKE interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.
R16410 (401Ah) Interrupt Status 2 Mask	2	IM_PS_POR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	1	IM_PS_SLEEP_OFF_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	0	IM_PS_ON_WAKE_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 91 Power State Interrupts

23.2.2 THERMAL INTERRUPTS

The primary TEMP_INT interrupt comprises a single secondary interrupt as described in Section 26. The secondary interrupt bit is defined in Table 92.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger a TEMP_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	1	TEMP_THW_CINT	Thermal Warning interrupt (Rising and Falling Edge triggered) Note: Cleared when a '1' is written.
R16410 (4019h) Interrupt Status 1 Mask	1	IM_TEMP_THW_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 92 Thermal Interrupts

23.2.3 GPIO INTERRUPTS

The primary GP_INT interrupt comprises sixteen secondary interrupts as described in Section 21.4. The secondary interrupt bits are defined in Table 93.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a GP_INT interrupt. The secondary interrupt bits in R16405 (4015h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16405 (4015h) Interrupt Status 5	15:0	GP*n*_EINT	GPIO interrupt. (Trigger is controlled by GP*n*_INT_MODE) Note: Cleared when a ‘1’ is written.
R16413 (401Dh) Interrupt Status 5 Mask	15:0	IM_GP*n*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Note: *n* is a number between 1 and 16 that identifies the individual GPIO.			

Table 93 GPIO Interrupts

23.2.4 ON PIN INTERRUPTS

The primary ON_PIN_INT interrupt comprises a single secondary interrupt as described in Section 11.6. The secondary interrupt bit is defined in Table 94.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger an ON_PIN_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	12	ON_PIN_CINT	ON pin interrupt. (Rising and Falling Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	12	IM_ON_PIN_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 94 ON Pin Interrupt

23.2.5 WATCHDOG INTERRUPTS

The primary WDOG_INT interrupt comprises a single secondary interrupt as described in Section 25. The secondary interrupt bits are defined in Table 95.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger a WDOG_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	11	WDOG_TO_EINT	Watchdog timeout interrupt. (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	11	IM_WDOG_TO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 95 Watchdog Timer Interrupts

23.2.6 TOUCH PANEL DATA INTERRUPTS

The primary TCHDATA_INT interrupt comprises a single secondary interrupt as described in Section 19.5. The secondary interrupt bits are defined in Table 96.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger a TCHDATA_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	10	TCHDATA_EINT	Touch panel Data interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	10	IM_TCHDATA_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 96 Touch Panel Data Interrupts

23.2.7 TOUCH PANEL PEN DOWN INTERRUPTS

The primary TCHPD_INT interrupt comprises a single secondary interrupt as described in Section 19.5. The secondary interrupt bits are defined in Table 97.

The secondary interrupt can be masked. When the mask bit is set, the corresponding interrupt event is masked and does not trigger a TCHPD_INT interrupt. The secondary interrupt bit in R16401 (4011h) is valid regardless of whether the mask bit is set. The secondary interrupt is masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	9	TCHPD_EINT	Touch panel Pen Down interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	9	IM_TCHPD_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 97 Touch Panel Pen Down Interrupts

23.2.8 AUXADC INTERRUPTS

The primary AUXADC_INT interrupt comprises five secondary interrupts as described in Section 18.5. The secondary interrupt bits are defined in Table 98.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a AUXADC_INT interrupt. The secondary interrupt bits in R16401 (4011h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	8	AUXADC_DATA_EINT	AUXADC Data Ready interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	7:4	AUXADC_DCOMP*n*_EINT	AUXADC Digital Comparator *n* interrupt (Trigger is controlled by DCMP*n*_GT) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	8	IM_AUXADC_DATA_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	7:4	IM_AUXADC_DCOMP*n*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Note: *n* is a number between 1 and 4 that identifies the individual Comparator.			

Table 98 AUXADC Interrupts

23.2.9 POWER PATH MANAGEMENT INTERRUPTS

The primary PPM_INT interrupt comprises three secondary interrupts as described in Section 17.5. The secondary interrupt bits are defined in Table 99.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a PPM_INT interrupt. The secondary interrupt bits in R16401 (4011h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	15	PPM_SYSLO_EINT	Power Path SYSLO interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	14	PPM_PWR_SRC_EINT	Power Path Source interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	13	PPM_USB_CURR_EINT	Power Path USB Current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	15	IM_PPM_SYSLO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	14	IM_PPM_PWR_SRC_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	13	IM_PPM_USB_CURR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 99 Power Path Management Interrupts

23.2.10 CURRENT SINK INTERRUPTS

The primary CS_INT interrupt comprises two secondary interrupts as described in Section 16.3. The secondary interrupt bits are defined in Table 100.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a CS_INT interrupt. The secondary interrupt bits in R16402 (4012h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	7	CS2_EINT	Current Sink 2 interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	6	CS1_EINT	Current Sink 1 interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16410 (401Ah) Interrupt Status 2 Mask	7	IM_CS2_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	6	IM_CS1_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 100 Current Sink Interrupts

23.2.11 REAL TIME CLOCK INTERRUPTS

The primary RTC_INT interrupt comprises two secondary interrupts as described in Section 20.3. The secondary interrupt bits are defined in Table 101.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a RTC_INT interrupt. The secondary interrupt bits in R16401 (4011h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	3	RTC_PER_EINT	RTC Periodic interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	2	RTC_ALM_EINT	RTC Alarm interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	3	IM_RTC_PER_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	2	IM_RTC_ALM_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 101 Real Time Clock (RTC) Interrupts

23.2.12 OTP MEMORY INTERRUPTS

The primary OTP_INT interrupt comprises two secondary interrupts as described in Section 14.5. The secondary interrupt bits are defined in Table 102.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a OTP_INT interrupt. The secondary interrupt bits in R16402 (4012h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	5	OTP_CMD_END_EINT	OTP / ICE Command End interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	4	OTP_ERR_EINT	OTP / ICE Command Fail interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16410 (401Ah) Interrupt Status 2 Mask	5	IM_OTP_CMD_END_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	4	IM_OTP_ERR_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 102 OTP Memory Interrupts

23.2.13 RESERVED

23.2.14 BATTERY CHARGER INTERRUPTS

The primary CHG_INT interrupt comprises six secondary interrupts as described in Section 17.7.8. The secondary interrupt bits are defined in Table 103.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a CHG_INT interrupt. The secondary interrupt bits in R16402 (4012h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16402 (4012h) Interrupt Status 2	15	CHG_BATT_HOT_EINT	Battery Hot interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	14	CHG_BATT_COLD_EINT	Battery Cold interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	13	CHG_BATT_FAIL_EINT	Battery Fail interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	12	CHG_OV_EINT	Battery Overvoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	11	CHG_END_EINT	Battery Charge End interrupt (End of Charge Current threshold reached) (Rising Edge triggered) Note: Cleared when a ‘1’ is written.

ADDRESS	BIT	LABEL	DESCRIPTION
	10	CHG_TO_EINT	Battery Charge Timeout interrupt (Charger Timer has expired) (Rising Edge triggered) Note: Cleared when a '1' is written.
	9	CHG_MODE_EINT	Battery Charge Mode interrupt (Charger Mode has changed) (Rising Edge triggered) Note: Cleared when a '1' is written.
	8	CHG_START_EINT	Battery Charge Start interrupt (Charging has started) (Rising Edge triggered) Note: Cleared when a '1' is written.
R16410 (401Ah) Interrupt Status 2 Mask	15	IM_CHG_BATT_HOT_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	14	IM_CHG_BATT_COLD_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	13	IM_CHG_BATT_FAIL_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	12	IM_CHG_OV_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	11	IM_CHG_END_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	10	IM_CHG_TO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	9	IM_CHG_MODE_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	8	IM_CHG_START_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 103 Battery Charger Interrupts

23.2.15 HIGH CURRENT INTERRUPTS

The primary HC_INT interrupt comprises two secondary interrupts as described in Section 15.13. The secondary interrupt bits are defined in Table 104.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a HC_INT interrupt. The secondary interrupt bits in R16404 (4014h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16404 (4014h) Interrupt Status 4	9	HC_DC2_EINT	DC-DC2 High Current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
	8	HC_DC1_EINT	DC-DC1 High Current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16412 (401Ch) Interrupt Status 4 Mask	9	IM_HC_DC2_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
	8	IM_HC_DC1_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 104 Overcurrent Interrupts

23.2.16 UNDERVOLTAGE INTERRUPTS

The primary UV_INT interrupt comprises fourteen secondary interrupts as described in Section 15.13). The secondary interrupt bits are defined in Table 105.

Each of the secondary interrupts can be masked. When a mask bit is set, the corresponding interrupt event is masked and does not trigger a UV_INT interrupt. The secondary interrupt bits in R16403 (4013h) and R16404 (4014h) are valid regardless of whether the mask bit is set. The secondary interrupts are all masked by default.

ADDRESS	BIT	LABEL	DESCRIPTION
R16403 (4013h) Interrupt Status 3	9:0	UV_LDO*n*_EINT	LDO*n* Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16404 (4014h) Interrupt Status 4	3:0	UV_DC*m*_EINT	DC-DC*m* Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16411 (401Bh) Interrupt Status 3 Mask	9:0	IM_UV_LDO*n*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
R16412 (401Ch) Interrupt Status 4 Mask	3:0	IM_UV_DC*m*_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)
Notes: 1. *n* is a number (1-5, 7) that identifies the individual LDO Regulator. 2. *m* is a number between 1 and 4 that identifies the individual DC-DC Converter.			

Table 105 Undervoltage Interrupts

24 RESETS AND SUPPLY VOLTAGE MONITORING

24.1 RESETS

The WM8311 provides hardware and software monitoring functions as inputs to a Reset management system. These functions enable the device to take appropriate action when power supplies are critically low or if a hardware or software fault condition is detected.

There are different levels of Resets, providing different response mechanisms according to the condition that caused the Reset event. Where applicable, the WM8311 will automatically return to the ON state and resume normal operation as quickly as possible following a Reset.

A System Reset occurs in the event of a Power Sequence Failure, Device overtemperature, SYSVDD undervoltage, Software 'OFF' request or VPMIC (LDO12) undervoltage condition. Under these conditions, the WM8311 asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. In the case of VPMIC undervoltage, the WM8311 enters the BACKUP state. The contents of the Register map are not reset under System Reset conditions.

A Device Reset occurs in the event of a Watchdog Timeout, Hardware Reset request or Converter (LDO or DC-DC) Undervoltage condition. Under these conditions, the WM8311 asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. The contents of the Register map are cleared to default values, except for the RTC and software scratch registers, which are maintained. The WM8311 will automatically return to the ON state after performing the Device Reset.

A Software Reset occurs when any value is written to Register 0000h, as described in Section 12.5. In this event, the WM8311 asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. The Register map contents may or may not be affected, depending on the value of the SW_RESET_CFG field. See Section 24.3 for further details of Software Reset configuration. The WM8311 will automatically return to the ON state after performing the Software Reset.

A Power-On Reset occurs when the supply voltage is less than the Power-On Reset threshold, as described in Section 24.4. In this event, the WM8311 is forced into the NO POWER state, as described in Section 11.2. All the contents of the Register map are lost in the NO POWER state.

A summary of the WM8311 Resets is contained in Table 106.

RESET TYPE	RESET CONDITION	DESCRIPTION	RESPONSE	AUTOMATIC RECOVERY
System Reset	Power Sequence Failure	DC Converters, LDOs or CLKOUT circuits (including FLL) have failed to start up within the permitted time. See Section 11.3.	Assert $\overline{\text{RESET}}$ pin. Select OFF state. If the Reset Condition is VPMIC (LDO12) undervoltage, then the WM8311 enters the BACKUP state.	No
	Device overtemperature	An overtemperature condition has been detected. See Section 26.		No
	SYSVDD undervoltage (1)	SYSVDD is less than the user-selectable threshold SYSLO_THR and SYSLO_ERR_ACT is configured to select OFF in this condition. See Section 24.4.		No
	SYSVDD undervoltage (2)	SYSVDD is less than the SHUTDOWN voltage. See Section 24.4.		No
	Software OFF request	OFF has been commanded by writing CHIP_ON = 0. See Section 11.3		No
	VPMIC (LDO12) undervoltage	The WM8311 supply voltage is less than the System Reset threshold. See Section 24.4.		No
Device Reset	Watchdog timeout	Watchdog timer has expired and the selected response is to generate a Device Reset. See Section 25.	Assert $\overline{\text{RESET}}$ pin. Shutdown and restart the WM8311. Reset Register map (Note the RTC and software scratch registers are not reset.)	Yes
	Hardware Reset	The $\overline{\text{RESET}}$ pin has been pulled low by an external source. See Section 24.2.		Yes
	Converter (LDO or DC-DC) Undervoltage	An undervoltage condition has been detected and the selected response is “Shut down system (Device Reset)” See Section 15.		Yes
Software Reset	Software Reset	Software Reset has been commanded by writing to Register 0000h. See Section 12.5.	Assert $\overline{\text{RESET}}$ pin. Shutdown and restart the WM8311. See Section 24.3 for configurable options regarding the Register Map contents.	Yes
Power On Reset	Power On Reset	The WM8311 supply voltage is less than the Power-On Reset (POR) threshold. See Section 24.4.	The WM8311 is in the NO POWER state. All register contents are lost.	No

Table 106 Resets Summary

In the cases where Automatic Recovery is supported (as noted in Table 106), the WM8311 will re-start the WM8311 following the Reset, and return the device to the ON state. The particular Reset condition which caused the return to the ON state will be indicated in the “ON Source” register - see Section 11.3.

Note that, if a Watchdog timeout or Converter undervoltage fault persists, a maximum of 6 Device Resets will be attempted to initiate the start-up sequence. Similarly, a maximum of 6 Software Resets is permitted. If these limits are exceeded, the WM8311 will remain in the OFF state until the next valid ON state transition event occurs.

The WM8311 asserts the $\overline{\text{RESET}}$ low as soon as the device begins the shutdown sequence. $\overline{\text{RESET}}$ is held low for the duration of the shutdown sequence and is held low in the OFF state. In the cases where Automatic Recovery is supported, $\overline{\text{RESET}}$ is automatically cleared (high) after successful completion of the startup sequence. The duration of the $\overline{\text{RESET}}$ low period after the startup sequence has completed is governed by the RST_DUR register field described in Section 11.7.

24.2 HARDWARE RESET

A Hardware Reset is triggered when an external source pulls the $\overline{\text{RESET}}$ pin low. Under this condition, the WM8311 transitions to the OFF state. The contents of the Register map are cleared to default values, except for the RTC and software scratch registers, which are maintained. The WM8311 will then automatically schedule an ON state transition to resume normal operation.

If the external source continues to pull the $\overline{\text{RESET}}$ pin low, then the WM8311 cannot fully complete the ON state transition following the Hardware Reset. In this case, the WM8311 will mask the external reset for up to 32 seconds. If the $\overline{\text{RESET}}$ pin is released (ie. it returns to logic ‘1’) during this time, then the ON state transition is completed and the Hardware Reset input is valid again from this point. If the $\overline{\text{RESET}}$ pin is not released, then the WM8311 will force an OFF condition on expiry of the 32 seconds timeout. Recovery from this forced OFF condition cannot occur until the external reset condition is de-asserted, followed by a valid ON event. If an ON event occurs before the external reset is de-asserted, then start-up will be attempted, but the transition will be unsuccessful, causing a return to the OFF state.

It is possible to mask the $\overline{\text{RESET}}$ pin input in the SLEEP state by setting the RST_SLP_MSK register bit as described in Section 11.7.

24.3 SOFTWARE RESET

A Software Reset is triggered by writing to Register 0000h, as described in Section 12.5. In this event, the WM8311 asserts the $\overline{\text{RESET}}$ pin and transitions to the OFF state. If the Reset occurred in the ON state, then the WM8311 will automatically return to the ON state following the Reset.

The SWRST_DLY register field determines whether a time delay is applied between the Software Reset command and the resultant shutdown and start-up sequences. When the SWRST_DLY bit is set, the programmable time delay PWRSTATE_DLY is applied before commencing the shutdown sequence.

The timing of the Software Reset is illustrated in Figure 37. See Section 11.3 for a definition of the PWRSTATE_DLY register.

The SW_RESET_CFG register field determines if the Register Map is reset under a Software Reset condition.

Note that the SW_RESET_CFG control register is locked by the WM8311 User Key. This register can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16387 (4003h) Power State	9	SWRST_DLY	0	Software Reset Delay 0 = No delay 1 = Software Reset is delayed by PWRSTATE_DLY following the Software Reset command
R16390 (4006h) Reset Control	10	SW_RESET_CFG	1	Software Reset Configuration. Selects whether the register map is reset to default values when Software Reset occurs. 0 = All registers except RTC and Software Scratch registers are reset by Software Reset 1 = Register Map is not affected by Software Reset *Protected by user key*

Table 107 Software Reset Configuration

The timing details of the Software Reset are illustrated in Figure 37.

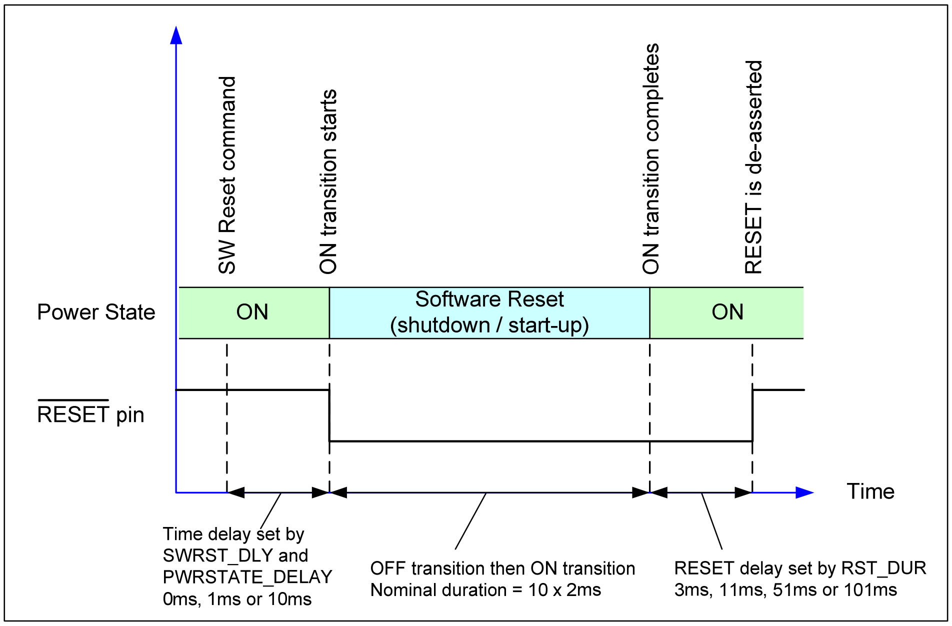


Figure 37 Software Reset Timing

24.4 SUPPLY VOLTAGE MONITORING

The WM8311 includes a number of mechanisms to prevent the system from starting up, or to force it to shut down, when the power sources are critically low.

The power supply configuration for the WM8311 is described in Section 17. The chip automatically chooses the most suitable supply, selecting between a Wall adapter supply, USB or Battery. The preferred source is routed to the SYSVDD pin, to which the other power management circuits would typically be connected. The SYSVDD voltage is monitored internally, as described below.

The internal regulator LDO12 is powered from an internal domain equivalent to SYSVDD and generates an internal supply (VPMIC) to support various “always-on” functions. In the absence of the Wall, USB or Battery supplies, LDO12 can be powered from a backup supply. (Note that SYSVDD is not maintained by the backup supply.) The VPMIC monitoring function controls the Power-On Reset circuit, which sets the threshold below which the WM8311 cannot operate.

The operation of the VPMIC monitoring circuit is illustrated in Figure 38. The internal signal $\overline{\text{PORRST}}$ is governed by the V_{POR} thresholds. These determine when the WM8311 is kept in the NO POWER state. The internal signal $\overline{\text{PMICRST}}$ is governed by the V_{RES} thresholds. These determine when the WM8311 is kept in the BACKUP state.

The VPMIC monitoring thresholds illustrated in Figure 38 are fixed. The voltage levels are defined in the Electrical Characteristics - see Section 7.5.

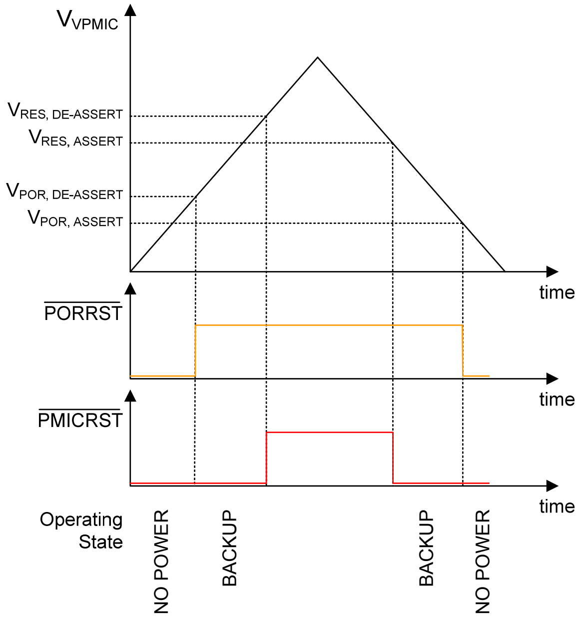


Figure 38 VPMIC Monitoring

The operation of the SYSVDD monitoring circuit is illustrated in Figure 39. The $V_{SHUTDOWN}$ threshold is the voltage below which the WM8311 forces an OFF transition. This threshold voltage is fixed and is defined in the Electrical Characteristics - see Section 7.5.

The V_{SYSOK} threshold is the level at which the internal signal SYSOK is asserted. Any ON request will be inhibited if SYSOK is not set. The V_{SYSOK} threshold can be set using the SYSOK_THR register field in accordance with the minimum voltage requirements of the application. Note that a hysteresis margin is added to the SYSOK_THR setting; see Section 7.5 for details.

The V_{SYSLO} threshold is the level at which the internal signal SYSLO is asserted. This indicates a SYSVDD undervoltage condition, at which a selectable response can be initiated. The V_{SYSLO} threshold can be set using the SYSLO_THR register field. The action taken under this undervoltage condition is selected using the SYSLO_ERR_ACT register field, as defined in Table 108. An Interrupt event is associated with the SYSLO condition - see Section 17.5.

The SYSLO status can be read from the SYSLO_STS register bit. This bit is asserted when SYSVDD is below the SYSLO threshold.

The WM8311 can also indicate the status of the SYSOK signal via a GPIO pin configured as a "SYSVDD Good" output (see Section 21). A GPIO pin configured as "SYSVDD Good" output will be asserted when the SYSVDD is above the SYSOK threshold.

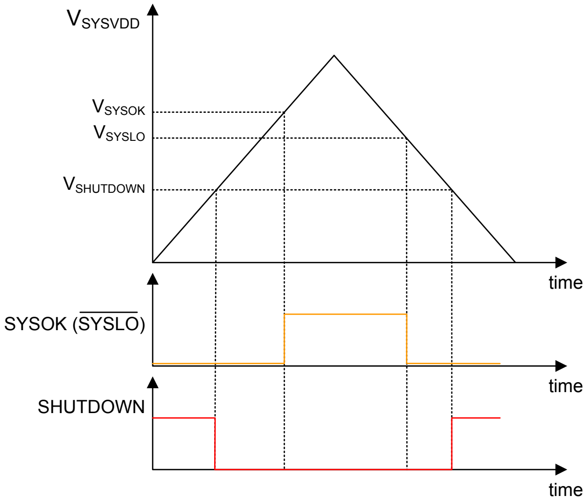


Figure 39 SYSVDD Monitoring

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16385 (4001h) SYSVDD Control	15:14	SYSLO_ERR_ ACT	00	SYSLO Error Action Selects the action taken when SYSLO is asserted 00 = Interrupt 01 = WAKE transition 10 = Reserved 11 = OFF transition
	11	SYSLO_STS	0	SYSLO Status 0 = Normal 1 = SYSVDD is below SYSLO threshold
	6:4	SYSLO_THR [2:0]	010	SYSLO threshold (falling SYSVDD) This is the falling SYSVDD voltage at which SYSLO will be asserted 000 = 2.8V 001 = 2.9V … 111 = 3.5V
	2:0	SYSOK_THR [2:0]	101	SYSOK threshold (rising SYSVDD) This is the rising SYSVDD voltage at which SYSOK will be asserted 000 = 2.8V 001 = 2.9V … 111 = 3.5V Note that the SYSOK hysteresis margin is added to these threshold levels.

Table 108 SYSVDD Monitoring Control

25 WATCHDOG TIMER

The WM8311 includes a Watchdog Timer designed to detect a possible software fault condition where the host processor has locked up. The Watchdog Timer is a free-running counter driven by the internal RC oscillator.

The Watchdog Timer is enabled by default; it can be enabled or disabled by writing to the WDOG_ENA register bit. The Watchdog behaviour in SLEEP is configurable; it can either be set to continue as normal or to be disabled. The Watchdog behaviour in SLEEP is determined by the WDOG_SLPENA bit.

The watchdog timer duration is set using WDOG_TO. The watchdog timer can be halted for debug purposes using the WDOG_DEBUG bit.

The Watchdog reset source is selectable between Software and Hardware triggers. (Note that the de-selected reset source has no effect.) If the Watchdog is not reset within a programmable timeout period, this is interpreted by the WM8311 as a fault condition. The Watchdog Timer then either triggers a Device Reset, or issues a WAKE request or raises an Interrupt. The action taken is determined by the WDOG_PRIMACT register field.

If the Watchdog is not reset within a further timeout period of the Watchdog counter, a secondary action is triggered. The secondary action taken at this point is determined by the WDOG_SECACT register field.

The Watchdog reset source is selected using the WDOG_RST_SRC register bit. When Software WDOG reset source is selected, the Watchdog is reset by writing a ‘1’ to the WDOG_RESET field. When Hardware WDOG reset source is selected, the Watchdog is reset by toggling a GPIO pin that has been configured as a Watchdog Reset Input (see Section 21).

If a Device Reset is triggered by the watchdog timeout, the WM8311 asserts the $\overline{\text{RESET}}$ pin, resets the internal control registers (excluding the RTC) and initiates a start-up sequence. The Watchdog Timer is not automatically reset as part of the Device Reset; the Watchdog must be reset by the host application following the Device Reset.

Note that, following a Device Reset, the action taken on subsequent timeout of the Watchdog Timer will be determined by the WDOG_PRIMACT register. If the watchdog timeout fault persists, then a maximum of 6 Device Reset attempts will be made. See Section 24. If the watchdog timeout occurs more than 6 times, the WM8311 will remain in the OFF state until the next valid ON state transition event occurs.

Note that the Watchdog control registers are locked by the WM8311 User Key. These registers can only be changed by writing the appropriate code to the Security register, as described in Section 12.4.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16388 (4004h) Watchdog	15	WDOG_ENA	1	Watchdog Timer Enable 0 = Disabled 1 = Enabled (enables the watchdog; does not reset it) *Protected by user key*
	14	WDOG_DEBUG	0	Watchdog Pause 0 = Disabled 1 = Enabled (halts the Watchdog timer for system debugging) *Protected by user key*
	13	WDOG_RST_SRC	1	Watchdog Reset Source 0 = Hardware only 1 = Software only *Protected by user key*
	12	WDOG_SLPENA	0	Watchdog SLEEP Enable 0 = Disabled 1 = Controlled by WDOG_ENA *Protected by user key*

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	11	WDOG_RESET	0	Watchdog Software Reset 0 = Normal 1 = Watchdog Reset (resets the watchdog, if WDOG_RST_SRC = 1) *Protected by user key*
	9:8	WDOG_SECACT	10	Secondary action of Watchdog timeout (taken after 2 timeout periods) 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition *Protected by user key*
	5:4	WDOG_PRIMACT	01	Primary action of Watchdog timeout 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition *Protected by user key*
	2:0	WDOG_TO [2:0]	111	Watchdog timeout period 000 = 0.256s 001 = 0.512s 010 = 1.024s 011 = 2.048s 100 = 4.096s 101 = 8.192s 110 = 16.384s 111 = 32.768s *Protected by user key*

Table 109 Controlling the Watchdog Timer

The Watchdog timeout interrupt event is indicated by the WDOG_TO_EINT register field. This secondary interrupt triggers a primary Watchdog Interrupt, WDOG_INT (see Section 23). This can be masked by setting the mask bit as described in Table 110.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	11	WDOG_TO_EINT	Watchdog timeout interrupt. (Rising Edge triggered) Note: Cleared when a ‘1’ is written.
R16409 (4019h) Interrupt Status 1 Mask	11	IM_WDOG_TO_EINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 110 Watchdog Timer Interrupts

26 TEMPERATURE SENSING

The WM8311 provides temperature monitoring as status information and also for self-protection of the device. Temperature monitoring is always enabled in the ON and SLEEP states.

The thermal warning temperature can be set using the THW_TEMP register field. The thermal warning hysteresis ensures that the THW_TEMP is not reset until the device temperature has dropped below the threshold by a suitable margin. The extent of the hysteresis can be selected using the THW_HYST register field.

The Thermal Warning condition can be read using the THW_STS register bit. An overtemperature condition causes the thermal warning interrupt (TEMP_THW_CINT) to be set. The thermal warning interrupt is also set when the overtemperature condition clears, ie. when the device has returned to its normal operating limits.

The thermal shutdown temperature is set at a fixed level. If a thermal shutdown condition is detected whilst in the ON or SLEEP states, then a System Reset is triggered, as described in Section 24.1, forcing a transition to the OFF state.

The temperature sensing circuit is configured and monitored using the register fields described in Table 111.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16386 (4002h)	3	THW_HYST	1	Thermal Warning hysteresis 0 = 8 degrees C 1 = 16 degrees C
	1:0	THW_TEMP [1:0]	10	Thermal Warning temperature 00 = 90 degrees C 01 = 100 degrees C 10 = 110 degrees C 11 = 120 degrees C
R16397 (400Dh)	15	THW_STS	0	Thermal Warning status 0 = Normal 1 = Overtemperature Warning (warning temperature is set by THW_TEMP)

Table 111 Temperature Sensing Control

The thermal warning interrupt event is indicated by the TEMP_THW_CINT register field. This secondary interrupt triggers a primary Thermal Interrupt, TEMP_INT (see Section 23). This can be masked by setting the mask bit as described in Table 112.

ADDRESS	BIT	LABEL	DESCRIPTION
R16401 (4011h) Interrupt Status 1	1	TEMP_THW_CINT	Thermal Warning interrupt (Rising and Falling Edge triggered) Note: Cleared when a ‘1’ is written.
R16410 (4019h) Interrupt Status 1 Mask	1	IM_TEMP_THW_CINT	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)

Table 112 Thermal Interrupts

27 VOLTAGE AND CURRENT REFERENCES

27.1 VOLTAGE REFERENCE (VREF)

The main voltage reference generated by the WM8311 is bonded to the VREFC pin. The accuracy of this reference is optimised by factory-set trim registers.

The voltage reference (VREF) requires an external decoupling capacitor; a 100nF X5R capacitor is recommended for typical applications, as noted in Section 30.2. If USB100MA_STARTUP=1X (see Section 17.4), then a 50nF capacitor should be used. Omitting this capacitor will result in increased noise on the voltage reference; this will particularly affect the analogue LDOs.

The VREFC capacitor should be grounded to the REFGND pin.

The voltage reference circuit includes a low-power mode, which enables power consumption to be minimised where appropriate. The low-power reference mode may lead to increased noise on the voltage reference; this mode should only be selected when minimum power consumption is more important than voltage stability. Note that the Low Power Reference mode is not supported when the Touch Panel or Auxiliary ADC functions are enabled.

The Low Power Reference mode is enabled when REF_LP register is set. The Low Power Reference mode should only be enabled when the Touch Panel and Auxiliary ADC are both disabled. Enabling the Low Power Reference mode will lead to a malfunction of the Touch Panel or Auxiliary ADC functions.

ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16387 (4003h)	12	REF_LP	0	Low Power Voltage Reference Control 0 = Normal 1 = Low Power Reference Mode select Note that Low Power Reference Mode is only supported when the Touch Panel and Auxiliary ADC are both disabled.

Table 113 Low Power Voltage Reference Control

27.2 CURRENT REFERENCE (IREF)

The Power Management circuits of the WM8311 use an integrated current reference.

This current reference (IREF) requires the connection of an external resistor to the IREFR pin; a 100kΩ (1%) resistor is recommended, as noted in Section 30.2. The WM8311 will malfunction if this resistor is omitted.

The IREFR resistor should be grounded to the REFGND pin.

28 REGISTER MAP OVERVIEW

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
0	0000	Reset ID	CHIP_ID[15:0]																0000_0000_0000_0000
1	0001	Revision	PARENT_REV[7:0]								CHILD_REV[7:0]								0000_0000_0000_0000
2	0002	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
3	0003	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
4	0004	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
5	0005	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
6	0006	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
7	0007	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16384	4000	Parent ID	PARENT_ID[15:0]																0110_0010_0000_0100
16385	4001	SYSVDD Control	SYSLO_ERR_ACT[1:0]		0	0	SYSLO_STS	0	0	0	0	SYSLO_THR[2:0]			0	SYSOK_THR[2:0]			0000_0000_0010_0101
16386	4002	Thermal Monitoring	0	0	0	0	0	0	0	0	0	0	0	0	THW_HYST	0	THW_TEMP[1:0]		0000_0000_0000_1010
16387	4003	Power State	CHIP_ON	CHIP_SLP	0	REF_LP	PWRSTATE_DLY[1:0]		SWRST_DLY	0	0	0	USB100MA_STARTUP[1:0]		USB_CURR_STS	USB_ILIM[2:0]			UU00_1000_0000_0010
16388	4004	Watchdog	WDOG_ENA	WDOG_DEBUG	WDOG_RST_SRC	WDOG_SLPENA	WDOG_RESET	0	WDOG_SECACT[1:0]		0	0	WDOG_PRIMACT[1:0]		0	WDOG_TO[2:0]			1010_P010_0001_0111
16389	4005	ON Pin Control	0	0	0	0	0	0	ON_PIN_SECACT[1:0]		0	0	ON_PIN_PRIMACT[1:0]		ON_PIN_STS	0	ON_PIN_TO[1:0]		0000_0001_0000_0000
16390	4006	Reset Control	RECONFIG_AT_ON	0	WALL_FET_ENA_DRV_STR	BATT_FET_ENA	0	SW_RESET_CFG	0	0	0	AUXRST_SLPENA	RST_SLP_MSK	RST_SLPENA	0	0	RST_DUR[1:0]		1000_0100_0111_0011
16391	4007	Control Interface	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTOINC	0	0	0000_0000_0000_0100
16392	4008	Security Key	SECURITY[15:0]																0000_0000_0000_0000
16393	4009	Software Scratch	SW_SCRATCH[15:0]																0000_0000_0000_0000
16394	400A	OTP Control	OTP_PROG	0	OTP_MEM	0	OTP_FINAL	OTP_VERIFY	OTP_WRITE	OTP_READ	OTP_READ_LVL[1:0]		OTP_BULK	0	0	0	OTP_PAGE[1:0]		U010_0000_0000_0000
16395	400B	Security Key 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16396	400C	GPIO Level	GP16_LVL	GP15_LVL	GP14_LVL	GP13_LVL	GP12_LVL	GP11_LVL	GP10_LVL	GP9_LVL	GP8_LVL	GP7_LVL	GP6_LVL	GP5_LVL	GP4_LVL	GP3_LVL	GP2_LVL	GP1_LVL	0000_0000_0000_0000
16397	400D	System Status	THW_STS	0	0	0	0	PWR_SRC_BATT	PWR_WALL	PWR_USB	0	0	0	MAIN_STATE[4:0]					0000_0000_0000_0000
16398	400E	ON Source	ON_TRANS	0	0	0	ON_GPIO	ON_SYSLO	ON_PEN_DOWN	ON_CHG	ON_WDOG_TO	ON_SW_REQ	ON_RTC_ALM	ON_ON_PIN	RESET_CNV_UV	RESET_SW	RESET_HW	RESET_WDOG	0000_0000_0000_0000
16399	400F	OFF Source	0	0	OFF_INTLDO_ERR	OFF_PWR_SEQ	OFF_GPIO	OFF_SYSVDD	OFF_THERR	0	0	OFF_SW_REQ	0	OFF_ON_PIN	0	0	0	0	0000_0000_0000_0000
16400	4010	System Interrupts	PS_INT	TEMP_INT	GP_INT	ON_PIN_INT	WDOG_INT	TCHDATA_INT	TCHPD_INT	AUXADC_INT	PPM_INT	CS_INT	RTC_INT	OTP_INT	0	CHG_INT	HC_INT	UV_INT	PPPP_PPPP_PPPP_PPPP
16401	4011	Interrupt Status 1	PPM_SYSLO_EINT	PPM_PWR_SRC_EINT	PPM_USB_CURR_EINT	ON_PIN_CINT	WDOG_TO_EINT	TCHDATA_EINT	TCHPD_EINT	AUXADC_DATA_EINT	AUXADC_DCOMP4_EINT	AUXADC_DCOMP3_EINT	AUXADC_DCOMP2_EINT	AUXADC_DCOMP1_EINT	RTC_PER_EINT	RTC_ALM_EINT	TEMP_THW_CINT	0	PPPP_PPPP_PPPP_PPP0
16402	4012	Interrupt Status 2	CHG_BATT_HOT_EINT	CHG_BATT_COLD_EINT	CHG_BATT_FAIL_EINT	CHG_OV_EINT	CHG_END_EINT	CHG_TO_EINT	CHG_MODE_EINT	CHG_START_EINT	CS2_EINT	CS1_EINT	OTP_CMD_END_EINT	OTP_ERR_EINT	0	PS_POR_EINT	PS_SLEEP_OFF_EINT	PS_ON_WAKE_EINT	PPPP_PPPP_PPPP_0PPP
16403	4013	Interrupt Status 3	0	0	0	0	0	0	0	0	0	UV_LDO7_EINT	0	UV_LDO5_EINT	UV_LDO4_EINT	UV_LDO3_EINT	UV_LDO2_EINT	UV_LDO1_EINT	0000_00PP_PPPP_PPPP
16404	4014	Interrupt Status 4	0	0	0	0	0	0	HC_DC2_EINT	HC_DC1_EINT	0	0	0	0	UV_DC4_EINT	UV_DC3_EINT	UV_DC2_EINT	UV_DC1_EINT	0000_00PP_PP00_PPPP
16405	4015	Interrupt Status 5	GP16_EINT	GP15_EINT	GP14_EINT	GP13_EINT	GP12_EINT	GP11_EINT	GP10_EINT	GP9_EINT	GP8_EINT	GP7_EINT	GP6_EINT	GP5_EINT	GP4_EINT	GP3_EINT	GP2_EINT	GP1_EINT	PPPP_PPPP_PPPP_PPPP
16406	4016	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16407	4017	IRQ Config	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IRQ_OD	IM_IRQ	0000_0000_0000_0010

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
16408	4018	System Interrupts Mask	IM_PS_INT	IM_TEMP_INT	IM_GP_INT	IM_ON_PIN_INT	IM_WDOG_INT	IM_TCHDATA_INT	IM_TCHPD_INT	IM_AUXADC_INT	IM_PPM_INT	IM_CS_INT	IM_RTC_INT	IM_OTP_INT	1	IM_CHG_INT	IM_HC_INT	IM_UV_INT	1111_1111_1111_1111
16409	4019	Interrupt Status 1 Mask	IM_PPM_SYSLO_EINT	IM_PPM_PWR_SRC_EINT	IM_PPM_USB_CURR_EINT	IM_ON_PIN_CINT	IM_WDOG_TO_EINT	IM_TCHDATA_EINT	IM_TCHPD_EINT	IM_AUXADC_DATA_EINT	IM_AUXADC_DCOMP4_EINT	IM_AUXADC_DCOMP3_EINT	IM_AUXADC_DCOMP2_EINT	IM_AUXADC_DCOMP1_EINT	IM_RTC_PER_EINT	IM_RTC_ALM_EINT	IM_TEMP_THW_CINT	0	1111_1111_1111_1110
16410	401A	Interrupt Status 2 Mask	IM_CHG_BATT_HOT_EINT	IM_CHG_BATT_COLD_EINT	IM_CHG_BATT_FAIL_EINT	IM_CHG_OV_EINT	IM_CHG_END_EINT	IM_CHG_TO_EINT	IM_CHG_MODE_EINT	IM_CHG_START_EINT	IM_CS2_EINT	IM_CS1_EINT	IM_OTP_CMD_END_EINT	IM_OTP_ERR_EINT	0	IM_PS_POR_EINT	IM_PS_SLEEP_OFF_EINT	IM_PS_ON_WAKE_EINT	1111_1111_1111_0111
16411	401B	Interrupt Status 3 Mask	0	0	0	0	0	0	1	1	1	IM_UV_LDO7_EINT	1	IM_UV_LDO5_EINT	IM_UV_LDO4_EINT	IM_UV_LDO3_EINT	IM_UV_LDO2_EINT	IM_UV_LDO1_EINT	0000_0011_1111_1111
16412	401C	Interrupt Status 4 Mask	0	0	0	0	0	0	IM_HC_DC2_EINT	IM_HC_DC1_EINT	1	0	0	0	IM_UV_DC4_EINT	IM_UV_DC3_EINT	IM_UV_DC2_EINT	IM_UV_DC1_EINT	0000_0011_1000_1111
16413	401D	Interrupt Status 5 Mask	IM_GP16_EINT	IM_GP15_EINT	IM_GP14_EINT	IM_GP13_EINT	IM_GP12_EINT	IM_GP11_EINT	IM_GP10_EINT	IM_GP9_EINT	IM_GP8_EINT	IM_GP7_EINT	IM_GP6_EINT	IM_GP5_EINT	IM_GP4_EINT	IM_GP3_EINT	IM_GP2_EINT	IM_GP1_EINT	1111_1111_1111_1111
16414	401E	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16415	401F	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16416	4020	RTC Write Counter	RTC_WR_CNT[15:0]																0000_0000_0000_0000
16417	4021	RTC Time 1	RTC_TIME[31:16]																0000_0000_0000_0000
16418	4022	RTC Time 2	RTC_TIME[15:0]																0000_0000_0000_0000
16419	4023	RTC Alarm 1	RTC_ALM[31:16]																0000_0000_0000_0000
16420	4024	RTC Alarm 2	RTC_ALM[15:0]																0000_0000_0000_0000
16421	4025	RTC Control	RTC_VALID	RTC_SYNC_BUSY	0	0	0	RTC_ALM_ENA	0	0	0	RTC_PINT_FREQ[2:0]			0	0	0	0	0000_0000_0000_0000
16422	4026	RTC Trim	0	0	0	0	0	0	RTC_TRIM[9:0]										0000_0000_0000_0000
16423	4027	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16424	4028	Touch Control 1	TCH_ENA	TCH_CVT_ENA	0	TCH_SLPENA	0	TCH_Z_ENA	TCH_Y_ENA	TCH_X_ENA	TCH_DELAY[2:0]			TCH_RATE[4:0]					0U00_0000_0100_0000
16425	4029	Touch Control 2	0	0	TCH_PD_WK	TCH_5WIRE	TCH_PDONLY	0	0	TCH_ISEL	0	0	0	0	TCH_RPU[3:0]				0000_0000_0000_0111
16426	402A	Touch Data X	TCH_PD1	0	0	0	TCH_X[11:0]												0000_0000_0000_0000
16427	402B	Touch Data Y	TCH_PD2	0	0	0	TCH_Y[11:0]												0000_0000_0000_0000
16428	402C	Touch Data Z	TCH_PD3	0	0	0	TCH_Z[11:0]												0000_0000_0000_0000
16429	402D	AuxADC Data	AUX_DATA_SRC[3:0]				AUX_DATA[11:0]												0000_0000_0000_0000
16430	402E	AuxADC Control	AUX_ENA	AUX_CVT_ENA	0	AUX_SLPENA	0	0	0	0	0	0	AUX_RATE[5:0]						0U00_0000_0000_0000
16431	402F	AuxADC Source	0	0	0	0	0	0	AUX_WALL_SEL	AUX_BATT_SEL	AUX_USB_SEL	AUX_SYSVDD_SEL	AUX_BATT_TEMP_SEL	AUX_CHIP_TEMP_SEL	AUX_AUX4_SEL	AUX_AUX3_SEL	AUX_AUX2_SEL	AUX_AUX1_SEL	0000_0000_0000_0000
16432	4030	Comparator Control	0	0	0	0	DCOMP4_STS	DCOMP3_STS	DCOMP2_STS	DCOMP1_STS	0	0	0	0	DCMP4_ENA	DCMP3_ENA	DCMP2_ENA	DCMP1_ENA	0000_0000_0000_0000
16433	4031	Comparator 1	DCMP1_SRC[2:0]			DCMP1_GT	DCMP1_THR[11:0]												0000_0000_0000_0000
16434	4032	Comparator 2	DCMP2_SRC[2:0]			DCMP2_GT	DCMP2_THR[11:0]												0000_0000_0000_0000
16435	4033	Comparator 3	DCMP3_SRC[2:0]			DCMP3_GT	DCMP3_THR[11:0]												0000_0000_0000_0000
16436	4034	Comparator 4	DCMP4_SRC[2:0]			DCMP4_GT	DCMP4_THR[11:0]												0000_0000_0000_0000
16437	4035	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16438	4036	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16439	4037	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
16440	4038	GPIO1 Control	GP1_DIR	GP1_PULL[1:0]		GP1_INT_MODE	GP1_PWR_DOM	GP1_POL	GP1_OD	0	GP1_ENA	0	0	0	GP1_FN[3:0]				1010_0100_0000_0000
16441	4039	GPIO2 Control	GP2_DIR	GP2_PULL[1:0]		GP2_INT_MODE	GP2_PWR_DOM	GP2_POL	GP2_OD	0	GP2_ENA	0	0	0	GP2_FN[3:0]				1010_0100_0000_0000
16442	403A	GPIO3 Control	GP3_DIR	GP3_PULL[1:0]		GP3_INT_MODE	GP3_PWR_DOM	GP3_POL	GP3_OD	0	GP3_ENA	0	0	0	GP3_FN[3:0]				1010_0100_0000_0000
16443	403B	GPIO4 Control	GP4_DIR	GP4_PULL[1:0]		GP4_INT_MODE	GP4_PWR_DOM	GP4_POL	GP4_OD	0	GP4_ENA	0	0	0	GP4_FN[3:0]				1010_0100_0000_0000
16444	403C	GPIO5 Control	GP5_DIR	GP5_PULL[1:0]		GP5_INT_MODE	GP5_PWR_DOM	GP5_POL	GP5_OD	0	GP5_ENA	0	0	0	GP5_FN[3:0]				1010_0100_0000_0000
16445	403D	GPIO6 Control	GP6_DIR	GP6_PULL[1:0]		GP6_INT_MODE	GP6_PWR_DOM	GP6_POL	GP6_OD	0	GP6_ENA	0	0	0	GP6_FN[3:0]				1010_0100_0000_0000
16446	403E	GPIO7 Control	GP7_DIR	GP7_PULL[1:0]		GP7_INT_MODE	GP7_PWR_DOM	GP7_POL	GP7_OD	0	GP7_ENA	0	0	0	GP7_FN[3:0]				1010_0100_0000_0000
16447	403F	GPIO8 Control	GP8_DIR	GP8_PULL[1:0]		GP8_INT_MODE	GP8_PWR_DOM	GP8_POL	GP8_OD	0	GP8_ENA	0	0	0	GP8_FN[3:0]				1010_0100_0000_0000
16448	4040	GPIO9 Control	GP9_DIR	GP9_PULL[1:0]		GP9_INT_MODE	GP9_PWR_DOM	GP9_POL	GP9_OD	0	GP9_ENA	0	0	0	GP9_FN[3:0]				1010_0100_0000_0000
16449	4041	GPIO10 Control	GP10_DIR	GP10_PULL[1:0]		GP10_INT_MODE	GP10_PWR_DOM	GP10_POL	GP10_OD	0	GP10_ENA	0	0	0	GP10_FN[3:0]				1010_0100_0000_0000
16450	4042	GPIO11 Control	GP11_DIR	GP11_PULL[1:0]		GP11_INT_MODE	GP11_PWR_DOM	GP11_POL	GP11_OD	0	GP11_ENA	0	0	0	GP11_FN[3:0]				1010_0100_0000_0000
16451	4043	GPIO12 Control	GP12_DIR	GP12_PULL[1:0]		GP12_INT_MODE	GP12_PWR_DOM	GP12_POL	GP12_OD	0	GP12_ENA	0	0	0	GP12_FN[3:0]				1010_0100_0000_0000
16452	4044	GPIO13 Control	GP13_DIR	GP13_PULL[1:0]		GP13_INT_MODE	0	GP13_POL	GP13_OD	0	GP13_ENA	0	0	0	GP13_FN[3:0]				1010_0100_0000_0000
16453	4045	GPIO14 Control	GP14_DIR	GP14_PULL[1:0]		GP14_INT_MODE	0	GP14_POL	GP14_OD	0	GP14_ENA	0	0	0	GP14_FN[3:0]				1010_0100_0000_0000
16454	4046	GPIO15 Control	GP15_DIR	GP15_PULL[1:0]		GP15_INT_MODE	0	GP15_POL	GP15_OD	0	GP15_ENA	0	0	0	GP15_FN[3:0]				1010_0100_0000_0000
16455	4047	GPIO16 Control	GP16_DIR	GP16_PULL[1:0]		GP16_INT_MODE	0	GP16_POL	GP16_OD	0	GP16_ENA	0	0	0	GP16_FN[3:0]				1010_0100_0000_0000
16456	4048	Charger Control 1	CHG_ENA	CHG_FRC	0	CHG_ITERM[2:0]			0	0	0	0	CHG_FAST	0	0	0	CHG_IMON_ENA	CHG_CHIP_TEMP_MON	0000_0000_0000_0001
16457	4049	Charger Control 2	0	CHG_OFF_MSK	0	0	CHG_TIME[3:0]				CHG_TRKL_ILIM[1:0]		CHG_VSEL[1:0]		CHG_FAST_ILIM[3:0]				0000_0110_0000_0010
16458	404A	Charger Status	BATT_OV_STS	CHG_STATE[2:0]			BATT_HOT_STS	BATT_COLD_STS	CHG_TOPOFF	CHG_ACTIVE	CHG_TIME_ELAPSED[7:0]								0000_0000_0000_0000
16459	404B	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16460	404C	Status LED 1	LED1_SRC[1:0]		0	0	0	0	LED1_MODE[1:0]		0	0	LED1_SEQ_LEN[1:0]		LED1_DUR[1:0]		LED1_DUTY_CYC[1:0]		1100_0000_0010_0110
16461	404D	Status LED 2	LED2_SRC[1:0]		0	0	0	0	LED2_MODE[1:0]		0	0	LED2_SEQ_LEN[1:0]		LED2_DUR[1:0]		LED2_DUTY_CYC[1:0]		1100_0000_0010_0110
16462	404E	Current Sink 1	CS1_ENA	CS1_DRIVE	CS1_STS	CS1_SLPENA	CS1_OFF_RAMP[1:0]		CS1_ON_RAMP[1:0]		0	0	CS1_ISEL[5:0]						0U00_0101_0000_0000
16463	404F	Current Sink 2	CS2_ENA	CS2_DRIVE	CS2_STS	CS2_SLPENA	CS2_OFF_RAMP[1:0]		CS2_ON_RAMP[1:0]		0	0	CS2_ISEL[5:0]						0U00_0101_0000_0000
16464	4050	DCDC Enable	0	0	0	0	0	0	0	0	EPE2_ENA	EPE1_ENA	0	0	DC4_ENA	DC3_ENA	DC2_ENA	DC1_ENA	0000_0000_UU00_UUUU
16465	4051	LDO Enable	0	0	0	0	0	LDO11_ENA	0	0	0	LDO7_ENA	0	LDO5_ENA	LDO4_ENA	LDO3_ENA	LDO2_ENA	LDO1_ENA	0000_0UUU_UUUU_UUUU
16466	4052	DCDC Status	0	0	0	0	0	0	0	0	EPE2_STS	EPE1_STS	0	0	DC4_STS	DC3_STS	DC2_STS	DC1_STS	0000_0000_0000_0000
16467	4053	LDO Status	0	0	0	0	0	LDO11_STS	0	0	0	LDO7_STS	0	LDO5_STS	LDO4_STS	LDO3_STS	LDO2_STS	LDO1_STS	0000_0000_0000_0000
16468	4054	DCDC UV Status	0	0	DC2_OV_STS	DC1_OV_STS	0	0	DC2_HC_STS	DC1_HC_STS	0	0	0	0	DC4_UV_STS	DC3_UV_STS	DC2_UV_STS	DC1_UV_STS	0000_0000_0000_0000
16469	4055	LDO UV Status	INTLDO_UV_STS	0	0	0	0	0	0	0	0	LDO7_UV_STS	0	LDO5_UV_STS	LDO4_UV_STS	LDO3_UV_STS	LDO2_UV_STS	LDO1_UV_STS	0000_0000_0000_0000
16470	4056	DC1 Control 1	DC1_RATE[1:0]		0	DC1_PHASE	0	0	DC1_FREQ[1:0]		DC1_FLT	0	DC1_SOFT_START[1:0]		0	0	DC1_CAP[1:0]		1000_0000_0000_0000
16471	4057	DC1 Control 2	DC1_ERR_ACT[1:0]		0	DC1_HWC_SRC[1:0]		DC1_HWC_VSEL	DC1_HWC_MODE[1:0]		0	DC1_HC_THR[2:0]			0	0	0	DC1_HC_IND_ENA	0000_0011_0000_0000

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
16472	4058	DC1 ON Config	DC1_ON_SLOT[2:0]			0	0	0	DC1_ON_MODE[1:0]		0	DC1_ON_VSEL[6:2]					DC1_ON_VSEL[1:0]		0000_0001_0000_0000
16473	4059	DC1 SLEEP Control	DC1_SLP_SLOT[2:0]			0	0	0	DC1_SLP_MODE[1:0]		0	DC1_SLP_VSEL[6:0]							0000_0011_0000_0000
16474	405A	DC1 DVS Control	0	0	0	DC1_DVS_SRC[1:0]		0	0	0	0	DC1_DVS_VSEL[6:0]							0000_0000_0000_0000
16475	405B	DC2 Control 1	DC2_RATE[1:0]		0	DC2_PHASE	0	0	DC2_FREQ[1:0]		DC2_FLT	0	DC2_SOFT_START[1:0]		0	0	DC2_CAP[1:0]		1001_0000_0000_0000
16476	405C	DC2 Control 2	DC2_ERR_ACT[1:0]		0	DC2_HWC_SRC[1:0]		DC2_HWC_VSEL	DC2_HWC_MODE[1:0]		0	DC2_HC_THR[2:0]			0	0	0	DC2_HC_IND_ENA	0000_0011_0000_0000
16477	405D	DC2 ON Config	DC2_ON_SLOT[2:0]			0	0	0	DC2_ON_MODE[1:0]		0	DC2_ON_VSEL[6:2]					DC2_ON_VSEL[1:0]		0000_0001_0000_0000
16478	405E	DC2 SLEEP Control	DC2_SLP_SLOT[2:0]			0	0	0	DC2_SLP_MODE[1:0]		0	DC2_SLP_VSEL[6:0]							0000_0011_0000_0000
16479	405F	DC2 DVS Control	0	0	0	DC2_DVS_SRC[1:0]		0	0	0	0	DC2_DVS_VSEL[6:0]							0000_0000_0000_0000
16480	4060	DC3 Control 1	0	0	0	DC3_PHASE	0	0	0	0	DC3_FLT	0	DC3_SOFT_START[1:0]		DC3_STNBY_LIM[1:0]		DC3_CAP[1:0]		0000_0000_0001_0100
16481	4061	DC3 Control 2	DC3_ERR_ACT[1:0]		0	DC3_HWC_SRC[1:0]		DC3_HWC_VSEL	DC3_HWC_MODE[1:0]		DC3_OVP	0	0	0	0	0	0	0	0000_0011_0000_0000
16482	4062	DC3 ON Config	DC3_ON_SLOT[2:0]			0	0	0	DC3_ON_MODE[1:0]		0	DC3_ON_VSEL[6:2]					DC3_ON_VSEL[1:0]		0000_0001_0000_0000
16483	4063	DC3 SLEEP Control	DC3_SLP_SLOT[2:0]			0	0	0	DC3_SLP_MODE[1:0]		0	DC3_SLP_VSEL[6:0]							0000_0011_0000_0000
16484	4064	DC4 Control	DC4_ERR_ACT[1:0]		0	DC4_HWC_SRC[1:0]		0	0	DC4_HWC_MODE	0	0	0	0	DC4_RANGE[1:0]		0	DC4_FBSRC	0000_0001_0000_0100
16485	4065	DC4 SLEEP Control	0	0	0	0	0	0	0	DC4_SLPENA	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16486	4066	EPE1 Control	EPE1_ON_SLOT[2:0]			EPE1_HWC_SRC[1:0]		0	0	EPE1_HWCENA	EPE1_SLP_SLOT[2:0]			0	0	0	0	0	0000_0000_0000_0000
16487	4067	EPE2 Control	EPE2_ON_SLOT[2:0]			EPE2_HWC_SRC[1:0]		0	0	EPE2_HWCENA	EPE2_SLP_SLOT[2:0]			0	0	0	0	0	0000_0000_0000_0000
16488	4068	LDO1 Control	LDO1_ERR_ACT[1:0]		0	LDO1_HWC_SRC[1:0]		LDO1_HWC_VSEL	LDO1_HWC_MODE[1:0]		LDO1_FLT	LDO1_SWI	0	0	0	0	0	LDO1_LP_MODE	0000_0010_0000_0000
16489	4069	LDO1 ON Control	LDO1_ON_SLOT[2:0]			0	0	0	0	LDO1_ON_MODE	0	0	0	LDO1_ON_VSEL[4:0]					0000_0000_0000_0000
16490	406A	LDO1 SLEEP Control	LDO1_SLP_SLOT[2:0]			0	0	0	0	LDO1_SLP_MODE	0	0	0	LDO1_SLP_VSEL[4:0]					0000_0001_0000_0000
16491	406B	LDO2 Control	LDO2_ERR_ACT[1:0]		0	LDO2_HWC_SRC[1:0]		LDO2_HWC_VSEL	LDO2_HWC_MODE[1:0]		LDO2_FLT	LDO2_SWI	0	0	0	0	0	LDO2_LP_MODE	0000_0010_0000_0000
16492	406C	LDO2 ON Control	LDO2_ON_SLOT[2:0]			0	0	0	0	LDO2_ON_MODE	0	0	0	LDO2_ON_VSEL[4:0]					0000_0000_0000_0000
16493	406D	LDO2 SLEEP Control	LDO2_SLP_SLOT[2:0]			0	0	0	0	LDO2_SLP_MODE	0	0	0	LDO2_SLP_VSEL[4:0]					0000_0001_0000_0000
16494	406E	LDO3 Control	LDO3_ERR_ACT[1:0]		0	LDO3_HWC_SRC[1:0]		LDO3_HWC_VSEL	LDO3_HWC_MODE[1:0]		LDO3_FLT	LDO3_SWI	0	0	0	0	0	LDO3_LP_MODE	0000_0010_0000_0000
16495	406F	LDO3 ON Control	LDO3_ON_SLOT[2:0]			0	0	0	0	LDO3_ON_MODE	0	0	0	LDO3_ON_VSEL[4:0]					0000_0000_0000_0000
16496	4070	LDO3 SLEEP Control	LDO3_SLP_SLOT[2:0]			0	0	0	0	LDO3_SLP_MODE	0	0	0	LDO3_SLP_VSEL[4:0]					0000_0001_0000_0000
16497	4071	LDO4 Control	LDO4_ERR_ACT[1:0]		0	LDO4_HWC_SRC[1:0]		LDO4_HWC_VSEL	LDO4_HWC_MODE[1:0]		LDO4_FLT	LDO4_SWI	0	0	0	0	0	LDO4_LP_MODE	0000_0010_0000_0000
16498	4072	LDO4 ON Control	LDO4_ON_SLOT[2:0]			0	0	0	0	LDO4_ON_MODE	0	0	0	LDO4_ON_VSEL[4:0]					0000_0000_0000_0000
16499	4073	LDO4 SLEEP Control	LDO4_SLP_SLOT[2:0]			0	0	0	0	LDO4_SLP_MODE	0	0	0	LDO4_SLP_VSEL[4:0]					0000_0001_0000_0000
16500	4074	LDO5 Control	LDO5_ERR_ACT[1:0]		0	LDO5_HWC_SRC[1:0]		LDO5_HWC_VSEL	LDO5_HWC_MODE[1:0]		LDO5_FLT	LDO5_SWI	0	0	0	0	0	LDO5_LP_MODE	0000_0010_0000_0000
16501	4075	LDO5 ON Control	LDO5_ON_SLOT[2:0]			0	0	0	0	LDO5_ON_MODE	0	0	0	LDO5_ON_VSEL[4:0]					0000_0000_0000_0000
16502	4076	LDO5 SLEEP Control	LDO5_SLP_SLOT[2:0]			0	0	0	0	LDO5_SLP_MODE	0	0	0	LDO5_SLP_VSEL[4:0]					0000_0001_0000_0000
16503	4077	LDO6 Control	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
16504	4078	LDO6 ON Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16505	4079	LDO6 SLEEP Control	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0000_0001_0000_0000
16506	407A	LDO7 Control	LDO7_ERR_ACT[1:0]		0	LDO7_HWC_SRC[1:0]		LDO7_HWC_VSEL	LDO7_HWC_MODE[1:0]		LDO7_FLT	LDO7_SWI	0	0	0	0	0	0	0000_0010_0000_0000
16507	407B	LDO7 ON Control	LDO7_ON_SLOT[2:0]			0	0	0	0	LDO7_ON_MODE	0	0	0	LDO7_ON_VSEL[4:0]					0000_0000_0000_0000
16508	407C	LDO7 SLEEP Control	LDO7_SLP_SLOT[2:0]			0	0	0	0	LDO7_SLP_MODE	0	0	0	LDO7_SLP_VSEL[4:0]					0000_0001_0000_0000
16509	407D	LDO8 Control	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000
16510	407E	LDO8 ON Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16511	407F	LDO8 SLEEP Control	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0000_0001_0000_0000
16512	4080	LDO9 Control	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000
16513	4081	LDO9 ON Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16514	4082	LDO9 SLEEP Control	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0000_0001_0000_0000
16515	4083	LDO10 Control	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0000_0010_0000_0000
16516	4084	LDO10 ON Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16517	4085	LDO10 SLEEP Control	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0000_0001_0000_0000
16518	4086	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16519	4087	LDO11 ON Control	LDO11_ON_SLOT[2:0]			LDO11_FRCENA	0	0	0	0	LDO11_VSEL_SRC	0	0	0	LDO11_ON_VSEL[3:0]				0000_0000_0000_0000
16520	4088	LDO11 SLEEP Control	LDO11_SLP_SLOT[2:0]			0	0	0	0	0	0	0	0	0	LDO11_SLP_VSEL[3:0]				0000_0000_0000_0000
16521	4089	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16522	408A	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16523	408B	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16524	408C	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16525	408D	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
16526	408E	Power Good Source 1	0	0	0	0	0	0	0	0	0	0	0	0	DC4_OK	DC3_OK	DC2_OK	DC1_OK	0000_0000_0000_0111
16527	408F	Power Good Source 2	0	0	0	0	0	0	1	1	1	LDO7_OK	1	LDO5_OK	LDO4_OK	LDO3_OK	LDO2_OK	LDO1_OK	0000_0011_1111_1111
16528	4090	Clock Control 1	CLKOUT_ENA	0	CLKOUT_OD	0	0	CLKOUT_SLOT[2:0]			0	CLKOUT_SLPSLOT[2:0]			0	0	0	CLKOUT_SRC	U000_0000_0000_0000
16529	4091	Clock Control 2	XTAL_INH	0	XTAL_ENA	XTAL_BKUPENA	0	0	0	0	FLL_AUTO	0	0	0	0	FLL_AUTO_FREQ[2:0]			0001_0000_1000_0000
16530	4092	FLL Control 1	0	0	0	0	0	0	0	0	0	0	0	0	0	FLL_FRAC	0	FLL_ENA	0000_0000_0000_0000
16531	4093	FLL Control 2	0	0	FLL_OUTDIV[5:0]						0	FLL_CTRL_RATE[2:0]			0	FLL_FRATIO[2:0]			0000_0000_0000_0000
16532	4094	FLL Control 3	FLL_K[15:0]																0000_0000_0000_0000
16533	4095	FLL Control 4	0	FLL_N[9:0]										0	FLL_GAIN[3:0]				0010_1110_1110_0000
16534	4096	FLL Control 5	0	0	0	0	0	0	0	0	0	0	0	FLL_CLK_REF_DIV[1:0]		0	FLL_CLK_SRC[1:0]		0000_0000_0000_0000
16535	4097	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
30720	7800	Unique ID 1	UNIQUE_ID[127:112]																0000_0000_0000_0000
30721	7801	Unique ID 2	UNIQUE_ID[111:96]																0000_0000_0000_0000
30722	7802	Unique ID 3	UNIQUE_ID[95:80]																0000_0000_0000_0000
30723	7803	Unique ID 4	UNIQUE_ID[79:64]																0000_0000_0000_0000
30724	7804	Unique ID 5	UNIQUE_ID[63:48]																0000_0000_0000_0000
30725	7805	Unique ID 6	UNIQUE_ID[47:32]																0000_0000_0000_0000
30726	7806	Unique ID 7	UNIQUE_ID[31:16]																0000_0000_0000_0000
30727	7807	Unique ID 8	UNIQUE_ID[15:0]																0000_0000_0000_0000
30728	7808	Factory OTP ID	OTP_FACT_ID[14:0]															OTP_FACT_FINAL	0000_0000_0000_0000
30729	7809	Factory OTP 1	DC3_TRIM[3:0]				DC2_TRIM[5:0]						DC1_TRIM[5:0]						0000_0000_0000_0000
30730	780A	Factory OTP 2	CHIP_ID[15:0]																0000_0000_0000_0000
30731	780B	Factory OTP 3	0	0	0	0	0	OSC_TRIM[3:0]				BG_TRIM[3:0]				LPBG_TRIM[2:0]			0000_0000_0000_0000
30732	780C	Factory OTP 4	0	0	0	0	0	0	0	0	CHILD_I2C_ADDR[6:0]							CH_AW	0000_0000_0000_0000
30733	780D	Factory OTP 5	0	0	0	0	0	0	0	0	0	0	CHARGE_TRIM[5:0]						0000_0000_0000_0000
30734	780E	Factory OTP 6	0	0	0	0	0	0	0	0	0	0	0	0	0	DC3_LIM_LOW	DC2_LIM_LOW	DC1_LIM_LOW	0000_0000_0000_0000
30735	780F	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30736	7810	Customer OTP ID	OTP_AUTO_PROG	OTP_CUST_ID[13:0]														OTP_CUST_FINAL	0000_0000_0000_0000
30737	7811	DC1 OTP Control	DC1_ON_SLOT[2:0]			0	0	0	DC1_FREQ[1:0]		DC1_PHASE	DC1_ON_VSEL[6:2]					DC1_CAP[1:0]		0000_0000_0000_0000
30738	7812	DC2 OTP Control	DC2_ON_SLOT[2:0]			0	0	0	DC2_FREQ[1:0]		DC2_PHASE	DC2_ON_VSEL[6:2]					DC2_CAP[1:0]		0000_0000_1000_0000
30739	7813	DC3 OTP Control	DC3_ON_SLOT[2:0]			0	0	0	0	0	DC3_PHASE	DC3_ON_VSEL[6:2]					DC3_CAP[1:0]		0000_0000_0000_0000
30740	7814	LDO1/2 OTP Control	LDO2_ON_SLOT[2:0]			LDO2_ON_VSEL[4:0]					LDO1_ON_SLOT[2:0]			LDO1_ON_VSEL[4:0]					0000_0000_0000_0000
30741	7815	LDO3/4 OTP Control	LDO4_ON_SLOT[2:0]			LDO4_ON_VSEL[4:0]					LDO3_ON_SLOT[2:0]			LDO3_ON_VSEL[4:0]					0000_0000_0000_0000
30742	7816	LDO5/6 OTP Control	0	0	0	0	0	0	0	0	LDO5_ON_SLOT[2:0]			LDO5_ON_VSEL[4:0]					0000_0000_0000_0000
30743	7817	LDO7/8 OTP Control	0	0	0	0	0	0	0	0	LDO7_ON_SLOT[2:0]			LDO7_ON_VSEL[4:0]					0000_0000_0000_0000
30744	7818	LDO9/10 OTP Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30745	7819	LDO11/EPE Control	LDO11_ON_SLOT[2:0]			0	LDO11_ON_VSEL[3:0]				EPE2_ON_SLOT[2:0]			EPE1_ON_SLOT[2:0]			USB100MA_STARTUP[1:0]		0000_0000_0000_0000
30746	781A	GPIO1 OTP Control	GP1_DIR	GP1_PULL[1:0]		GP1_INT_MODE	GP1_PWR_DOM	GP1_POL	GP1_OD	GP1_ENA	GP1_FN[3:0]				CLKOUT_SRC	XTAL_ENA	XTAL_INH	CHG_ENA	1010_0100_0000_0000
30747	781B	GPIO2 OTP Control	GP2_DIR	GP2_PULL[1:0]		GP2_INT_MODE	GP2_PWR_DOM	GP2_POL	GP2_OD	GP2_ENA	GP2_FN[3:0]				CLKOUT_SLOT[2:0]			WDOG_ENA	1010_0100_0000_0001
30748	781C	GPIO3 OTP Control	GP3_DIR	GP3_PULL[1:0]		GP3_INT_MODE	GP3_PWR_DOM	GP3_POL	GP3_OD	GP3_ENA	GP3_FN[3:0]				FLL_AUTO_FREQ[2:0]			0	1010_0100_0000_0000
30749	781D	GPIO4 OTP Control	GP4_DIR	GP4_PULL[1:0]		GP4_INT_MODE	GP4_PWR_DOM	GP4_POL	GP4_OD	GP4_ENA	GP4_FN[3:0]				LED1_SRC[1:0]		LED2_SRC[1:0]		1010_0100_0000_1111
30750	781E	GPIO5 OTP Control	GP5_DIR	GP5_PULL[1:0]		GP5_INT_MODE	GP5_PWR_DOM	GP5_POL	GP5_OD	GP5_ENA	GP5_FN[3:0]				USB_ILIM[2:0]			0	1010_0100_0000_0100
30751	781F	GPIO6 OTP Control	GP6_DIR	GP6_PULL[1:0]		GP6_INT_MODE	GP6_PWR_DOM	GP6_POL	GP6_OD	GP6_ENA	GP6_FN[3:0]				SYSOK_THR[2:0]			0	1010_0100_0000_1010

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bin Default
30752	**7820**	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30753	**7821**	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30754	**7822**	*Reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30755	**7823**	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0L0H_H0LL
30756	**7824**	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30757	**7825**	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30758	**7826**	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000_0000_0000_0000
30759	**7827**	ICE CHECK DATA	ICE_VALID_DATA[15:0]																0000_0000_0000_0000

29 REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Reset ID	15:0	CHIP_ID [15:0]	0000_0000_0000_0000	Writing to this register causes a Software Reset. The register map contents may be reset, depending on SW_RESET_CFG. Reading from this register will indicate Chip ID.	

Register 00h Reset ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R1 (01h) Revision	15:8	PARENT_REV [7:0]	0000_0000	The revision number of the parent die	
	7:0	CHILD_REV [7:0]	0000_0000	The revision number of the child die (when present)	

Register 01h Revision

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16384 (4000h) Parent ID	15:0	PARENT_ID [15:0]	0110_0010_0000_0100	The ID of the parent die	

Register 4000h Parent ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16385 (4001h) SYSVDD Control	15:14	SYSLO_ERR_ACT [1:0]	00	SYSLO Error Action Selects the action taken when SYSLO is asserted 00 = Interrupt 01 = WAKE transition 10 = Reserved 11 = OFF transition	
	11	SYSLO_STS	0	SYSLO Status 0 = Normal 1 = SYSVDD is below SYSLO threshold	
	6:4	SYSLO_THR [2:0]	010	SYSLO threshold (falling SYSVDD) This is the falling SYSVDD voltage at which SYSLO will be asserted 000 = 2.8V 001 = 2.9V … 111 = 3.5V	
	2:0	SYSOK_THR [2:0]	101	SYSOK threshold (rising SYSVDD) This is the rising SYSVDD voltage at which SYSOK will be asserted 000 = 2.8V 001 = 2.9V … 111 = 3.5V Note that the SYSOK hysteresis margin is added to these threshold levels.	

Register 4001h SYSVDD Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16386 (4002h) Thermal Monitoring	3	THW_HYST	1	Thermal Warning hysteresis 0 = 8 degrees C 1 = 16 degrees C	
	1:0	THW_TEMP [1:0]	10	Thermal Warning temperature 00 = 90 degrees C 01 = 100 degrees C 10 = 110 degrees C 11 = 120 degrees C	

Register 4002h Thermal Monitoring

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16387 (4003h) Power State	15	CHIP_ON	0	Indicates whether the system is ON or OFF. 0 = OFF 1 = ON (or SLEEP) OFF can be commanded by writing CHIP_ON = 0. Note that writing CHIP_ON = 1 is not a valid ‘ON’ event, and will not trigger an ON transition.	
	14	CHIP_SLP	0	Indicates whether the system is in the SLEEP state. 0 = Not in SLEEP 1 = SLEEP WAKE can be commanded by writing CHIP_SLP = 0. SLEEP can be commanded by writing CHIP_SLP = 1.	
	12	REF_LP	0	Low Power Voltage Reference Control 0 = Normal 1 = Low Power Reference Mode select Note that Low Power Reference Mode is only supported when the Touch Panel and Auxiliary ADC are both disabled.	
	11:10	PWRSTATE_DLY [1:0]	10	Power State transition delay 00 = No delay 01 = No delay 10 = 1ms 11 = 10ms	
	9	SWRST_DLY	0	Software Reset Delay 0 = No delay 1 = Software Reset is delayed by PWRSTATE_DLY following the Software Reset command	
	5:4	USB100MA_STARTUP [1:0]	00	Sets the device behaviour when starting up under USB power, when USB_ILIM = 010b (100mA) 00 = Normal 01 = Soft-Start 10 = Only start if BATTVDD > 3.1V 11 = Only start if BATTVDD > 3.4V In the 1X modes, if the battery voltage is less than the selected threshold, then the device will enable trickle charge mode instead of executing the start-up request. The start-up request is delayed until the battery voltage threshold has been met.	
	3	USB_CURR_STS	0	Indicates if the USB current limit has been reached 0 = Normal 1 = USB current limit	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	USB_ILIM [2:0]	010	Sets the USB current limit 000 = 0mA (USB switch is open) 001 = 2.5mA 010 = 100mA 011 = 500mA 100 = 900mA 101 = 1500mA 110 = 1800mA 111 = 550mA Note that, when starting up the WM8311 with the USBVDD supply selected, the USB_ILIM register must be set to 100mA or higher.	

Register 4003h Power State

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16388 (4004h) Watchdog	15	WDOG_ENA	1	Watchdog Timer Enable 0 = Disabled 1 = Enabled (enables the watchdog; does not reset it) *Protected by security key.*	
	14	WDOG_DEBUG	0	Watchdog Pause 0 = Disabled 1 = Enabled (halts the Watchdog timer for system debugging) *Protected by security key.*	
	13	WDOG_RST_SRC	1	Watchdog Reset Source 0 = Hardware only 1 = Software only *Protected by security key.*	
	12	WDOG_SLPENA	0	Watchdog SLEEP Enable 0 = Disabled 1 = Controlled by WDOG_ENA *Protected by security key.*	
	11	WDOG_RESET	0	Watchdog Software Reset 0 = Normal 1 = Watchdog Reset (resets the watchdog, if WDOG_RST_SRC = 1)	
	9:8	WDOG_SECACT [1:0]	10	Secondary action of Watchdog timeout (taken after 2 timeout periods) 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition *Protected by security key.*	
	5:4	WDOG_PRIMACT [1:0]	01	Primary action of Watchdog timeout 00 = No action 01 = Interrupt 10 = Device Reset 11 = WAKE transition *Protected by security key.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	WDOG_TO [2:0]	111	Watchdog timeout period 000 = 0.256s 001 = 0.512s 010 = 1.024s 011 = 2.048s 100 = 4.096s 101 = 8.192s 110 = 16.384s 111 = 32.768s *Protected by security key.*	

Register 4004h Watchdog

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16389 (4005h) ON Pin Control	9:8	ON_PIN_SECACT [1:0]	01	Secondary action of ON pin (taken after 1 timeout period) 00 = Interrupt 01 = ON request 10 = OFF request 11 = Reserved *Protected by security key.*	
	5:4	ON_PIN_PRIMACT [1:0]	00	Primary action of ON pin 00 = Ignore 01 = ON request 10 = OFF request 11 = Reserved Note that an Interrupt is always raised. *Protected by security key.*	
	3	ON_PIN_STS	0	Current status of ON pin 0 = Asserted (logic 0) 1 = Not asserted (logic 1)	
	1:0	ON_PIN_TO [1:0]	00	ON pin timeout period 00 = 1s 01 = 2s 10 = 4s 11 = 8s *Protected by security key.*	

Register 4005h ON Pin Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16390 (4006h) Reset Control	15	RECONFIG_AT_ON	1	Selects if the bootstrap configuration data should be reloaded when an ON transition is scheduled 0 = Disabled 1 = Enabled *Protected by security key.*	
	13	WALL_FET_ENA_DRV_STR	0	Sets the drive strength of the WALLFETENA pin. (Note this pin is Active Low.) 0 = Weak drive (500kOhm) 1 = Strong drive (50kOhm)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12	BATT_FET_ENA	0	Enables the FET gate functionality on the BATTFETENA pin. (Note this pin is Active Low.) 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.	
	10	SW_RESET_CFG	1	Software Reset Configuration. Selects whether the register map is reset to default values when Software Reset occurs. 0 = All registers except RTC and Software Scratch registers are reset by Software Reset 1 = Register Map is not affected by Software Reset *Protected by security key.*	
	6	AUXRST_SLPENA	1	Sets the output status of Auxiliary Reset (GPIO) function in SLEEP 0 = Auxiliary Reset not asserted 1 = Auxiliary Reset asserted *Protected by security key.*	
	5	RST_SLP_MSK	1	Masks the RESET pin input in SLEEP mode 0 = External RESET active in SLEEP 1 = External RESET masked in SLEEP *Protected by security key.*	
	4	RST_SLPENA	1	Sets the output status of RESET pin in SLEEP 0 = RESET high (not asserted) 1 = RESET low (asserted) *Protected by security key.*	
	1:0	RST_DUR [1:0]	11	Delay period for releasing RESET after ON or WAKE sequence 00 = 3ms 01 = 11ms 10 = 51ms 11 = 101ms *Protected by security key.*	

Register 4006h Reset Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16391 (4007h) Control Interface	2	AUTOINC	1	Enable Auto-Increment function 0 = Disabled 1 = Enabled	

Register 4007h Control Interface

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16392 (4008h) Security Key	15:0	SECURITY [15:0]	0000_0000_0000_0000	Security Key A value of 9716h must be written to this register to access the user-keyed registers.	

Register 4008h Security Key

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16393 (4009h) Software Scratch	15:0	SW_SCRATCH [15:0]	0000_0000_0000_0000	oftware Scratch Register for use by the host processor. Note that this register's contents are retained in the BACKUP power state.	

Register 4009h Software Scratch

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16394 (400Ah) OTP Control	15	OTP_PROG	0	Selects the PROGRAM device state. 0 = No action 1 = Select PROGRAM mode Note that, after PROGRAM mode has been selected, the chip will remain in PROGRAM mode until a Device Reset. *Protected by security key.*	
	13	OTP_MEM	1	Selects ICE or OTP memory for Program commands. 0 = ICE 1 = OTP *Protected by security key.*	
	11	OTP_FINAL	0	Selects the FINALISE command, preventing further OTP programming. 0 = No action 1 = Finalise Command *Protected by security key.*	
	10	OTP_VERIFY	0	Selects the VERIFY command for the selected OTP memory page(s). 0 = No action 1 = Verify Command *Protected by security key.*	
	9	OTP_WRITE	0	Selects WRITE command for the selected OTP memory page(s). 0 = No action 1 = Write Command *Protected by security key.*	
	8	OTP_READ	0	Selects READ command for the selected memory page(s). 0 = No action 1 = Read Command *Protected by security key.*	
	7:6	OTP_READ_LVL [1:0]	00	Selects the Margin Level for READ or VERIFY OTP commands. 00 = Normal 01 = Reserved 10 = Margin 1 11 = Margin 2 *Protected by security key.*	
	5	OTP_BULK	0	Selects the number of memory pages for ICE / OTP commands. 0 = Single Page 1 = All Pages	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	OTP_PAGE [1:0]	00	Selects the single memory page for ICE / OTP commands (when OTP_BULK=0). If OTP is selected (OTP_MEM = 1): 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 If ICE is selected (OTP_MEM = 0): 00 = Page 2 01 = Page 3 10 = Page 4 11 = Reserved	

Register 400Ah OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16396 (400Ch) GPIO Level	15	GP16_LVL	0	GPIO16 level. When GP16_FN = 0h and GP16_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP16_POL is 0, the register contains the opposite logic level to the external pin.	
	14	GP15_LVL	0	GPIO15 level. When GP15_FN = 0h and GP15_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP15_POL is 0, the register contains the opposite logic level to the external pin.	
	13	GP14_LVL	0	GPIO14 level. When GP14_FN = 0h and GP14_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP14_POL is 0, the register contains the opposite logic level to the external pin.	
	12	GP13_LVL	0	GPIO13 level. When GP13_FN = 0h and GP13_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP13_POL is 0, the register contains the opposite logic level to the external pin.	
	11	GP12_LVL	0	GPIO12 level. When GP12_FN = 0h and GP12_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP12_POL is 0, the register contains the opposite logic level to the external pin.	
	10	GP11_LVL	0	GPIO11 level. When GP11_FN = 0h and GP11_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP11_POL is 0, the register contains the opposite logic level to the external pin.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	9	GP10_LVL	0	GPIO10 level. When GP10_FN = 0h and GP10_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP10_POL is 0, the register contains the opposite logic level to the external pin.	
	8	GP9_LVL	0	GPIO9 level. When GP9_FN = 0h and GP9_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP9_POL is 0, the register contains the opposite logic level to the external pin.	
	7	GP8_LVL	0	GPIO8 level. When GP8_FN = 0h and GP8_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP8_POL is 0, the register contains the opposite logic level to the external pin.	
	6	GP7_LVL	0	GPIO7 level. When GP7_FN = 0h and GP7_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP7_POL is 0, the register contains the opposite logic level to the external pin.	
	5	GP6_LVL	0	GPIO6 level. When GP6_FN = 0h and GP6_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP6_POL is 0, the register contains the opposite logic level to the external pin.	
	4	GP5_LVL	0	GPIO5 level. When GP5_FN = 0h and GP5_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP5_POL is 0, the register contains the opposite logic level to the external pin.	
	3	GP4_LVL	0	GPIO4 level. When GP4_FN = 0h and GP4_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP4_POL is 0, the register contains the opposite logic level to the external pin.	
	2	GP3_LVL	0	GPIO3 level. When GP3_FN = 0h and GP3_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP3_POL is 0, the register contains the opposite logic level to the external pin.	
	1	GP2_LVL	0	GPIO2 level. When GP2_FN = 0h and GP2_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP2_POL is 0, the register contains the opposite logic level to the external pin.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	GP1_LVL	0	GPIO1 level. When GP1_FN = 0h and GP1_DIR = 0, write to this bit to set a GPIO output. Read from this bit to read GPIO input level. When GP1_POL is 0, the register contains the opposite logic level to the external pin.	

Register 400Ch GPIO Level

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16397 (400Dh) System Status	15	THW_STS	0	Thermal Warning status 0 = Normal 1 = Overtemperature Warning (warning temperature is set by THW_TEMP)	
	10	PWR_SRC_BATT	0	Battery Power Source status 0 = Battery is not supplying current 1 = Battery is supplying current	
	9	PWR_WALL	0	Wall Adaptor status 0 = Wall Adaptor voltage not present 1 = Wall Adaptor voltage is present	
	8	PWR_USB	0	USB status 0 = USB voltage not present 1 = USB voltage is present	
	4:0	MAIN_STATE [4:0]	0_0000	Main State Machine condition 0_0000 = OFF 0_0001 = ON_CHK 0_0010 = OTP_DN 0_0011 = READ_OTP 0_0100 = READ_ICE 0_0101 = ICE_DN 0_0110 = BGDELAY 0_0111 = HYST 0_1000 = S_PRG_RD_OTP 0_1001 = S_PRG_OTP_DN 0_1010 = PWRDN1 0_1011 = PROGRAM 0_1100 = PROG_DN 0_1101 = PROG_OTP 0_1110 = VFY_OTP 0_1111 = VFY_DN 1_0000 = SD_RD_OTP 1_0001 = UNUSED 1_0010 = ICE_FAIL 1_0011 = SHUTDOWN 1_0100 = STARTFAIL 1_0101 = STARTUP 1_0110 = PREACTIVE 1_0111 = XTAL_CHK 1_1000 = PWRDN2 1_1001 = SHUT_DLY 1_1010 = RESET 1_1011 = RESET_DLY	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1_1100 = SLEEP 1_1101 = SLEEP_DLY 1_1110 = CHK_RST 1_1111 = ACTIVE (ON)	

Register 400Dh System Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16398 (400Eh) ON Source	15	ON_TRANS	0	Most recent ON/WAKE event type 0 = WAKE transition 1 = ON transition *Reset by state machine.*	
	11	ON_GPIO	0	Most recent ON/WAKE event type 0 = Not caused by GPIO input 1 = Caused by GPIO input *Reset by state machine.*	
	10	ON_SYSLO	0	Most recent WAKE event type 0 = Not caused by SYSVDD 1 = Caused by SYSLO threshold. Note that the SYSLO threshold cannot trigger an ON event. *Reset by state machine.*	
	9	ON_PEN_DOWN	0	Most recent WAKE event type 0 = Not caused by Pen Down 1 = Caused by Touch Panel Pen Down detection. Note that the Pen Down detection cannot trigger an ON event. *Reset by state machine.*	
	8	ON_CHG	0	Most recent WAKE event type 0 = Not caused by Battery Charger 1 = Caused by Battery Charger TBC if this could cause ON due to Charger plugged in? *Reset by state machine.*	
	7	ON_WDOG_TO	0	Most recent WAKE event type 0 = Not caused by Watchdog timer 1 = Caused by Watchdog timer *Reset by state machine.*	
	6	ON_SW_REQ	0	Most recent WAKE event type 0 = Not caused by software WAKE 1 = Caused by software WAKE command (CHIP_SLP = 0) *Reset by state machine.*	
	5	ON_RTC_ALM	0	Most recent ON/WAKE event type 0 = Not caused by RTC Alarm 1 = Caused by RTC Alarm *Reset by state machine.*	
	4	ON_ON_PIN	0	Most recent ON/WAKE event type 0 = Not caused by the ON pin 1 = Caused by the ON pin *Reset by state machine.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	RESET_CNV_UV	0	Most recent ON event type 0 = Not caused by undervoltage 1 = Caused by a Device Reset due to a Converter (LDO or DC-DC) undervoltage condition *Reset by state machine.*	
	2	RESET_SW	0	Most recent ON event type 0 = Not caused by Software Reset 1 = Caused by Software Reset *Reset by state machine.*	
	1	RESET_HW	0	Most recent ON event type 0 = Not caused by Hardware Reset 1 = Caused by Hardware Reset *Reset by state machine.*	
	0	RESET_WDOG	0	Most recent ON event type 0 = Not caused by the Watchdog 1 = Caused by a Device Reset triggered by the Watchdog timer *Reset by state machine.*	

Register 400Eh ON Source

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16399 (400Fh) OFF Source	13	OFF_INTLDO_ERR	0	Most recent OFF event type 0 = Not caused by LDO13 Error condition 1 = Caused by LDO13 Error condition *Reset by state machine.*	
	12	OFF_PWR_SEQ	0	Most recent OFF event type 0 = Not caused by Power Sequence Failure 1 = Caused by a Power Sequence Failure *Reset by state machine.*	
	11	OFF_GPIO	0	Most recent OFF event type 0 = Not caused by GPIO input 1 = Caused by GPIO input *Reset by state machine.*	
	10	OFF_SYSVDD	0	Most recent OFF event type 0 = Not caused by SYSVDD 1 = Caused by the SYSLO or SHUTDOWN threshold *Reset by state machine.*	
	9	OFF_THERR	0	Most recent OFF event type 0 = Not caused by temperature 1 = Caused by over-temperature *Reset by state machine.*	
	6	OFF_SW_REQ	0	Most recent OFF event type 0 = Not caused by software OFF 1 = Caused by software OFF command (CHIP_ON = 0) *Reset by state machine.*	
	4	OFF_ON_PIN	0	Most recent OFF event type 0 = Not caused by the ON pin 1 = Caused by the ON pin *Reset by state machine.*	

Register 400Fh OFF Source

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16400 (4010h) System Interrupts	15	PS_INT	0	Power State primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	14	TEMP_INT	0	Thermal primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	13	GP_INT	0	GPIO primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	12	ON_PIN_INT	0	ON Pin primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	11	WDOG_INT	0	Watchdog primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	10	TCHDATA_INT	0	Touch Panel Data primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	9	TCHPD_INT	0	Touch Panel Pen Down primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	8	AUXADC_INT	0	AUXADC primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	7	PPM_INT	0	Power Path Management primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	6	CS_INT	0	Current Sink primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	5	RTC_INT	0	Real Time Clock primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	4	OTP_INT	0	OTP Memory primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	2	CHG_INT	0	Battery Charger primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	1	HC_INT	0	High Current primary interrupt 0 = No interrupt 1 = Interrupt is asserted	
	0	UV_INT	0	Undervoltage primary interrupt 0 = No interrupt 1 = Interrupt is asserted	

Register 4010h System Interrupts

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
R16401 (4011h) Interrupt Status 1	15	PPM_SYSLO_EINT	0	Power Path SYSLO interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	14	PPM_PWR_SRC_EINT	0	Power Path Source interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	13	PPM_USB_CURR_EINT	0	Power Path USB Current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	12	ON_PIN_CINT	0	ON pin interrupt. (Rising and Falling Edge triggered) Note: Cleared when a ‘1’ is written.	
	11	WDOG_TO_EINT	0	Watchdog timeout interrupt. (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	10	TCHDATA_EINT	0	Touch panel Data interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	9	TCHPD_EINT	0	Touch panel Pen Down interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	8	AUXADC_DATA_EINT	0	AUXADC Data Ready interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	7	AUXADC_DCOMP4_EINT	0	AUXADC Digital Comparator 4 interrupt (Trigger is controlled by DCMP4_GT) Note: Cleared when a ‘1’ is written.	
	6	AUXADC_DCOMP3_EINT	0	AUXADC Digital Comparator 3 interrupt (Trigger is controlled by DCMP3_GT) Note: Cleared when a ‘1’ is written.	
	5	AUXADC_DCOMP2_EINT	0	AUXADC Digital Comparator 2 interrupt (Trigger is controlled by DCMP2_GT) Note: Cleared when a ‘1’ is written.	
	4	AUXADC_DCOMP1_EINT	0	AUXADC Digital Comparator 1 interrupt (Trigger is controlled by DCMP1_GT) Note: Cleared when a ‘1’ is written.	
	3	RTC_PER_EINT	0	RTC Periodic interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	2	RTC_ALM_EINT	0	RTC Alarm interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	1	TEMP_THW_CINT	0	Thermal Warning interrupt (Rising and Falling Edge triggered) Note: Cleared when a ‘1’ is written.	

Register 4011h Interrupt Status 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16402 (4012h) Interrupt Status 2	15	CHG_BATT_HOT_EINT	0	Battery Hot interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	14	CHG_BATT_COLD_EINT	0	Battery Cold interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	13	CHG_BATT_FAIL_EINT	0	Battery Fail interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	12	CHG_OV_EINT	0	Battery Overvoltage interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	11	CHG_END_EINT	0	Battery Charge End interrupt (End of Charge Current threshold reached) (Rising Edge triggered) Note: Cleared when a '1' is written.	
	10	CHG_TO_EINT	0	Battery Charge Timeout interrupt (Charger Timer has expired) (Rising Edge triggered) Note: Cleared when a '1' is written.	
	9	CHG_MODE_EINT	0	Battery Charge Mode interrupt (Charger Mode has changed) (Rising Edge triggered) Note: Cleared when a '1' is written.	
	8	CHG_START_EINT	0	Battery Charge Start interrupt (Charging has started) (Rising Edge triggered) Note: Cleared when a '1' is written.	
	7	CS2_EINT	0	Current Sink 2 interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	6	CS1_EINT	0	Current Sink 1 interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	5	OTP_CMD_END_EINT	0	OTP / ICE Command End interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	4	OTP_ERR_EINT	0	OTP / ICE Command Fail interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	2	PS_POR_EINT	0	Power On Reset interrupt (Rising Edge triggered) Note: Cleared when a '1' is written.	
	1	PS_SLEEP_OFF_EINT	0	SLEEP or OFF interrupt (Power state transition to SLEEP or OFF states) (Rising Edge triggered) Note: Cleared when a '1' is written.	
	0	PS_ON_WAKE_EINT	0	ON or WAKE interrupt (Power state transition to ON state) (Rising Edge triggered) Note: Cleared when a '1' is written.	

Register 4012h Interrupt Status 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16403 (4013h) Interrupt Status 3	6	UV_LDO7_EINT	0	LDO7 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	4	UV_LDO5_EINT	0	LDO5 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	3	UV_LDO4_EINT	0	LDO4 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	2	UV_LDO3_EINT	0	LDO3 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	1	UV_LDO2_EINT	0	LDO2 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	0	UV_LDO1_EINT	0	LDO1 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	

Register 4013h Interrupt Status 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16404 (4014h) Interrupt Status 4	9	HC_DC2_EINT	0	DC-DC2 High current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	8	HC_DC1_EINT	0	DC-DC1 High current interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	3	UV_DC4_EINT	0	DC-DC4 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	2	UV_DC3_EINT	0	DC-DC3 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	1	UV_DC2_EINT	0	DC-DC2 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	
	0	UV_DC1_EINT	0	DC-DC1 Undervoltage interrupt (Rising Edge triggered) Note: Cleared when a ‘1’ is written.	

Register 4014h Interrupt Status 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16405 (4015h) Interrupt Status 5	15	GP16_EINT	0	GPIO16 interrupt. (Trigger is controlled by GP16_INT_MODE) Note: Cleared when a ‘1’ is written.	
	14	GP15_EINT	0	GPIO15 interrupt. (Trigger is controlled by GP15_INT_MODE) Note: Cleared when a ‘1’ is written.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	13	GP14_EINT	0	GPIO14 interrupt. (Trigger is controlled by GP14_INT_MODE) Note: Cleared when a ‘1’ is written.	
	12	GP13_EINT	0	GPIO13 interrupt. (Trigger is controlled by GP13_INT_MODE) Note: Cleared when a ‘1’ is written.	
	11	GP12_EINT	0	GPIO12 interrupt. (Trigger is controlled by GP12_INT_MODE) Note: Cleared when a ‘1’ is written.	
	10	GP11_EINT	0	GPIO11 interrupt. (Trigger is controlled by GP11_INT_MODE) Note: Cleared when a ‘1’ is written.	
	9	GP10_EINT	0	GPIO10 interrupt. (Trigger is controlled by GP10_INT_MODE) Note: Cleared when a ‘1’ is written.	
	8	GP9_EINT	0	GPIO9 interrupt. (Trigger is controlled by GP9_INT_MODE) Note: Cleared when a ‘1’ is written.	
	7	GP8_EINT	0	GPIO8 interrupt. (Trigger is controlled by GP8_INT_MODE) Note: Cleared when a ‘1’ is written.	
	6	GP7_EINT	0	GPIO7 interrupt. (Trigger is controlled by GP7_INT_MODE) Note: Cleared when a ‘1’ is written.	
	5	GP6_EINT	0	GPIO6 interrupt. (Trigger is controlled by GP6_INT_MODE) Note: Cleared when a ‘1’ is written.	
	4	GP5_EINT	0	GPIO5 interrupt. (Trigger is controlled by GP5_INT_MODE) Note: Cleared when a ‘1’ is written.	
	3	GP4_EINT	0	GPIO4 interrupt. (Trigger is controlled by GP4_INT_MODE) Note: Cleared when a ‘1’ is written.	
	2	GP3_EINT	0	GPIO3 interrupt. (Trigger is controlled by GP3_INT_MODE) Note: Cleared when a ‘1’ is written.	
	1	GP2_EINT	0	GPIO2 interrupt. (Trigger is controlled by GP2_INT_MODE) Note: Cleared when a ‘1’ is written.	
	0	GP1_EINT	0	GPIO1 interrupt. (Trigger is controlled by GP1_INT_MODE) Note: Cleared when a ‘1’ is written.	

Register 4015h Interrupt Status 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16407 (4017h) IRQ Config	1	IRQ_OD	1	IRQ pin configuration 0 = CMOS 1 = Open Drain (integrated pull-up)	
	0	IM_IRQ	0	IRQ pin output mask 0 = Normal 1 = IRQ output is masked	

Register 4017h IRQ Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16408 (4018h) System Interrupts Mask	15	IM_PS_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	14	IM_TEMP_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	13	IM_GP_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	12	IM_ON_PIN_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	11	IM_WDOG_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	10	IM_TCHDATA_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	9	IM_TCHPD_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_AUXADC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_PPM_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	6	IM_CS_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	5	IM_RTC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	IM_OTP_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_CHILD_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_CHG_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_HC_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_UV_INT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 4018h System Interrupts Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16409 (4019h) Interrupt Status 1 Mask	15	IM_PPM_SYSLO_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	14	IM_PPM_PWR_SRC_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	13	IM_PPM_USB_CURR_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	12	IM_ON_PIN_CINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	11	IM_WDOG_TO_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	10	IM_TCHDATA_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	9	IM_TCHPD_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	8	IM_AUXADC_DATA_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_AUXADC_DCOMP4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	6	IM_AUXADC_DCOMP3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	5	IM_AUXADC_DCOMP2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	4	IM_AUXADC_DCOMP1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_RTC_PER_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_RTC_ALM_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_TEMP_THW_CINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 4019h Interrupt Status 1 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16410 (401Ah) Interrupt Status 2 Mask	15	IM_CHG_BATT_HOT_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	14	IM_CHG_BATT_COLD_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	13	IM_CHG_BATT_FAIL_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	12	IM_CHG_OV_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	11	IM_CHG_END_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	10	IM_CHG_TO_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	9	IM_CHG_MODE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_CHG_START_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_CS2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	6	IM_CS1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	5	IM_OTP_CMD_END_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	4	IM_OTP_ERR_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_PS_POR_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_PS_SLEEP_OFF_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_PS_ON_WAKE_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Ah Interrupt Status 2 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16411 (401Bh) Interrupt Status 3 Mask	6	IM_UV_LDO7_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	4	IM_UV_LDO5_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_UV_LDO4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_UV_LDO3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_UV_LDO2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_UV_LDO1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Bh Interrupt Status 3 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16412 (401Ch) Interrupt Status 4 Mask	9	IM_HC_DC2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_HC_DC1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_UV_DC4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_UV_DC3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_UV_DC2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	IM_UV_DC1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Ch Interrupt Status 4 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16413 (401Dh) Interrupt Status 5 Mask	15	IM_GP16_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	14	IM_GP15_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	13	IM_GP14_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	12	IM_GP13_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	11	IM_GP12_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	10	IM_GP11_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	9	IM_GP10_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	8	IM_GP9_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	7	IM_GP8_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	6	IM_GP7_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	IM_GP6_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	4	IM_GP5_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	3	IM_GP4_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	2	IM_GP3_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	1	IM_GP2_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	
	0	IM_GP1_EINT	1	Interrupt mask. 0 = Do not mask interrupt. 1 = Mask interrupt. Default value is 1 (masked)	

Register 401Dh Interrupt Status 5 Mask

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16416 (4020h) RTC Write Counter	15:0	RTC_WR_CNT [15:0]	0000_0000_0000_0000	RTC Write Counter. This random number is updated on every write to the RTC_TIME registers.	

Register 4020h RTC Write Counter

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16417 (4021h) RTC Time 1	15:0	RTC_TIME [15:0]	0000_0000_0000_0000	RTC Seconds counter (MSW) RTC_TIME increments by 1 every second. This is the 16 MSBs.	

Register 4021h RTC Time 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16418 (4022h) RTC Time 2	15:0	RTC_TIME [15:0]	0000_0000_0000_0000	RTC Seconds counter (LSW) RTC_TIME increments by 1 every second. This is the 16 LSBs.	

Register 4022h RTC Time 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16419 (4023h) RTC Alarm 1	15:0	RTC_ALM [15:0]	0000_0000_0000_0000	RTC Alarm time (MSW) 16 MSBs of RTC_ALM	

Register 4023h RTC Alarm 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16420 (4024h) RTC Alarm 2	15:0	RTC_ALM [15:0]	0000_0000_0000_0000	RTC Alarm time (LSW) 16 LSBs of RTC_ALM	

Register 4024h RTC Alarm 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16421 (4025h) RTC Control	15	RTC_VALID	0	RTC Valid status 0 = RTC_TIME has not been set since Power On Reset 1 = RTC_TIME has been written to since Power On Reset	
	14	RTC_SYNC_BUSY	0	RTC Busy status 0 = Normal 1 = Busy The RTC registers should not be written to when RTC_SYNC_BUSY = 1.	
	10	RTC_ALM_ENA	0	RTC Alarm Enable 0 = Disabled 1 = Enabled	
	6:4	RTC_PINT_FREQ [2:0]	000	RTC Periodic Interrupt timeout period 000 = Disabled 001 = 2s 010 = 4s 011 = 8s 100 = 16s 101 = 32s 110 = 64s 111 = 128s	

Register 4025h RTC Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16422 (4026h) RTC Trim	9:0	RTC_TRIM [9:0]	00_0000_0000	RTC frequency trim. Value is a 10bit fixed point <4,6> 2's complement number. MSB Scaling = -8Hz. The register indicates the error (in Hz) with respect to the ideal 32768Hz) of the input crystal frequency. *Protected by security key.*	

Register 4026h RTC Trim

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
R16424 (4028h) Touch Control 1	15	TCH_ENA	0	Touch Panel Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.	
	14	TCH_CVT_ENA	0	Touch Panel Conversion Enable 0 = Disabled 1 = Enabled In automatic mode, conversions are enabled by setting this bit. In manual mode (TCH_RATE = 0), setting this bit will initiate a set of conversion; the bit is reset automatically after each set of measurements.	
	12	TCH_SLPENA	0	Touch Panel SLEEP Enable 0 = Disabled 1 = Controlled by TCH_ENA	
	10	TCH_Z_ENA	0	Enables Z-axis touch panel measurements. (Z-axis is the pressure axis - 4-wire only.) 0 = Disabled 1 = Enabled	
	9	TCH_Y_ENA	0	Enables Y-axis touch panel measurements 0 = Disabled 1 = Enabled	
	8	TCH_X_ENA	0	Enables X-axis touch panel measurements 0 = Disabled 1 = Enabled	
	7:5	TCH_DELAY [2:0]	010	Settling time between X, Y and Z measurements. (Nominal timing only; typically +/-20% of quoted values.) 000 = 30us 001 = 60us 010 = 120us 011 = 240us 100 = 480us 101 = 960us 110 = 1920us 111 = 3840us	
	4:0	TCH_RATE [4:0]	0_0000	Touch-panel Conversion Rate 0 = Manual 1 = 16 packets/s 2 = 32 packets/s 3 = 48 packets/s … 31 = 496 packets/s	

Register 4028h Touch Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16425 (4029h) Touch Control 2	13	TCH_PD_WK	0	WAKE transition select for Pen Down event 0 = Disabled 1 = Enabled	
	12	TCH_5WIRE	0	Touch Panel control mode 0 = 4-wire 1 = 5-wire	
	11	TCH_PDONLY	0	Select Automatic conversions only when Pen Down is detected. (No effect on Manual conversion.) 0 = Normal 1 = Pen-Down only	
	8	TCH_ISEL	0	Pressure measurement current select 0 = 200uA 1 = 400uA Note - this applies to 4-wire mode only	
	3:0	TCH_RPU [3:0]	0111	Pen-Down sensitivity (pull-up resistor) 0000 = 64k (most sensitive) 0001 = 64k / 2 0010 = 64k / 3 0011 = 64k / 4 …. 1111 = 64k / 16 (least sensitive)	

Register 4029h Touch Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16426 (402Ah) Touch Data X	15	TCH_PD1	0	Pen down status (indicates if the Pen Down was detected prior to the TP measurement) 0 = Pen Down not detected 1 = Pen Down detected	
	11:0	TCH_X [11:0]	0000_0000_0000	Touch panel X-axis data (12-bit unsigned binary number)	

Register 402Ah Touch Data X

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16427 (402Bh) Touch Data Y	15	TCH_PD2	0	Pen down status (indicates if the Pen Down was detected prior to the TP measurement) 0 = Pen Down not detected 1 = Pen Down detected	
	11:0	TCH_Y [11:0]	0000_0000_0000	Touch panel Y-axis data (12-bit unsigned binary number)	

Register 402Bh Touch Data Y

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16428 (402Ch) Touch Data Z	15	TCH_PD3	0	Pen down status (indicates if the Pen Down was detected prior to the TP measurement) 0 = Pen Down not detected 1 = Pen Down detected	
	11:0	TCH_Z [11:0]	0000_0000_0000	Touch panel Z-axis data (12-bit unsigned binary number)	

Register 402Ch Touch Data Z

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16429 (402Dh) AuxADC Data	15:12	AUX_DATA_SRC [3:0]	0000	AUXADC Data Source 0 = Reserved 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage 8 = USB voltage 9 = BATT voltage 10 = WALL voltage 11 = Reserved 12 = Reserved 13 = Reserved 14 = Reserved 15 = Reserved	
	11:0	AUX_DATA [11:0]	0000_0000_0000	AUXADC Measurement Data Voltage (mV) = AUX_DATA x 1.465 ChipTemp (°C) = (498 - AUX_DATA) / 1.09 BattTemp (°C) = (value is dependent on NTC thermistor)	

Register 402Dh AuxADC Data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16430 (402Eh) AuxADC Control	15	AUX_ENA	0	AUXADC Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.	
	14	AUX_CVT_ENA	0	AUXADC Conversion Enable 0 = Disabled 1 = Enabled In automatic mode, conversions are enabled by setting this bit. In manual mode (AUX_RATE = 0), setting this bit will initiate a conversion; the bit is reset automatically after each conversion.	
	12	AUX_SLPENA	0	AUXADC SLEEP Enable 0 = Disabled 1 = Controlled by AUX_ENA	

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
	5:0	AUX_RATE [5:0]	00_0000	AUXADC Conversion Rate 0 = Manual 1 = 2 samples/s 2 = 4 samples/s 3 = 6 samples/s … 31 = 62 samples/s 32 = Reserved 33 = 16 samples/s 34 = 32 samples/s 35 = 48 samples/s … 63 = 496 samples/s	

Register 402Eh AuxADC Control

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
R16431 (402Fh) AuxADC Source	9	AUX_WALL_SEL	0	AUXADC WALL input select 0 = Disable WALLVDD measurement 1 = Enable WALLVDD measurement	
	8	AUX_BATT_SEL	0	AUXADC BATT input select 0 = Disable BATTVDD measurement 1 = Enable BATTVDD measurement	
	7	AUX_USB_SEL	0	AUXADC USB input select 0 = Disable USBVDD measurement 1 = Enable USBVDD measurement	
	6	AUX_SYSVDD_SEL	0	AUXADC SYSVDD input select 0 = Disable SYSVDD measurement 1 = Enable SYSVDD measurement	
	5	AUX_BATT_TEMP_SEL	0	AUXADC Battery Temp input select 0 = Disable Battery Temp measurement 1 = Enable Battery Temp measurement	
	4	AUX_CHIP_TEMP_SEL	0	AUXADC Chip Temp input select 0 = Disable Chip Temp measurement 1 = Enable Chip Temp measurement	
	3	AUX_AUX4_SEL	0	AUXADCIN4 input select 0 = Disable AUXADCIN4 measurement 1 = Enable AUXADCIN4 measurement	
	2	AUX_AUX3_SEL	0	AUXADCIN3 input select 0 = Disable AUXADCIN3 measurement 1 = Enable AUXADCIN3 measurement	
	1	AUX_AUX2_SEL	0	AUXADCIN2 input select 0 = Disable AUXADCIN2 measurement 1 = Enable AUXADCIN2 measurement	
	0	AUX_AUX1_SEL	0	AUXADCIN1 input select 0 = Disable AUXADCIN1 measurement 1 = Enable AUXADCIN1 measurement	

Register 402Fh AuxADC Source

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16432 (4030h) Comparator Control	11	DCOMP4_STS	0	Digital Comparator 4 status 0 = Comparator 4 threshold not detected 1 = Comparator 4 threshold detected (Trigger is controlled by DCMP4_GT)	
	10	DCOMP3_STS	0	Digital Comparator 3 status 0 = Comparator 3 threshold not detected 1 = Comparator 3 threshold detected (Trigger is controlled by DCMP3_GT)	
	9	DCOMP2_STS	0	Digital Comparator 2 status 0 = Comparator 2 threshold not detected 1 = Comparator 2 threshold detected (Trigger is controlled by DCMP2_GT)	
	8	DCOMP1_STS	0	Digital Comparator 1 status 0 = Comparator 1 threshold not detected 1 = Comparator 1 threshold detected (Trigger is controlled by DCMP1_GT)	
	3	DCMP4_ENA	0	Digital Comparator 4 Enable 0 = Disabled 1 = Enabled	
	2	DCMP3_ENA	0	Digital Comparator 3 Enable 0 = Disabled 1 = Enabled	
	1	DCMP2_ENA	0	Digital Comparator 2 Enable 0 = Disabled 1 = Enabled	
	0	DCMP1_ENA	0	Digital Comparator 1 Enable 0 = Disabled 1 = Enabled	

Register 4030h Comparator Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16433 (4031h) Comparator 1	15:13	DCMP1_SRC [2:0]	000	Digital Comparator 1 source select 0 = USB voltage 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage	
	12	DCMP1_GT	0	Digital Comparator 1 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than threshold	
	11:0	DCMP1_THR [11:0]	0000_0000_0000	Digital Comparator 1 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4031h Comparator 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16434 (4032h) Comparator 2	15:13	DCMP2_SRC [2:0]	000	Digital Comparator 2 source select 0 = WALL voltage 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage	
	12	DCMP2_GT	0	Digital Comparator 2 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than threshold	
	11:0	DCMP2_THR [11:0]	0000_0000 _0000	Digital Comparator 2 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4032h Comparator 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16435 (4033h) Comparator 3	15:13	DCMP3_SRC [2:0]	000	Digital Comparator 3 source select 0 = BATT voltage 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage	
	12	DCMP3_GT	0	Digital Comparator 3 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than threshold	
	11:0	DCMP3_THR [11:0]	0000_0000 _0000	Digital Comparator 3 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4033h Comparator 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16436 (4034h) Comparator 4	15:13	DCMP4_SRC [2:0]	000	Digital Comparator 4 source select 0 = Reserved 1 = AUXADCIN1 2 = AUXADCIN2 3 = AUXADCIN3 4 = AUXADCIN4 5 = Chip Temperature 6 = Battery Temperature 7 = SYSVDD voltage	
	12	DCMP4_GT	0	Digital Comparator 4 interrupt control 0 = interrupt when less than threshold 1 = interrupt when greater than threshold	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	11:0	DCMP4_THR [11:0]	0000_0000_0000	Digital Comparator 4 threshold (12-bit unsigned binary number; coding is the same as AUX_DATA)	

Register 4034h Comparator 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16440 (4038h) GPIO1 Control	15	GP1_DIR	1	GPIO1 pin direction 0 = Output 1 = Input	
	14:13	GP1_PULL [1:0]	01	GPIO1 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP1_INT_MODE	0	GPIO1 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP1_POL=1) or falling edge triggered (if GP1_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP1_PWR_DOM	0	GPIO1 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP1_POL	1	GPIO1 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP1_OD	0	GPIO1 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP1_ENA	0	GPIO1 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP1_FN [3:0]	0000	GPIO1 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions:	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4038h GPIO1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16441 (4039h) GPIO2 Control	15	GP2_DIR	1	GPIO2 pin direction 0 = Output 1 = Input	
	14:13	GP2_PULL [1:0]	01	GPIO2 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP2_INT_MODE	0	GPIO2 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP2_POL=1) or falling edge triggered (if GP2_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP2_PWR_DOM	0	GPIO2 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP2_POL	1	GPIO2 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP2_OD	0	GPIO2 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP2_ENA	0	GPIO2 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP2_FN [3:0]	0000	GPIO2 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4039h GPIO2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16442 (403Ah) GPIO3 Control	15	GP3_DIR	1	GPIO3 pin direction 0 = Output 1 = Input	
	14:13	GP3_PULL [1:0]	01	GPIO3 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP3_INT_MODE	0	GPIO3 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP3_POL=1) or falling edge triggered (if GP3_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP3_PWR_DOM	0	GPIO3 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP3_POL	1	GPIO3 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	9	GP3_OD	0	GPIO3 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP3_ENA	0	GPIO3 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP3_FN [3:0]	0000	GPIO3 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Ah GPIO3 Control

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
R16443 (403Bh) GPIO4 Control	15	GP4_DIR	1	GPIO4 pin direction 0 = Output 1 = Input	
	14:13	GP4_PULL [1:0]	01	GPIO4 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP4_INT_MODE	0	GPIO4 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP4_POL=1) or falling edge triggered (if GP4_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP4_PWR_DOM	0	GPIO4 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP4_POL	1	GPIO4 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP4_OD	0	GPIO4 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP4_ENA	0	GPIO4 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP4_FN [3:0]	0000	GPIO4 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Bh GPIO4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16444 (403Ch) GPIO5 Control	15	GP5_DIR	1	GPIO5 pin direction 0 = Output 1 = Input	
	14:13	GP5_PULL [1:0]	01	GPIO5 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP5_INT_MODE	0	GPIO5 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP5_POL=1) or falling edge triggered (if GP5_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP5_PWR_DOM	0	GPIO5 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP5_POL	1	GPIO5 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP5_OD	0	GPIO5 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP5_ENA	0	GPIO5 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP5_FN [3:0]	0000	GPIO5 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Ch GPIO5 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16445 (403Dh) GPIO6 Control	15	GP6_DIR	1	GPIO6 pin direction 0 = Output 1 = Input	
	14:13	GP6_PULL [1:0]	01	GPIO6 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP6_INT_MODE	0	GPIO6 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP6_POL=1) or falling edge triggered (if GP6_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP6_PWR_DOM	0	GPIO6 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP6_POL	1	GPIO6 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP6_OD	0	GPIO6 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP6_ENA	0	GPIO6 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	GP6_FN [3:0]	0000	GPIO6 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Dh GPIO6 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16446 (403Eh) GPIO7 Control	15	GP7_DIR	1	GPIO7 pin direction 0 = Output 1 = Input	
	14:13	GP7_PULL [1:0]	01	GPIO7 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP7_INT_MODE	0	GPIO7 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP7_POL=1) or falling edge triggered (if GP7_POL=0) 1 = GPIO interrupt is triggered on rising and falling	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				edges	
	11	GP7_PWR_DOM	0	GPIO7 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP7_POL	1	GPIO7 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP7_OD	0	GPIO7 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP7_ENA	0	GPIO7 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP7_FN [3:0]	0000	GPIO7 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Eh GPIO7 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16447 (403Fh) GPIO8 Control	15	GP8_DIR	1	GPIO8 pin direction 0 = Output 1 = Input	
	14:13	GP8_PULL [1:0]	01	GPIO8 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP8_INT_MODE	0	GPIO8 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP8_POL=1) or falling edge triggered (if GP8_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP8_PWR_DOM	0	GPIO8 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP8_POL	1	GPIO8 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP8_OD	0	GPIO8 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP8_ENA	0	GPIO8 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP8_FN [3:0]	0000	GPIO8 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 403Fh GPIO8 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16448 (4040h) GPIO9 Control	15	GP9_DIR	1	GPIO9 pin direction 0 = Output 1 = Input	
	14:13	GP9_PULL [1:0]	01	GPIO9 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP9_INT_MODE	0	GPIO9 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP9_POL=1) or falling edge triggered (if GP9_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP9_PWR_DOM	0	GPIO9 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP9_POL	1	GPIO9 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP9_OD	0	GPIO9 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP9_ENA	0	GPIO9 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP9_FN [3:0]	0000	GPIO9 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4040h GPIO9 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16449 (4041h) GPIO10 Control	15	GP10_DIR	1	GPIO10 pin direction 0 = Output 1 = Input	
	14:13	GP10_PULL [1:0]	01	GPIO10 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP10_INT_MODE	0	GPIO10 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP10_POL=1) or falling edge triggered (if GP10_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP10_PWR_DOM	0	GPIO10 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP10_POL	1	GPIO10 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP10_OD	0	GPIO10 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP10_ENA	0	GPIO10 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	GP10_FN [3:0]	0000	GPIO10 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4041h GPIO10 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16450 (4042h) GPIO11 Control	15	GP11_DIR	1	GPIO11 pin direction 0 = Output 1 = Input	
	14:13	GP11_PULL [1:0]	01	GPIO11 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12	GP11_INT_MODE	0	GPIO11 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP11_POL=1) or falling edge triggered (if GP11_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP11_PWR_DOM	0	GPIO11 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP11_POL	1	GPIO11 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP11_OD	0	GPIO11 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP11_ENA	0	GPIO11 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP11_FN [3:0]	0000	GPIO11 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz)	

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
				15 = Auxiliary Reset	

Register 4042h GPIO11 Control

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
R16451 (4043h) GPIO12 Control	15	GP12_DIR	1	GPIO12 pin direction 0 = Output 1 = Input	
	14:13	GP12_PULL [1:0]	01	GPIO12 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP12_INT_MODE	0	GPIO12 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP12_POL=1) or falling edge triggered (if GP12_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP12_PWR_DOM	0	GPIO12 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP12_POL	1	GPIO12 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP12_OD	0	GPIO12 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP12_ENA	0	GPIO12 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	GP12_FN [3:0]	0000	GPIO12 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4043h GPIO12 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16452 (4044h) GPIO13 Control	15	GP13_DIR	1	GPIO13 pin direction 0 = Output 1 = Input	
	14:13	GP13_PULL [1:0]	01	GPIO13 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP13_INT_MODE	0	GPIO13 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP13_POL=1) or falling edge triggered (if GP13_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10	GP13_POL	1	GPIO13 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP13_OD	0	GPIO13 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP13_ENA	0	GPIO13 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP13_FN [3:0]	0000	GPIO13 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4044h GPIO13 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16453 (4045h) GPIO14 Control	15	GP14_DIR	1	GPIO14 pin direction 0 = Output 1 = Input	
	14:13	GP14_PULL [1:0]	01	GPIO14 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP14_INT_MODE	0	GPIO14 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP14_POL=1) or falling edge triggered (if GP14_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	10	GP14_POL	1	GPIO14 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP14_OD	0	GPIO14 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP14_ENA	0	GPIO14 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP14_FN [3:0]	0000	GPIO14 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4045h GPIO14 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16454 (4046h) GPIO15 Control	15	GP15_DIR	1	GPIO15 pin direction 0 = Output 1 = Input	
	14:13	GP15_PULL [1:0]	01	GPIO15 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP15_INT_MODE	0	GPIO15 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP15_POL=1) or falling edge triggered (if GP15_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	10	GP15_POL	1	GPIO15 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP15_OD	0	GPIO15 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP15_ENA	0	GPIO15 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP15_FN [3:0]	0000	GPIO15 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4046h GPIO15 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16455 (4047h) GPIO16 Control	15	GP16_DIR	1	GPIO16 pin direction 0 = Output 1 = Input	
	14:13	GP16_PULL [1:0]	01	GPIO16 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP16_INT_MODE	0	GPIO16 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP16_POL=1) or falling edge triggered (if GP16_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	10	GP16_POL	1	GPIO16 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP16_OD	0	GPIO16 Output pin configuration 0 = CMOS 1 = Open Drain	
	7	GP16_ENA	0	GPIO16 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	3:0	GP16_FN [3:0]	0000	GPIO16 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	

Register 4047h GPIO16 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16456 (4048h) Charger Control 1	15	CHG_ENA	0	Battery Charger Enable 0 = Disable 1 = Enable *Protected by security key.*	
	14	CHG_FRC	0	Force charging 0 = Normal behaviour 1 = Force charging CHG_FRC enables charging even if the battery voltage is above the restart threshold. It is not recommended to use this feature; there are safety implications in its use. This bit should be reset to 0 after charging has started. Host processor should monitor CHG_MODE_EINT to confirm that charging has started. *Protected by security key.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12:10	CHG_ITERM [2:0]	000	Battery End of Charge current threshold 000 = 20mA 001 = 30mA 010 = 40mA 011 = 50mA 100 = 60mA 101 = 70mA 110 = 80mA 111 = 90mA *Protected by security key.*	
	5	CHG_FAST	0	Battery Fast Charge Enable 0 = Disable 1 = Enable *Protected by security key.*	
	1	CHG_IMON_ENA	0	Enable battery charge current monitor at AUXADCIN1. 0 = Disabled 1 = Enabled (Note - a resistor is required between AUXADCIN1 and GND in order to measure the charge current using the AUXADC. The recommended resistor value is 10k.) *Protected by security key.*	
	0	CHG_CHIP_TEMP_MON	1	Battery Charger Thermal warning select 0 = Thermal Warning is ignored 1 = Thermal Warning pauses Battery Charger *Protected by security key.*	

Register 4048h Charger Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16457 (4049h) Charger Control 2	14	CHG_OFF_MSK	0	Battery Charger OFF mask select 0 = OFF requests not masked 1 = OFF requests masked during Charging *Protected by security key.*	
	11:8	CHG_TIME [3:0]	0110	Battery charger timeout 0000 = 60min 0001 = 90min 0010 = 120min 0011 = 150min 0100 = 180min 0101 = 210min 0110 = 240min 0111 = 270min 1000 = 300min 1001 = 330min 1010 = 360min 1011 = 390min 1100 = 420min 1101 = 450min 1110 = 480min 1111 = 510min *Protected by security key.*	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:6	CHG_TRKL_ILIM [1:0]	00	Battery Trickle Charge current limit 00 = 50mA 01 = 100mA 10 = 150mA 11 = 200mA *Protected by security key.*	
	5:4	CHG_VSEL [1:0]	00	Battery Charger target voltage 00 = 4.05V 01 = 4.10V 10 = 4.15V 11 = 4.20V Note that incorrect setting of this register may lead to a safety hazard condition. *Protected by security key.*	
	3:0	CHG_FAST_ILIM [3:0]	0010	Battery Fast Charge current limit 0000 = 0mA 0001 = 50mA 0010 = 100mA 0011 = 150mA 0100 = 200mA 0101 = 250mA 0110 = 300mA 0111 = 350mA 1000 = 400mA 1001 = 450mA 1010 = 500mA 1011 = 600mA 1100 = 700mA 1101 = 800mA 1110 = 900mA 1111 = 1000mA *Protected by security key.*	

Register 4049h Charger Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16458 (404Ah) Charger Status	15	BATT_OV_STS	0	Battery Overvoltage status 0 = Normal 1 = Battery Overvoltage	
	14:12	CHG_STATE [2:0]	000	Battery Charger state 000 = Off 001 = Trickle Charge 010 = Fast Charge 011 = Trickle Charge overtemperature 100 = Fast Charge overtemperature 101 = Defective 110 = Reserved 111 = Reserved	
	11	BATT_HOT_STS	0	Battery Hot status 0 = Normal 1 = Battery Hot	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10	BATT_COLD_ STS	0	Battery Cold status 0 = Normal 1 = Battery Cold	
	9	CHG_TOPOFF	0	Battery Charger constant-voltage charge mode status 0 = Constant-voltage mode not active 1 = Constant-voltage mode is active	
	8	CHG_ACTIVE	0	Battery Charger status 0 = Not charging 1 = Charging	
	7:0	CHG_TIME_ELAPSED [7:0]	0000_0000	Battery charger elapsed time 00h = 0min 01h = 2min 02h = 4min 03h = 6min ... FFh = 510min	

Register 404Ah Charger Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16460 (404Ch) Status LED 1	15:14	LED1_SRC [1:0]	11	LED1 Source (Selects the LED1 function.) 00 = Off 01 = Power State Status 10 = Charger Status 11 = Manual Mode Note - LED1 also indicates completion of OTP Auto Program	
	9:8	LED1_MODE [1:0]	00	LED1 Mode (Controls LED1 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence	
	5:4	LED1_SEQ_LEN [1:0]	10	LED1 Pulse Sequence Length (when LED1_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses	
	3:2	LED1_DUR [1:0]	01	LED1 On time (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	LED1_DUTY_CYC [1:0]	10	LED1 Duty Cycle (On:Off ratio) (when LED1_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2 (33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)	

Register 404Ch Status LED 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16461 (404Dh) Status LED 2	15:14	LED2_SRC [1:0]	11	LED2 Source (Selects the LED2 function.) 00 = Off 01 = Power State Status 10 = Charger Status 11 = Manual Mode Note - LED2 also indicates an OTP Auto Program Error condition	
	9:8	LED2_MODE [1:0]	00	LED2 Mode (Controls LED2 in Manual Mode only.) 00 = Off 01 = Constant 10 = Continuous Pulsed 11 = Pulsed Sequence	
	5:4	LED2_SEQ_LEN [1:0]	10	LED2 Pulse Sequence Length (when LED2_MODE = Pulsed Sequence) 00 = 1 pulse 01 = 2 pulses 10 = 4 pulses 11 = 7 pulses	
	3:2	LED2_DUR [1:0]	01	LED2 On time (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1 second 01 = 250ms 10 = 125ms 11 = 62.5ms	
	1:0	LED2_DUTY_CYC [1:0]	10	LED2 Duty Cycle (On:Off ratio) (when LED2_MODE = Continuous Pulsed or Pulsed Sequence) 00 = 1:1 (50% on) 01 = 1:2 (33.3% on) 10 = 1:3 (25% on) 11 = 1:7 (12.5% on)	

Register 404Dh Status LED 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16462 (404Eh) Current Sink 1	15	CS1_ENA	0	Current Sink 1 Enable (ISINK1 pin) 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.	
	14	CS1_DRIVE	0	Current Sink 1 output drive enable 0 = Disabled 1 = Enabled	
	13	CS1_STS	0	Current Sink 1 status 0 = Normal 1 = Sink current cannot be regulated	
	12	CS1_SLPENA	0	Current Sink 1 SLEEP Enable 0 = Disabled 1 = Controlled by CS1_ENA	
	11:10	CS1_OFF_RAMP [1:0]	01	ISINK1 Switch-Off ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.	
	9:8	CS1_ON_RAMP [1:0]	01	ISINK1 Switch-On ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.	
	5:0	CS1_ISEL [5:0]	00_0000	ISINK1 current. Current = 2.0µA × 2^(CS1_ISEL/4), where CS1_ISEL is an unsigned binary number. Alternatively, CS1_ISEL = 13.29 x LOG(current/2.0µA) 00_0000 = 2.0µA 11_0111 = 27.6mA Values greater than 11_0111 will result in the maximum current of approx 27.6mA.	

Register 404Eh Current Sink 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16463 (404Fh) Current Sink 2	15	CS2_ENA	0	Current Sink 2 Enable (ISINK2 pin) 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.	
	14	CS2_DRIVE	0	Current Sink 2 output drive enable 0 = Disabled 1 = Enabled	
	13	CS2_STS	0	Current Sink 2 status 0 = Normal 1 = Sink current cannot be regulated	
	12	CS2_SLPENA	0	Current Sink 2 SLEEP Enable 0 = Disabled 1 = Controlled by CS2_ENA	
	11:10	CS2_OFF_RAMP [1:0]	01	ISINK2 Switch-Off ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.	
	9:8	CS2_ON_RAMP [1:0]	01	ISINK2 Switch-On ramp 00 = instant (no ramp) 01 = 1 step every 4ms (220ms) 10 = 1 step every 8ms (440ms) 11 = 1 step every 16ms (880ms) The time quoted in brackets is valid for the maximum change in current drive setting. The actual time scales according to the extent of the change in current drive setting.	
	5:0	CS2_ISEL [5:0]	00_0000	ISINK2 current. Current = 2.0µA × 2^(CS2_ISEL/4), where CS2_ISEL is an unsigned binary number. Alternatively, CS2_ISEL = 13.29 x LOG(current/2.0µA) 00_0000 = 2.0µA 11_0111 = 27.6mA Values greater than 11_0111 will result in the maximum current of approx 27.6mA.	

Register 404Fh Current Sink 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16464 (4050h) DCDC Enable	7	EPE2_ENA	0	EPE2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE2_STS)	
	6	EPE1_ENA	0	EPE1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in EPE1_STS)	
	3	DC4_ENA	0	DC-DC4 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC4_STS)	
	2	DC3_ENA	0	DC-DC3 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC3_STS)	
	1	DC2_ENA	0	DC-DC2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC2_STS)	
	0	DC1_ENA	0	DC_DC1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in DC1_STS)	

Register 4050h DCDC Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16465 (4051h) LDO Enable	10	LDO11_ENA	0	LDO11 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO11_STS)	
	6	LDO7_ENA	0	LDO7 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO7_STS)	
	4	LDO5_ENA	0	LDO5 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO5_STS)	
	3	LDO4_ENA	0	LDO4 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO4_STS)	
	2	LDO3_ENA	0	LDO3 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO3_STS)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	LDO2_ENA	0	LDO2 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO2_STS)	
	0	LDO1_ENA	0	LDO1 Enable request 0 = Disabled 1 = Enabled (Note that the actual status is indicated in LDO1_STS)	

Register 4051h LDO Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16466 (4052h) DCDC Status	7	EPE2_STS	0	EPE2 Status 0 = Disabled 1 = Enabled	
	6	EPE1_STS	0	EPE1 Status 0 = Disabled 1 = Enabled	
	3	DC4_STS	0	DC-DC4 Status 0 = Disabled 1 = Enabled	
	2	DC3_STS	0	DC-DC3 Status 0 = Disabled 1 = Enabled	
	1	DC2_STS	0	DC-DC2 Status 0 = Disabled 1 = Enabled	
	0	DC1_STS	0	DC-DC1 Status 0 = Disabled 1 = Enabled	

Register 4052h DCDC Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16467 (4053h) LDO Status	10	LDO11_STS	0	LDO11 Status 0 = Disabled 1 = Enabled	
	6	LDO7_STS	0	LDO7 Status 0 = Disabled 1 = Enabled	
	4	LDO5_STS	0	LDO5 Status 0 = Disabled 1 = Enabled	
	3	LDO4_STS	0	LDO4 Status 0 = Disabled 1 = Enabled	
	2	LDO3_STS	0	LDO3 Status 0 = Disabled 1 = Enabled	
	1	LDO2_STS	0	LDO2 Status 0 = Disabled 1 = Enabled	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	LDO1_STS	0	LDO1 Status 0 = Disabled 1 = Enabled	

Register 4053h LDO Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16468 (4054h) DCDC UV Status	13	DC2_OV_STS	0	DC-DC2 Overvoltage Status 0 = Normal 1 = Overvoltage	
	12	DC1_OV_STS	0	DC-DC1 Overvoltage Status 0 = Normal 1 = Overvoltage	
	9	DC2_HC_STS	0	DC-DC2 High Current Status 0 = Normal 1 = High Current	
	8	DC1_HC_STS	0	DC-DC1 High Current Status 0 = Normal 1 = High Current	
	3	DC4_UV_STS	0	DC-DC4 Undervoltage Status 0 = Normal 1 = Undervoltage	
	2	DC3_UV_STS	0	DC-DC3 Undervoltage Status 0 = Normal 1 = Undervoltage	
	1	DC2_UV_STS	0	DC-DC2 Undervoltage Status 0 = Normal 1 = Undervoltage	
	0	DC1_UV_STS	0	DC-DC1 Undervoltage Status 0 = Normal 1 = Undervoltage	

Register 4054h DCDC UV Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16469 (4055h) LDO UV Status	15	INTLDO_UV_STS	0	LDO13 (Internal LDO) Undervoltage Status 0 = Normal 1 = Undervoltage	
	6	LDO7_UV_STS	0	LDO7 Undervoltage Status 0 = Normal 1 = Undervoltage	
	4	LDO5_UV_STS	0	LDO5 Undervoltage Status 0 = Normal 1 = Undervoltage	
	3	LDO4_UV_STS	0	LDO4 Undervoltage Status 0 = Normal 1 = Undervoltage	
	2	LDO3_UV_STS	0	LDO3 Undervoltage Status 0 = Normal 1 = Undervoltage	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1	LDO2_UV_STS	0	LDO2 Undervoltage Status 0 = Normal 1 = Undervoltage	
	0	LDO1_UV_STS	0	LDO1 Undervoltage Status 0 = Normal 1 = Undervoltage	

Register 4055h LDO UV Status

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16470 (4056h) DC1 Control 1	15:14	DC1_RATE [1:0]	10	DC-DC1 Voltage Ramp rate 00 = 1 step every 32us 01 = 1 step every 16us 10 = 1 step every 8us 11 = Immediate voltage change	
	12	DC1_PHASE	0	DC-DC1 Clock Phase Control 0 = Normal 1 = Inverted	
	9:8	DC1_FREQ [1:0]	00	DC-DC1 Switching Frequency 00 = Reserved 01 = 2.0MHz 10 = Reserved 11 = 4.0MHz	
	7	DC1_FLT	0	DC-DC1 Output float 0 = DC-DC1 output discharged when disabled 1 = DC-DC1 output floating when disabled	
	5:4	DC1_SOFT_START [1:0]	00	DC-DC1 Soft-Start Control (Duration in each of the 8 startup current limiting steps.) 00 = 32us steps 01 = 64us steps 10 = 128us steps 11 = 256us steps	
	1:0	DC1_CAP [1:0]	00	DC-DC1 Output Capacitor 00 = 4.7uF to 20uF 01 = Reserved 10 = 22uF to 47uF 11 = Reserved	

Register 4056h DC1 Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16471 (4057h) DC1 Control 2	15:14	DC1_ERR_ACT [1:0]	00	DC-DC1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12:11	DC1_HWC_SRC [1:0]	00	DC-DC1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	DC1_HWC_VSEL	0	DC-DC1 Hardware Control Voltage select 0 = Set by DC1_ON_VSEL 1 = Set by DC1_SLP_VSEL	
	9:8	DC1_HWC_MODE [1:0]	11	DC-DC1 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode	
	6:4	DC1_HC_THR [2:0]	000	DC-DC1 High Current threshold 000 = 125mA 001 = 250mA 010 = 375mA 011 = 500mA 100 = 625mA 101 = 750mA 110 = 875mA 111 = 1000mA	
	0	DC1_HC_IND_ENA	0	DC-DC1 High Current detect enable 0 = Disabled 1 = Enabled	

Register 4057h DC1 Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16472 (4058h) DC1 ON Config	15:13	DC1_ON_SLOT [2:0]	000	DC-DC1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	9:8	DC1_ON_MODE [1:0]	01	DC-DC1 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:2	DC1_ON_VSEL [6:2]	0_0000	DC-DC1 ON Voltage select DC1_ON_VSEL [6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. DC1_ON_VSEL [6:2] also exist in ICE/OTP memory, controlling the voltage in 50mV steps. DC1_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	
	1:0	DC1_ON_VSEL [1:0]	00	DC-DC1 ON Voltage select DC1_ON_VSEL [6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. See DC1_ON_VSEL [6:2] for definition.	

Register 4058h DC1 ON Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16473 (4059h) DC1 SLEEP Control	15:13	DC1_SLP_SLOT [2:0]	000	DC-DC1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.	
	9:8	DC1_SLP_MODE [1:0]	11	DC-DC1 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:0	DC1_SLP_VSEL [6:0]	000_0000	DC-DC1 SLEEP Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	

Register 4059h DC1 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16474 (405Ah) DC1 DVS Control	12:11	DC1_DVS_SRC [1:0]	00	DC-DC1 DVS Control Source 00 = Disabled 01 = Enabled 10 = Controlled by Hardware DVS1 11 = Controlled by Hardware DVS2	
	6:0	DC1_DVS_VSEL [6:0]	000_0000	DC-DC1 DVS Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	

Register 405Ah DC1 DVS Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16475 (405Bh) DC2 Control 1	15:14	DC2_RATE [1:0]	10	DC-DC2 Voltage Ramp rate 00 = 1 step every 32us 01 = 1 step every 16us 10 = 1 step every 8us 11 = Immediate voltage change	
	12	DC2_PHASE	1	DC-DC2 Clock Phase Control 0 = Normal 1 = Inverted	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	9:8	DC2_FREQ [1:0]	00	DC-DC2 Switching Frequency 00 = Reserved 01 = 2.0MHz 10 = Reserved 11 = 4.0MHz	
	7	DC2_FLT	0	DC-DC2 Output float 0 = DC-DC2 output discharged when disabled 1 = DC-DC2 output floating when disabled	
	5:4	DC2_SOFT_START [1:0]	00	DC-DC2 Soft-Start Control (Duration in each of the 8 startup current limiting steps.) 00 = 32us steps 01 = 64us steps 10 = 128us steps 11 = 256us steps	
	1:0	DC2_CAP [1:0]	00	DC-DC2 Output Capacitor 00 = 4.7uF to 20uF 01 = Reserved 10 = 22uF to 47uF 11 = Reserved	

Register 405Bh DC2 Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16476 (405Ch) DC2 Control 2	15:14	DC2_ERR_ACT [1:0]	00	DC-DC2 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	DC2_HWC_SRC [1:0]	00	DC-DC2 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	DC2_HWC_VSEL	0	DC-DC2 Hardware Control Voltage select 0 = Set by DC2_ON_VSEL 1 = Set by DC2_SLP_VSEL	
	9:8	DC2_HWC_MODE [1:0]	11	DC-DC2 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode	
	6:4	DC2_HC_THR [2:0]	000	DC-DC2 High Current threshold 000 = 125mA 001 = 250mA 010 = 375mA 011 = 500mA 100 = 625mA 101 = 750mA 110 = 875mA 111 = 1000mA	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	DC2_HC_IND_ENA	0	DC-DC2 High Current detect enable 0 = Disabled 1 = Enabled	

Register 405Ch DC2 Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16477 (405Dh) DC2 ON Config	15:13	DC2_ON_SLOT [2:0]	000	DC-DC2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	9:8	DC2_ON_MODE [1:0]	01	DC-DC2 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:2	DC2_ON_VSEL [6:2]	0_0000	DC-DC2 ON Voltage select DC2_ON_VSEL [6:0] selects the DC-DC2 output voltage from 0.6V to 1.8V in 12.5mV steps. DC2_ON_VSEL [6:2] also exist in ICE/OTP memory, controlling the voltage in 50mV steps. DC2_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	
	1:0	DC2_ON_VSEL [1:0]	00	DC-DC2 ON Voltage select DC2_ON_VSEL [6:0] selects the DC-DC2 output voltage from 0.6V to 1.8V in 12.5mV steps. See DC2_ON_VSEL [6:2] for definition.	

Register 405Dh DC2 ON Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16478 (405Eh) DC2 SLEEP Control	15:13	DC2_SLP_SLOT [2:0]	000	DC-DC2 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC2 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.	
	9:8	DC2_SLP_MODE [1:0]	11	DC-DC2 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:0	DC2_SLP_VSEL [6:0]	000_0000	DC-DC2 SLEEP Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	

Register 405Eh DC2 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16479 (405Fh) DC2 DVS Control	12:11	DC2_DVS_SRC [1:0]	00	DC-DC2 DVS Control Source 00 = Disabled 01 = Enabled 10 = Controlled by Hardware DVS1 11 = Controlled by Hardware DVS2	
	6:0	DC2_DVS_VSEL [6:0]	000_0000	DC-DC2 DVS Voltage select 0.6V to 1.8V in 12.5mV steps 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	

Register 405Fh DC2 DVS Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16480 (4060h) DC3 Control 1	12	DC3_PHASE	0	DC-DC3 Clock Phase Control 0 = Normal 1 = Inverted	
	7	DC3_FLT	0	DC-DC3 Output float 0 = DC-DC3 output discharged when disabled 1 = DC-DC3 output floating when disabled	
	5:4	DC3_SOFT_START [1:0]	01	DC-DC3 Soft-Start Control (Duration in each of the 3 intermediate startup current limiting steps.) 00 = Immediate start-up 01 = 512us steps 10 = 4.096ms steps 11 = 32.768ms steps	
	3:2	DC3_STNBY_LIM [1:0]	01	DC-DC3 Current Limit Sets the maximum DC output current in Hysteretic Mode. Typical values shown below. 00 = 100mA 01 = 200mA 10 = 400mA 11 = 800mA *Protected by security key.*	
	1:0	DC3_CAP [1:0]	00	DC-DC3 Output Capacitor 00 = 10uF to 20uF 01 = 10uF to 20uF 10 = 22uF to 45uF 11 = 47uF to 100uF	

Register 4060h DC3 Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16481 (4061h) DC3 Control 2	15:14	DC3_ERR_ACT [1:0]	00	DC-DC3 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	DC3_HWC_SRC [1:0]	00	DC-DC3 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	DC3_HWC_VSEL	0	DC-DC3 Hardware Control Voltage select 0 = Set by DC3_ON_VSEL 1 = Set by DC3_SLP_VSEL	
	9:8	DC3_HWC_MODE [1:0]	11	DC-DC3 Hardware Control Operating Mode 00 = Forced Continuous Conduction Mode 01 = Disabled 10 = LDO Mode 11 = Hysteretic Mode	
	7	DC3_OVP	0	DC-DC3 Overvoltage Protection 0 = Disabled 1 = Enabled	

Register 4061h DC3 Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16482 (4062h) DC3 ON Config	15:13	DC3_ON_SLOT [2:0]	000	DC-DC3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	9:8	DC3_ON_MODE [1:0]	01	DC-DC3 ON Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:2	DC3_ON_VSEL [6:2]	0_0000	DC-DC3 ON Voltage select DC3_ON_VSEL [6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. DC3_ON_VSEL [6:2] also exist in ICE/OTP memory, controlling the voltage in 100mV steps. DC3_ON_VSEL [6:0] is coded as follows: 00h = 0.85V 01h = 0.875V … 65h = 3.375V	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				66h to 7Fh = 3.4V	
	1:0	DC3_ON_VSEL [1:0]	00	DC3 ON Voltage select DC3_ON_VSEL [6:0] selects the DC3 output voltage from 0.85V to 3.4V in 25mV steps. See DC3_ON_VSEL [6:2] for definition.	

Register 4062h DC3 ON Config

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16483 (4063h) DC3 SLEEP Control	15:13	DC3_SLP_SLOT [2:0]	000	DC-DC3 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If DC-DC3 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the converter enters its SLEEP condition.	
	9:8	DC3_SLP_MODE [1:0]	11	DC-DC3 SLEEP Operating Mode 00 = Forced Continuous Conduction Mode 01 = Auto Mode (Continuous / Discontinuous Conduction with Pulse-Skipping) 10 = LDO Mode 11 = Hysteretic Mode	
	6:0	DC3_SLP_VSEL [6:0]	000_0000	DC-DC3 SLEEP Voltage select 0.85V to 3.4V in 25mV steps 00h = 0.85V 01h = 0.875V … 65h = 3.375V 66h to 7Fh = 3.4V	

Register 4063h DC3 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16484 (4064h) DC4 Control	15:14	DC4_ERR_ACT [1:0]	00	DC-DC4 Error Action (Undervoltage) 00 = Ignore 01 = Shut down converter 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	12:11	DC4_HWC_SRC [1:0]	00	DC-DC4 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	8	DC4_HWC_MODE	1	DC-DC4 Hardware Control Operating Mode 0 = DC-DC4 is controlled by DC4_ENA 1 = DC-DC4 is disabled when Hardware Control Source is asserted	
	3:2	DC4_RANGE [1:0]	01	Selects the voltage range for DC-DC4 00 = 20V < VOUT <= 30V 01 = 10V < VOUT <= 20V 10 = 6.5V < VOUT <= 10V 11 = Reserved *Protected by security key.*	
	0	DC4_FBSRC	0	DC-DC4 Voltage Feedback source 0 = ISINK1 1 = ISINK2	

Register 4064h DC4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16485 (4065h) DC4 SLEEP Control	8	DC4_SLPENA	0	DC-DC4 SLEEP Enable 0 = Disabled 1 = Controlled by DC4_ENA	

Register 4065h DC4 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16486 (4066h) EPE1 Control	15:13	EPE1_ON_SLOT [2:0]	000	EPE1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:11	EPE1_HWC_SRC [1:0]	00	EPE1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	8	EPE1_HWCENA	0	EPE1 Hardware Control Enable 0 = EPE1 is controlled by EPE1_ENA (Hardware Control input(s) are ignored) 1 = EPE1 is controlled by HWC inputs (Hardware Control input(s) force EPE1 to be de-asserted)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:5	EPE1_SLP_SLOT [2:0]	000	EPE1 SLEEP Slot select 000 = No action 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = No action 111 = No action	

Register 4066h EPE1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16487 (4067h) EPE2 Control	15:13	EPE2_ON_SLOT [2:0]	000	EPE2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:11	EPE2_HWC_SRC [1:0]	00	EPE2 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	8	EPE2_HWCENA	0	EPE2 Hardware Control Enable 0 = EPE2 is controlled by EPE2_ENA (Hardware Control input(s) are ignored) 1 = EPE2 is controlled by HWC inputs (Hardware Control input(s) force EPE2 to be de-asserted)	
	7:5	EPE2_SLP_SLOT [2:0]	000	EPE2 SLEEP Slot select 000 = No action 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = No action 111 = No action	

Register 4067h EPE2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16488 (4068h) LDO1 Control	15:14	LDO1_ERR_ACT [1:0]	00	LDO1 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO1_HWC_SRC [1:0]	00	LDO1 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO1_HWC_VSEL	0	LDO1 Hardware Control Voltage select 0 = Set by LDO1_ON_VSEL 1 = Set by LDO1_SLP_VSEL	
	9:8	LDO1_HWC_MODE [1:0]	10	LDO1 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO1_ON_MODE	
	7	LDO1_FLT	0	LDO1 Output float 0 = LDO1 output discharged when disabled 1 = LDO1 output floating when disabled	
	6	LDO1_SWI	0	LDO1 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO1_LP_MODE	0	LDO1 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 4068h LDO1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16489 (4069h) LDO1 ON Control	15:13	LDO1_ON_SLOT [2:0]	000	LDO1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO1_ON_MODE	0	LDO1 ON Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO1_ON_VSEL [4:0]	0_0000	LDO1 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 4069h LDO1 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16490 (406Ah) LDO1 SLEEP Control	15:13	LDO1_SLP_SLOT [2:0]	000	LDO1 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO1 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO1_SLP_MODE	1	LDO1 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO1_SLP_VSEL [4:0]	0_0000	LDO1 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 406Ah LDO1 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16491 (406Bh) LDO2 Control	15:14	LDO2_ERR_ACT [1:0]	00	LDO2 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO2_HWC_SRC [1:0]	00	LDO2 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO2_HWC_VSEL	0	LDO2 Hardware Control Voltage select 0 = Set by LDO2_ON_VSEL 1 = Set by LDO2_SLP_VSEL	
	9:8	LDO2_HWC_MODE [1:0]	10	LDO2 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO2_ON_MODE	
	7	LDO2_FLT	0	LDO2 Output float 0 = LDO2 output discharged when disabled 1 = LDO2 output floating when disabled	
	6	LDO2_SWI	0	LDO2 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO2_LP_MODE	0	LDO2 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 406Bh LDO2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16492 (406Ch) LDO2 ON Control	15:13	LDO2_ON_SLOT [2:0]	000	LDO2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO2_ON_MODE	0	LDO2 ON Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO2_ON_VSEL [4:0]	0_0000	LDO2 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 406Ch LDO2 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16493 (406Dh) LDO2 SLEEP Control	15:13	LDO2_SLP_SLOT [2:0]	000	LDO2 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO2 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO2_SLP_MODE	1	LDO2 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO2_SLP_VSEL [4:0]	0_0000	LDO2 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 406Dh LDO2 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16494 (406Eh) LDO3 Control	15:14	LDO3_ERR_ACT [1:0]	00	LDO3 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO3_HWC_SRC [1:0]	00	LDO3 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO3_HWC_VSEL	0	LDO3 Hardware Control Voltage select 0 = Set by LDO3_ON_VSEL 1 = Set by LDO3_SLP_VSEL	
	9:8	LDO3_HWC_MODE [1:0]	10	LDO3 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO3_ON_MODE	
	7	LDO3_FLT	0	LDO3 Output float 0 = LDO3 output discharged when disabled 1 = LDO3 output floating when disabled	
	6	LDO3_SWI	0	LDO3 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO3_LP_MODE	0	LDO3 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 406Eh LDO3 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16495 (406Fh) LDO3 ON Control	15:13	LDO3_ON_SLOT [2:0]	000	LDO3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO3_ON_MODE	0	LDO3 ON Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO3_ON_VSEL [4:0]	0_0000	LDO3 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 406Fh LDO3 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16496 (4070h) LDO3 SLEEP Control	15:13	LDO3_SLP_SLOT [2:0]	000	LDO3 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO3 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO3_SLP_MODE	1	LDO3 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO3_SLP_VSEL [4:0]	0_0000	LDO3 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 4070h LDO3 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16497 (4071h) LDO4 Control	15:14	LDO4_ERR_ACT [1:0]	00	LDO4 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO4_HWC_SRC [1:0]	00	LDO4 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO4_HWC_VSEL	0	LDO4 Hardware Control Voltage select 0 = Set by LDO4_ON_VSEL 1 = Set by LDO4_SLP_VSEL	
	9:8	LDO4_HWC_MODE [1:0]	10	LDO4 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO4_ON_MODE	
	7	LDO4_FLT	0	LDO4 Output float 0 = LDO4 output discharged when disabled 1 = LDO4 output floating when disabled	
	6	LDO4_SWI	0	LDO4 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO4_LP_MODE	0	LDO4 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 4071h LDO4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16498 (4072h) LDO4 ON Control	15:13	LDO4_ON_SLOT [2:0]	000	LDO4 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO4_ON_MODE	0	LDO4 ON Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO4_ON_VSEL [4:0]	0_0000	LDO4 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 4072h LDO4 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16499 (4073h) LDO4 SLEEP Control	15:13	LDO4_SLP_SLOT [2:0]	000	LDO4 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO4 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO4_SLP_MODE	1	LDO4 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO4_SLP_VSEL [4:0]	0_0000	LDO4 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 4073h LDO4 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16500 (4074h) LDO5 Control	15:14	LDO5_ERR_ACT [1:0]	00	LDO5 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO5_HWC_SRC [1:0]	00	LDO5 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO5_HWC_VSEL	0	LDO5 Hardware Control Voltage select 0 = Set by LDO5_ON_VSEL 1 = Set by LDO5_SLP_VSEL	
	9:8	LDO5_HWC_MODE [1:0]	10	LDO5 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO5_ON_MODE	
	7	LDO5_FLT	0	LDO5 Output float 0 = LDO5 output discharged when disabled 1 = LDO5 output floating when disabled	
	6	LDO5_SWI	0	LDO5 Switch Mode 0 = LDO mode 1 = Switch mode	
	0	LDO5_LP_MODE	0	LDO5 Low Power Mode Select 0 = 50mA (reduced quiescent current) 1 = 20mA (minimum quiescent current) Selects which Low Power mode is used in ON, SLEEP, or under HWC modes.	

Register 4074h LDO5 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16501 (4075h) LDO5 ON Control	15:13	LDO5_ON_SLOT [2:0]	000	LDO5 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO5_ON_MODE	0	LDO5 ON Operating Mode 0 = Normal mode 1 = Low Power mode	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:0	LDO5_ON_VSEL [4:0]	0_0000	LDO5 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 4075h LDO5 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16502 (4076h) LDO5 SLEEP Control	15:13	LDO5_SLP_SLOT [2:0]	000	LDO5 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO5 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO5_SLP_MODE	1	LDO5 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO5_SLP_VSEL [4:0]	0_0000	LDO5 SLEEP Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 4076h LDO5 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16506 (407Ah) LDO7 Control	15:14	LDO7_ERR_ACT [1:0]	00	LDO7 Error Action (Undervoltage) 00 = Ignore 01 = Shut down regulator 10 = Shut down system (Device Reset) 11 = Reserved Note that an Interrupt is always raised.	
	12:11	LDO7_HWC_SRC [1:0]	00	LDO7 Hardware Control Source 00 = Disabled 01 = Hardware Control 1 10 = Hardware Control 2 11 = Hardware Control 1 or 2	
	10	LDO7_HWC_VSEL	0	LDO7 Hardware Control Voltage select 0 = Set by LDO7_ON_VSEL 1 = Set by LDO7_SLP_VSEL	
	9:8	LDO7_HWC_MODE [1:0]	10	LDO7 Hardware Control Operating Mode 00 = Low Power mode 01 = Turn converter off 10 = Low Power mode 11 = Set by LDO7_ON_MODE	
	7	LDO7_FLT	0	LDO7 Output float 0 = LDO7 output discharged when disabled 1 = LDO7 output floating when disabled	
	6	LDO7_SWI	0	LDO7 Switch Mode 0 = LDO mode 1 = Switch mode	

Register 407Ah LDO7 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16507 (407Bh) LDO7 ON Control	15:13	LDO7_ON_SLOT [2:0]	000	LDO7 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	8	LDO7_ON_MODE	0	LDO7 ON Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO7_ON_VSEL [4:0]	0_0000	LDO7 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V … 0Ch = 1.60V 0Dh = 1.70V … 1Eh = 3.40V	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				1Fh = 3.50V	

Register 407Bh LDO7 ON Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16508 (407Ch) LDO7 SLEEP Control	15:13	LDO7_SLP_SLOT [2:0]	000	LDO7 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO7 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	8	LDO7_SLP_MODE	1	LDO7 SLEEP Operating Mode 0 = Normal mode 1 = Low Power mode	
	4:0	LDO7_SLP_VSEL [4:0]	0_0000	LDO7 SLEEP Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V … 0Ch = 1.60V 0Dh = 1.70V … 1Eh = 3.40V 1Fh = 3.50V	

Register 407Ch LDO7 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16519 (4087h) LDO11 ON Control	15:13	LDO11_ON_SLOT [2:0]	000	LDO11 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
	12	LDO11_FRCENA	0	LDO11 Force Enable (forces LDO11 to be enabled at all times in the OFF, ON and SLEEP states) 0 = Disabled 1 = Enabled	
	7	LDO11_VSEL_SRC	0	LDO11 Voltage Select source 0 = Normal (LDO11 settings) 1 = Same as DC-DC Converter 1	
	3:0	LDO11_ON_VSEL [3:0]	0000	LDO11 ON Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V … Eh = 1.50V Fh = 1.55V	

Register 4087h LDO11 ON Control

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
R16520 (4088h) LDO11 SLEEP Control	15:13	LDO11_SLP_SLOT [2:0]	000	LDO11 SLEEP Slot select 000 = SLEEP voltage / operating mode transition in Timeslot 5 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = SLEEP voltage / operating mode transition in Timeslot 3 111 = SLEEP voltage / operating mode transition in Timeslot 1 If LDO11 is assigned to a Hardware Enable Input, then codes 001-101 select in which timeslot the regulator enters its SLEEP condition.	
	3:0	LDO11_SLP_VSEL [3:0]	0000	LDO11 SLEEP Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V … Eh = 1.50V Fh = 1.55V	

Register 4088h LDO11 SLEEP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16526 (408Eh) Power Good Source 1	3	DC4_OK	0	DC-DC4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	2	DC3_OK	1	DC-DC3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	1	DC2_OK	1	DC-DC2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	0	DC1_OK	1	DC-DC1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	

Register 408Eh Power Good Source 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16527 (408Fh) Power Good Source 2	6	LDO7_OK	1	LDO7 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	4	LDO5_OK	1	LDO5 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	3	LDO4_OK	1	LDO4 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	2	LDO3_OK	1	LDO3 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	1	LDO2_OK	1	LDO2 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	
	0	LDO1_OK	1	LDO1 status selected as an input to PWR_GOOD 0 = Disabled 1 = Enabled	

Register 408Fh Power Good Source 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16528 (4090h) Clock Control 1	15	CLKOUT_ENA	0	CLKOUT output enable 0 = Disabled 1 = Enabled *Protected by security key*	
	13	CLKOUT_OD	0	CLKOUT pin configuration 0 = CMOS 1 = Open Drain	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	10:8	CLKOUT_SLOT [2:0]	000	CLKOUT output enable ON slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Do not enable 111 = Do not enable	
	6:4	CLKOUT_SLPSLOT [2:0]	000	CLKOUT output SLEEP slot select 000 = Controlled by CLKOUT_ENA 001 = Disable in Timeslot 5 010 = Disable in Timeslot 4 011 = Disable in Timeslot 3 100 = Disable in Timeslot 2 101 = Disable in Timeslot 1 110 = Controlled by CLKOUT_ENA 111 = Controlled by CLKOUT_ENA	
	0	CLKOUT_SRC	0	CLKOUT output source select 0 = FLL output 1 = 32.768kHz oscillator	

Register 4090h Clock Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16529 (4091h) Clock Control 2	15	XTAL_INH	0	Crystal Start-Up Inhibit 0 = Disabled 1 = Enabled When XTAL_INH=1, the ‘ON’ transition is inhibited until the crystal oscillator is valid	
	13	XTAL_ENA	0	Crystal Oscillator Enable 0 = Disabled at all times 1 = Enabled in OFF, ON and SLEEP states (Note that the BACKUP behaviour is determined by XTAL_BKUPENA.)	
	12	XTAL_BKUPENA	1	Selects the RTC and 32.768kHz oscillator in BACKUP state 0 = RTC unclocked in BACKUP 1 = RTC maintained in BACKUP (Note that XTAL_ENA must also be set if the RTC is to be maintained in BACKUP.)	
	7	FLL_AUTO	1	FLL Automatic Mode Enable 0 = Manual configuration mode 1 = Automatic configuration mode (To enable the FLL output, FLL_ENA must also be set in Automatic mode)	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	FLL_AUTO_FREQ [2:0]	000	FLL Automatic Mode Frequency select 000 = 2.048MHz 001 = 11.2896MHz 010 = 12MHz 011 = 12.288MHz 100 = 19.2MHz 101 = 22.5792MHz 110 = 24MHz 111 = 24.576MHz	

Register 4091h Clock Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16530 (4092h) FLL Control 1	2	FLL_FRAC	0	Fractional enable 0 = Integer Mode 1 = Fractional Mode Integer mode offers reduced power consumption. Fractional mode offers best FLL performance, provided also that N.K is a non-integer value.	
	0	FLL_ENA	0	FLL Enable 0 = Disabled 1 = Enabled Note - this bit is reset to 0 when the OFF power state is entered.	

Register 4092h FLL Control 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16531 (4093h) FLL Control 2	13:8	FLL_OUTDIV [5:0]	00_0000	FOUT clock divider 000000 = Reserved 000001 = Reserved 000010 = Reserved 000011 = 4 000100 = 5 000101 = 6 … 111110 = 63 111111 = 64 (FOUT = FVCO / FLL_OUTDIV)	
	6:4	FLL_CTRL_RATE [2:0]	000	Frequency of the FLL control block 000 = FVCO / 1 (Recommended value) 001 = FVCO / 2 010 = FVCO / 3 011 = FVCO / 4 100 = FVCO / 5 101 = FVCO / 6 110 = FVCO / 7 111 = FVCO / 8 Recommended that this register is not changed from default.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	FLL_FRATIO [2:0]	000	FVCO clock divider 000 = 1 001 = 2 010 = 4 011 = 8 1XX = 16 000 recommended for high FREF 011 recommended for low FREF	

Register 4093h FLL Control 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16532 (4094h) FLL Control 3	15:0	FLL_K [15:0]	0000_0000_0000_0000	Fractional multiply for FREF (MSB = 0.5)	

Register 4094h FLL Control 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16533 (4095h) FLL Control 4	14:5	FLL_N [9:0]	01_0111_0111	Integer multiply for FREF (LSB = 1)	
	3:0	FLL_GAIN [3:0]	0000	Gain applied to error 0000 = x 1 (Recommended value) 0001 = x 2 0010 = x 4 0011 = x 8 0100 = x 16 0101 = x 32 0110 = x 64 0111 = x 128 1XXX = x 256 Recommended that this register is not changed from default.	

Register 4095h FLL Control 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R16534 (4096h) FLL Control 5	4:3	FLL_CLK_REF_DIV [1:0]	00	FLL Clock Reference Divider 00 = 1 01 = 2 10 = 4 11 = 8 CLKIN must be divided down to <=13.5MHz. For lower power operation, the reference clock can be divided down further if desired.	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	FLL_CLK_SRC [1:0]	00	FLL Clock source 00 = 32.768kHz xtal oscillator 01 = CLKIN 10 = Reserved 11 = Reserved	

Register 4096h FLL Control 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30720 (7800h) Unique ID 1	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 7	

Register 7800h Unique ID 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30721 (7801h) Unique ID 2	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 6	

Register 7801h Unique ID 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30722 (7802h) Unique ID 3	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 5	

Register 7802h Unique ID 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30723 (7803h) Unique ID 4	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 4	

Register 7803h Unique ID 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30724 (7804h) Unique ID 5	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 3	

Register 7804h Unique ID 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30725 (7805h) Unique ID 6	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 2	

Register 7805h Unique ID 6

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30726 (7806h) Unique ID 7	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 1	

Register 7806h Unique ID 7

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30727 (7807h) Unique ID 8	15:0	UNIQUE_ID [15:0]	0000_0000_0000_0000	Unique ID, Word 0	

Register 7807h Unique ID 8

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30728 (7808h) Factory OTP ID	15:1	OTP_FACT_ID [14:0]	000_0000_0000_0000	[No description available]	
	0	OTP_FACT_FINAL	0	[No description available]	

Register 7808h Factory OTP ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30729 (7809h) Factory OTP 1	15:12	DC3_TRIM [3:0]	0000	[No description available]	
	11:6	DC2_TRIM [5:0]	00_0000	[No description available]	
	5:0	DC1_TRIM [5:0]	00_0000	[No description available]	

Register 7809h Factory OTP 1

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30730 (780Ah) Factory OTP 2	15:0	CHIP_ID [15:0]	0000_0000_0000_0000	[No description available]	

Register 780Ah Factory OTP 2

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30731 (780Bh) Factory OTP 3	10:7	OSC_TRIM [3:0]	0000	[No description available]	
	6:3	BG_TRIM [3:0]	0000	[No description available]	
	2:0	LPBG_TRIM [2:0]	000	[No description available]	

Register 780Bh Factory OTP 3

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30732 (780Ch) Factory OTP 4	7:1	CHILD_I2C_ADDR [6:0]	000_0000	[No description available]	
	0	CH_AW	0	[No description available]	

Register 780Ch Factory OTP 4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30733 (780Dh) Factory OTP 5	5:0	CHARGE_TRIM [5:0]	00_0000	[No description available]	

Register 780Dh Factory OTP 5

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30736 (7810h) Customer OTP ID	15	OTP_AUTO_PROG	0	If this bit is set when bootstrap data is loaded from ICE (in development mode), then the ICE contents will be programmed in the OTP.	
	14:1	OTP_CUST_ID [13:0]	00_0000_0000_0000	This field is checked when an ‘ON’ transition is requested. A non-zero value is used to confirm valid data.	
	0	OTP_CUST_FINAL	0	If OTP_CUST_FINAL is set in the OTP and also set in the DCRW, then no further Writes are possible to the OTP.	

Register 7810h Customer OTP ID

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30737 (7811h) DC1 OTP Control	15:13	DC1_ON_SLOT [2:0]	000	DC-DC1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	9:8	DC1_FREQ [1:0]	00	DC-DC1 Switching Frequency 00 = Reserved 01 = 2.0MHz 10 = Reserved 11 = 4.0MHz	
	7	DC1_PHASE	0	DC-DC1 Clock Phase Control 0 = Normal 1 = Inverted	
	6:2	DC1_ON_VSEL [6:2]	0_0000	DC-DC1 ON Voltage select DC1_ON_VSEL [6:0] selects the DC-DC1 output voltage from 0.6V to 1.8V in 12.5mV steps. DC1_ON_VSEL [6:2] controls the voltage in 50mV steps. DC1_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	
	1:0	DC1_CAP [1:0]	00	DC-DC1 Output Capacitor 00 = 4.7uF to 20uF 01 = Reserved 10 = 22uF to 47uF 11 = Reserved	

Register 7811h DC1 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30738 (7812h) DC2 OTP Control	15:13	DC2_ON_SLOT [2:0]	000	DC-DC2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	9:8	DC2_FREQ [1:0]	00	DC-DC2 Switching Frequency 00 = Reserved 01 = 2.0MHz 10 = Reserved 11 = 4.0MHz	
	7	DC2_PHASE	1	DC-DC2 Clock Phase Control 0 = Normal 1 = Inverted	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:2	DC2_ON_VSEL [6:2]	0_0000	DC-DC2 ON Voltage select DC2_ON_VSEL [6:0] selects the DC-DC2 output voltage from 0.6V to 1.8V in 12.5mV steps. DC2_ON_VSEL [6:2] controls the voltage in 50mV steps. DC2_ON_VSEL [6:0] is coded as follows: 00h to 08h = 0.6V 09h = 0.6125V … 48h = 1.4V (see note) … 67h = 1.7875V 68h to 7Fh = 1.8V Note - Maximum output voltage selection in 4MHz switching mode is 48h (1.4V).	
	1:0	DC2_CAP [1:0]	00	DC-DC2 Output Capacitor 00 = 4.7uF to 20uF 01 = Reserved 10 = 22uF to 47uF 11 = Reserved	

Register 7812h DC2 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30739 (7813h) DC3 OTP Control	15:13	DC3_ON_SLOT [2:0]	000	DC-DC3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	7	DC3_PHASE	0	DC-DC3 Clock Phase Control 0 = Normal 1 = Inverted	
	6:2	DC3_ON_VSEL [6:2]	0_0000	DC-DC3 ON Voltage select DC3_ON_VSEL [6:0] selects the DC-DC3 output voltage from 0.85V to 3.4V in 25mV steps. DC3_ON_VSEL [6:2] controls the voltage in 100mV steps. DC3_ON_VSEL [6:0] is coded as follows: 00h = 0.85V 01h = 0.875V … 65h = 3.375V 66h to 7Fh = 3.4V	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	1:0	DC3_CAP [1:0]	00	DC-DC3 Output Capacitor 00 = 10uF to 20uF 01 = 10uF to 20uF 10 = 22uF to 45uF 11 = 47uF to 100uF	

Register 7813h DC3 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30740 (7814h) LDO1/2 OTP Control	15:13	LDO2_ON_SLOT [2:0]	000	LDO2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	LDO2_ON_VSEL [4:0]	0_0000	LDO2 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	
	7:5	LDO1_ON_SLOT [2:0]	000	LDO1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:0	LDO1_ON_VSEL [4:0]	0_0000	LDO1 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 7814h LDO1/2 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30741 (7815h) LDO3/4 OTP Control	15:13	LDO4_ON_SLOT [2:0]	000	LDO4 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	12:8	LDO4_ON_VSEL [4:0]	0_0000	LDO4 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	
	7:5	LDO3_ON_SLOT [2:0]	000	LDO3 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:0	LDO3_ON_VSEL [4:0]	0_0000	LDO3 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 7815h LDO3/4 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30742 (7816h) LDO5/6 OTP Control	7:5	LDO5_ON_SLOT [2:0]	000	LDO5 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:0	LDO5_ON_VSEL [4:0]	0_0000	LDO5 ON Voltage select 0.9V to 1.6V in 50mV steps 1.7V to 3.3V in 100mV steps 00h = 0.90V 01h = 0.95V … 0Eh = 1.60V 0Fh = 1.70V … 1Eh = 3.20V 1Fh = 3.30V	

Register 7816h LDO5/6 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30743 (7817h) LDO7/8 OTP Control	7:5	LDO7_ON_SLOT [2:0]	000	LDO7 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:0	LDO7_ON_VSEL [4:0]	0_0000	LDO7 ON Voltage select 1.0V to 1.6V in 50mV steps 1.7V to 3.5V in 100mV steps 00h = 1.00V 01h = 1.05V 02h = 1.10V … 0Ch = 1.60V 0Dh = 1.70V … 1Eh = 3.40V 1Fh = 3.50V	

Register 7817h LDO7/8 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30745 (7819h) LDO11/EPE Control	15:13	LDO11_ON_SLOT [2:0]	000	LDO11 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	11:8	LDO11_ON_VSEL [3:0]	0000	LDO11 ON Voltage select 0.80V to 1.55V in 50mV steps 0h = 0.80V 1h = 0.85V 2h = 0.90V … Eh = 1.50V Fh = 1.55V	
	7:5	EPE2_ON_SLOT [2:0]	000	EPE2 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	4:2	EPE1_ON_SLOT [2:0]	000	EPE1 ON Slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	1:0	USB100MA_STARTUP [1:0]	00	Sets the device behaviour when starting up under USB power, when USB_ILIM = 010b (100mA) 00 = Normal 01 = Soft-Start 10 = Only start if BATTVDD > 3.1V 11 = Only start if BATTVDD > 3.4V In the 1X modes, if the battery voltage is less than the selected threshold, then the device will enable trickle charge mode instead of executing the start-up request. The start-up request is delayed until the battery voltage threshold has been met.	

Register 7819h LDO11/EPE Control

REGISTER ADDRESS	**BIT**	**LABEL**	**DEFAULT**	**DESCRIPTION**	**REFER TO**
R30746 (781Ah) GPIO1 OTP Control	15	GP1_DIR	1	GPIO1 pin direction 0 = Output 1 = Input	
	14:13	GP1_PULL [1:0]	01	GPIO1 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP1_INT_MODE	0	GPIO1 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP1_POL=1) or falling edge triggered (if GP1_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP1_PWR_DOM	0	GPIO1 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP1_POL	1	GPIO1 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP1_OD	0	GPIO1 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP1_ENA	0	GPIO1 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP1_FN [3:0]	0000	GPIO1 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3	CLKOUT_SRC	0	CLKOUT output source select 0 = FLL output 1 = 32.768kHz oscillator	
	1	XTAL_INH	0	Crystal Start-Up Inhibit 0 = Disabled 1 = Enabled When XTAL_INH=1, the 'ON' transition is inhibited until the crystal oscillator is valid	
	0	CHG_ENA	0	Battery Charger Enable 0 = Disable 1 = Enable *Protected by security key.*	

Register 781Ah GPIO1 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30747 (781Bh) GPIO2 OTP Control	15	GP2_DIR	1	GPIO2 pin direction 0 = Output 1 = Input	
	14:13	GP2_PULL [1:0]	01	GPIO2 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP2_INT_MODE	0	GPIO2 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP2_POL=1) or falling edge triggered (if GP2_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP2_PWR_DOM	0	GPIO2 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP2_POL	1	GPIO2 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP2_OD	0	GPIO2 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP2_ENA	0	GPIO2 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	7:4	GP2_FN [3:0]	0000	GPIO2 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3:1	CLKOUT_SLOT [2:0]	000	CLKOUT output enable slot select 000 = Do not enable 001 = Enable in Timeslot 1 010 = Enable in Timeslot 2 011 = Enable in Timeslot 3 100 = Enable in Timeslot 4 101 = Enable in Timeslot 5 110 = Controlled by Hardware Enable 1 111 = Controlled by Hardware Enable 2	
	0	WDOG_ENA	1	Watchdog Timer Enable 0 = Disabled 1 = Enabled (enables the watchdog; does not reset it) *Protected by security key.*	

Register 781Bh GPIO2 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30748 (781Ch) GPIO3 OTP Control	15	GP3_DIR	1	GPIO3 pin direction 0 = Output 1 = Input	
	14:13	GP3_PULL [1:0]	01	GPIO3 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP3_INT_MODE	0	GPIO3 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP3_POL=1) or falling edge triggered (if GP3_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP3_PWR_DOM	0	GPIO3 Power Domain select 0 = DBVDD 1 = PMICVDD (LDO12)	
	10	GP3_POL	1	GPIO3 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP3_OD	0	GPIO3 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP3_ENA	0	GPIO3 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP3_FN [3:0]	0000	GPIO3 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3:1	FLL_AUTO_FREQ [2:0]	000	FLL Automatic Mode Frequency select 000 = 2.048MHz 001 = 11.2896MHz 010 = 12MHz 011 = 12.288MHz 100 = 19.2MHz 101 = 22.5792MHz 110 = 24MHz 111 = 24.576MHz	

Register 781Ch GPIO3 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30749 (781Dh) GPIO4 OTP Control	15	GP4_DIR	1	GPIO4 pin direction 0 = Output 1 = Input	
	14:13	GP4_PULL [1:0]	01	GPIO4 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP4_INT_MODE	0	GPIO4 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP4_POL=1) or falling edge triggered (if GP4_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP4_PWR_DOM	0	GPIO4 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP4_POL	1	GPIO4 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP4_OD	0	GPIO4 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP4_ENA	0	Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP4_FN [3:0]	0000	GPIO4 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3:2	LED1_SRC [1:0]	11	LED1 Source Selects the LED1 function.) 00 = Off 01 = Power State Status 10 = Charger Status 11 = Manual Mode Note - LED1 also indicates completion of OTP Auto Program	
	1:0	LED2_SRC [1:0]	11	LED2 Source Selects the LED2 function.) 00 = Off 01 = Power State Status 10 = Charger Status 11 = Manual Mode Note - LED2 also indicates an OTP Auto Program Error condition	

Register 781Dh GPIO4 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30750 (781Eh) GPIO5 OTP Control	15	GP5_DIR	1	GPIO5 pin direction 0 = Output 1 = Input	
	14:13	GP5_PULL [1:0]	01	GPIO5 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP5_INT_MODE	0	GPIO5 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP5_POL=1) or falling edge triggered (if GP5_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP5_PWR_DOM	0	GPIO5 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP5_POL	1	GPIO5 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP5_OD	0	GPIO5 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP5_ENA	0	GPIO5 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP5_FN [3:0]	0000	GPIO5 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request 4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3:1	USB_ILIM [2:0]	010	Sets the USB current limit 000 = 0mA (USB switch is open) 001 = 2.5mA 010 = 100mA 011 = 500mA 100 = 900mA 101 = 1500mA 110 = 1800mA 111 = 550mA	

Register 781Eh GPIO5 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30751 (781Fh) GPIO6 OTP Control	15	GP6_DIR	1	GPIO6 pin direction 0 = Output 1 = Input	
	14:13	GP6_PULL [1:0]	01	GPIO6 Pull-Up / Pull-Down configuration 00 = No pull resistor 01 = Pull-down enabled 10 = Pull-up enabled 11 = Reserved	
	12	GP6_INT_MODE	0	GPIO6 Interrupt Mode 0 = GPIO interrupt is rising edge triggered (if GP6_POL=1) or falling edge triggered (if GP6_POL=0) 1 = GPIO interrupt is triggered on rising and falling edges	
	11	GP6_PWR_DOM	0	GPIO6 Power Domain select 0 = DBVDD 1 = SYSVDD	
	10	GP6_POL	1	GPIO6 Polarity select 0 = Inverted (active low) 1 = Non-Inverted (active high)	
	9	GP6_OD	0	GPIO6 Output pin configuration 0 = CMOS 1 = Open Drain	
	8	GP6_ENA	0	GPIO6 Enable control 0 = GPIO pin is tri-stated 1 = Normal operation	
	7:4	GP6_FN [3:0]	0000	GPIO6 Pin Function Input functions: 0 = GPIO input (long de-bounce) 1 = GPIO input 2 = Power On/Off request 3 = Sleep/Wake request	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
				4 = Sleep/Wake request (long de-bounce) 5 = Sleep request 6 = Power On request 7 = Watchdog Reset input 8 = DVS1 input 9 = DVS2 input 10 = HW Enable1 input 11 = HW Enable2 input 12 = HW Control1 input 13 = HW Control2 input 14 = HW Control1 input (long de-bounce) 15 = HW Control2 input (long de-bounce) Output functions: 0 = GPIO output 1 = 32.768kHz oscillator output 2 = ON state 3 = SLEEP state 4 = Power State Change 5 = Reserved 6 = Touch Panel Pen Down 7 = Touch Panel Conversion complete 8 = DC-DC1 DVS Done 9 = DC-DC2 DVS Done 10 = External Power Enable1 11 = External Power Enable2 12 = System Supply Good (SYSOK) 13 = Converter Power Good (PWR_GOOD) 14 = External Power Clock (2MHz) 15 = Auxiliary Reset	
	3:1	SYSOK_THR [2:0]	101	SYSOK threshold (rising SYSVDD) This is the rising SYSVDD voltage at which SYSOK will be asserted 000 = 2.8V 001 = 2.9V … 111 = 3.5V Note that the SYSOK hysteresis margin is added to these threshold levels.	

Register 781Fh GPIO6 OTP Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R30759 (7827h) ICE CHECK DATA	15:0	ICE_VALID_DATA [15:0]	0000_0000_0000_0000	This field is checked in development mode when an 'ON' transition is requested. A value of A596h is required to confirm valid data.	

Register 7827h ICE CHECK DATA

30 APPLICATIONS INFORMATION

30.1 TYPICAL CONNECTIONS

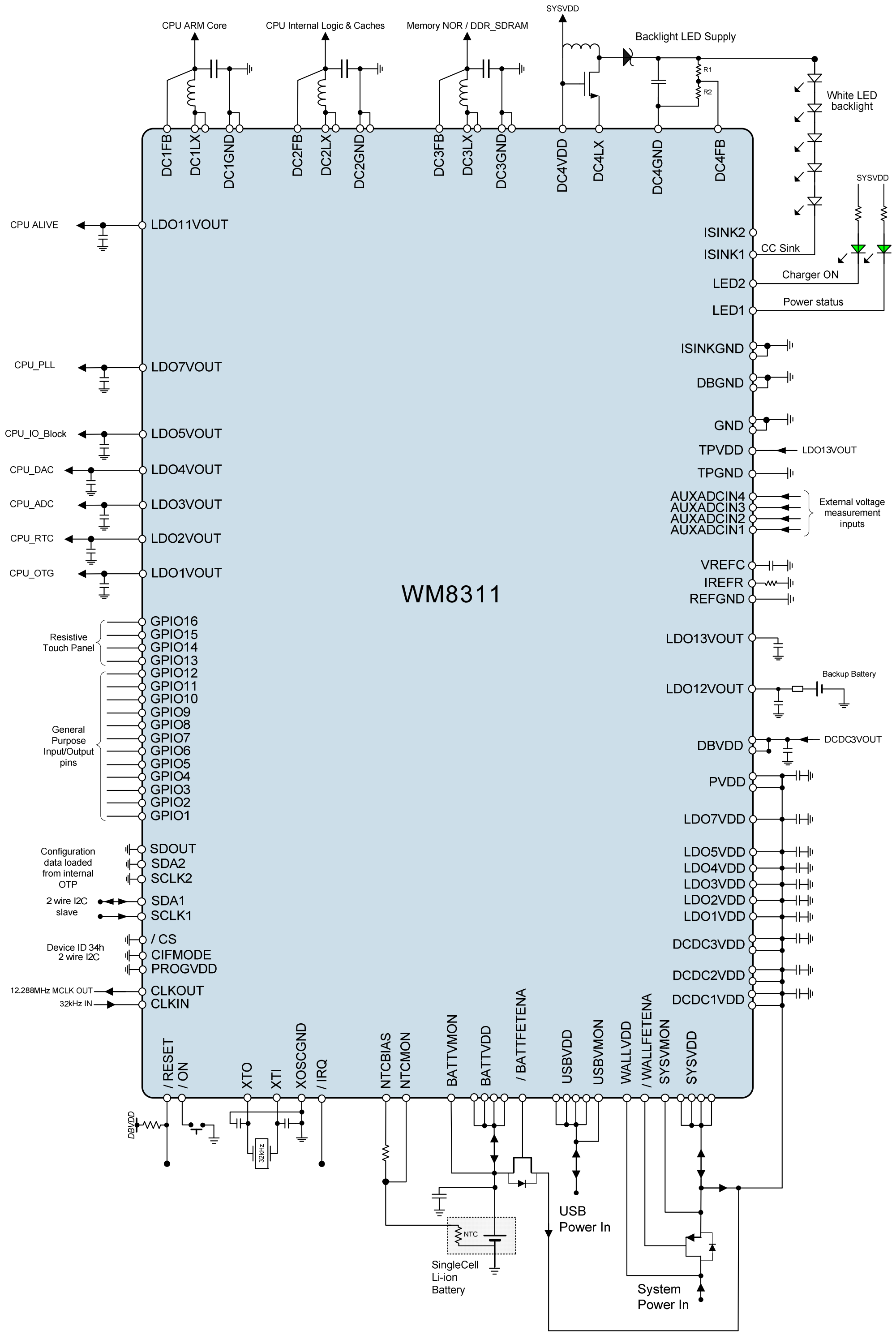


Figure 40 WM8311 Typical Connections Diagram

For detailed schematics, bill of materials and recommended external components refer to the WM8311 evaluation board users manual.

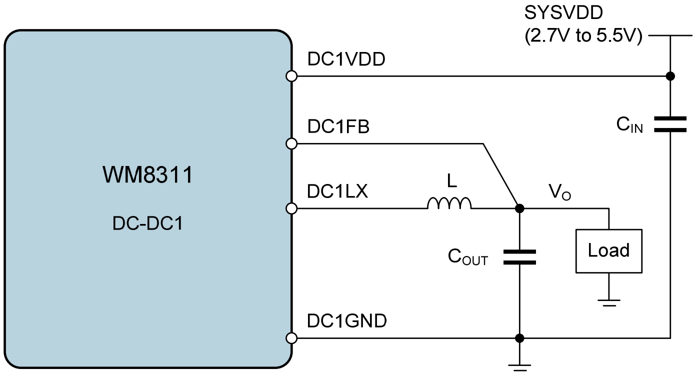
30.2 VOLTAGE AND CURRENT REFERENCE COMPONENTS

A decoupling capacitor is required between VREFC and REFGND; a 100nF X5R capacitor is recommended (available in 0201 package size). If USB100MA_STARTUP=1X (see Section 17.4), then a 50nF capacitor should be used.

A current reference resistor is required between IREFR and REFGND; a 100kΩ (1%) resistor is recommended.

30.3 DC-DC BUCK CONVERTER EXTERNAL COMPONENTS

The recommended connections to the DC-DC buck converters are illustrated in Figure 41.



Note: Equivalent circuit applies for DC-DC2 and DC-DC3

Figure 41 DC-DC Synchronous Buck Converter External Components

When selecting suitable capacitors, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. It should be noted that some components' capacitance changes significantly depending on the DC voltage applied. Ceramic X7R or X5R types are recommended.

The choice of output capacitor varies depending on the required transient response. Larger values may be required for optimum performance under large load transient conditions. Smaller values may be sufficient for a steady load, or in applications without stringent requirements on output voltage accuracy during load transients.

For layout and size reasons, users may choose to implement large values of output capacitance by connecting two or more capacitors in parallel. To ensure stable operation, the DC*m*_CAP register fields must be set according to the output capacitance, as described in Section 15.6.

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependant on the inductor value and can be determined by the following equation:

$$\triangle I_L = \frac{V_{OUT} \, . \, (1 - (V_{OUT} / V_{IN}))}{L \, . \, F_{SW}}$$

$\triangle I_L$ = Inductor ripple current
V_{OUT} = Output voltage
V_{IN} = Input voltage
L = Inductance
F_{SW} = Switching frequency

As a minimum requirement, the DC current rating should be equal to the maximum load current plus one half of the inductor current ripple:

$$I_{Lpeak} = I_{OUTmax} + (\triangle I_L / 2)$$

I_{Lpeak} = Inductor peak current
I_{OUTmax} = Maximum load current
$\triangle I_L$ = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the component's inductance is valid at the applicable operating temperature.

The WM8311 incorporates a current-limit protection feature for all DC-DC Buck Converter outputs. In order to achieve the benefit of this feature, the output inductor saturation current limit must be greater than or equal to the P-channel Current Limit for the applicable converter (see Section 7).

Wolfson recommends the following external components for use with DC-DC Converters 1 and 2.

The output inductor must be consistent with the DC*m*_FREQ register settings. The supported configurations are listed in Table 114. Note that for output voltages greater than 1.4V, the 2MHz mode must be used.

DCm_FREQ	SWITCHING FREQUENCY	OUTPUT INDUCTOR	COMMENTS
00	n/a	n/a	n/a
01	2MHz	2.2µH	Best efficiency
10	n/a	n/a	n/a
11	4MHz	0.5µH	Best transient performance

Table 114 Output Inductor Selection - DC-DC1, DC-DC2

The output capacitor must be consistent with the DC*m*_CAP register settings. For best performance, the 47µF component is recommended. For typical applications, the 22µF is suitable. The alternative values may be used for size or cost reasons if preferred.

COMPONENT	VALUE	PART NUMBER	SIZE
L	0.5µH	Coilcraft XPL2010-501MLB	2 x 2.5 x 1mm
	2.2µH	Coilcraft LPS3015-222ML TDK VLS252012T-2R2M1R3	3 x 3 x 1.5mm 2 x 1.25 x 1.2mm
C_{OUT}	47µF	MuRata GRM21BR60G476MEA1	0805
	22µF	MuRata GRM21BR60J226ME39	0805
	10µF	MuRata GRM188R60J106ME84	0603
	4.7µF	MuRata GRM188R60J475ME84	0603
C_{IN}	10µF	MuRata GRM188R60J106ME84	0603

Table 115 Recommended External Components - DC-DC1, DC-DC2

Wolfson recommends the following external components for use with DC-DC Converter 3.

Note that the switching frequency of DC-DC3 is fixed at 2MHz and the output inductor must be 2.2µH in all cases.

The output capacitor must be consistent with the DC3_CAP register setting. For best performance, the 47µF component is recommended. For typical applications, the 22µF is suitable. The alternative values may be used for size or cost reasons if preferred.

COMPONENT	VALUE	PART NUMBER	SIZE
L	2.2µH	Coilcraft LPS3015-222ML TDK VLS252012T-2R2M1R3	3 x 3 x 1.5mm 2 x 1.25 x 1.2mm
C_{OUT}	47µF	MuRata GRM21BR60G476MEA1	0805
	22µF	MuRata GRM21BR60J226ME39	0805
	10µF	MuRata GRM188R60J106ME84	0603
C_{IN}	4.7µF	MuRata GRM188R60J475ME84	0603

Table 116 Recommended External Components - DC-DC3

30.4 DC-DC (STEP-UP) CONVERTER EXTERNAL COMPONENTS

The recommended connections to the DC-DC (Step-Up) Converter are illustrated in Figure 42.

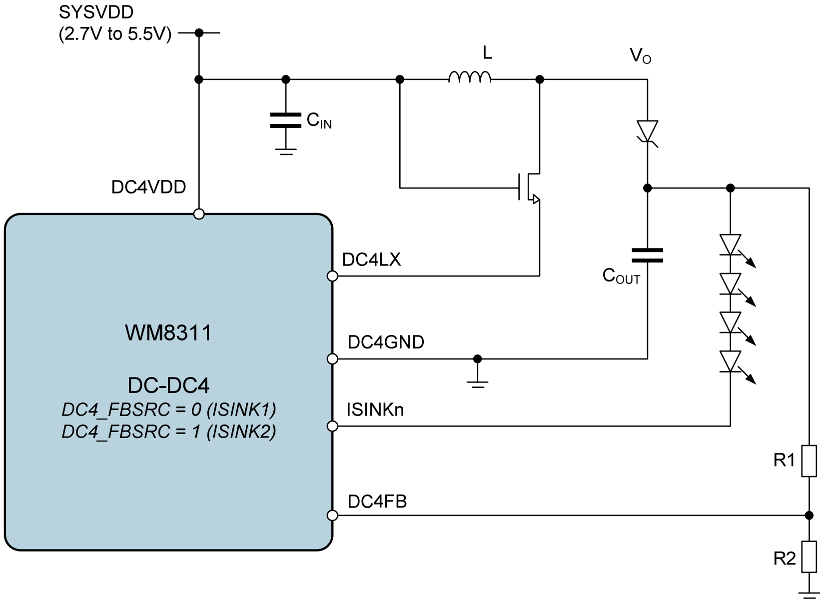


Figure 42 DC-DC (Step-Up) Converters External Components

In the constant current mode, the DC-DC Converter output voltage is controlled by the WM8311 in order to achieve the required current in ISINK1 or ISINK2. The required current is set by the CSn_ISEL register fields, as described in Section 16.2.2. A typical application for this mode would be a white LED driver, where several LEDs are connected in series to achieve uniform brightness.

The DC-DC (Step-Up) Converter is capable of generating output voltages of up to 30V. The maximum output voltage is determined by the two external resistors R1 and R2, which form a resistive divider between load connection and the voltage feedback pin DC4FB. The maximum output voltage is set as described in the following equation:

$$V_{OUT} = \frac{(R1/R2) + 1}{2}$$

Setting R2 to 47kΩ is recommended for most applications; R1 can be calculated using the following equation, given the required output voltage:

$$R1 = R2 \,.\, (2V_{OUT} - 1)$$

Note that the resistors determine the maximum output voltage. The actual voltage will be determined by the selected ISINK current, subject to the device limits.

When selecting a suitable capacitor, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended. The choice of output capacitor for DC-DC4 varies depending on the required output voltage. See Table 117 for further details.

When selecting a suitable output inductor, the inductance value and the saturation current must be compatible with the operating conditions of the converter.

The magnitude of the inductor current ripple is dependent on the inductor value and can be determined by the following equation:

$$\triangle I_L = \frac{V_{OUT} - V_{IN}}{L \cdot F_{SW}}$$

$\triangle I_L$ = Inductor ripple current
V_{OUT} = Output voltage
V_{IN} = Input voltage
L = Inductance
F_{SW} = Switching frequency

The inductor current is also a function of the DC-DC Converter maximum input current, which can be determined by the following equation:

$$I_{INmax} = \frac{I_{OUTmax}}{\text{efficiency}} \times \frac{V_{OUT}}{V_{IN}}$$

I_{OUTmax} = Maximum load current
I_{INmax} = Maximum input current
V_{OUT} = Output voltage
V_{IN} = Input voltage

As a minimum requirement, the DC current rating should be equal to the maximum input current plus one half of the inductor current ripple.

$$I_{Lpeak} = I_{OUTmax} + (\triangle I_L / 2)$$

I_{Lpeak} = Inductor peak current
I_{OUTmax} = Maximum load current
$\triangle I_L$ = Inductor ripple current

To be suitable for the application, the chosen inductor must have a saturation current that is higher than the peak inductor current given by the above equation. To maximise the converter efficiency, the inductor should also have a low DC Resistance (DCR), resulting in minimum conduction losses. Care should also be taken to ensure that the component's inductance is suitable at the applicable operating temperature.

When ISINK1 or ISINK2 is used in conjunction with DC-DC Converter 4, the ISINK should always be switched on before the DC-DC Converter is switched on. Conversely, the DC-DC Converter should always be switched off before the ISINK is switched off.

Wolfson recommends the following external components for use with DC-DC Converter 4.

The output capacitor C_{OUT} must be selected according to the required output voltage. For 10V output, 4.7μF is recommended. For 15V output, 3.3μF is recommended. For 20-30V output, 1.5μF is recommended.

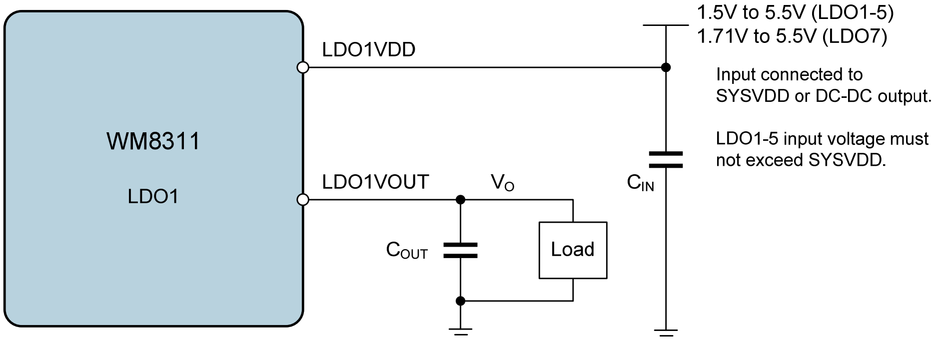
The resistors R1 and R2 must be selected according to the required output voltage - refer to the equations above. The values quoted below are suitable for 20V output.

COMPONENT	VALUE	PART NUMBER	SIZE
L	10μH	Taiyo-Yuden NR3015T100M	3 x 3 x 1.5mm
C_{OUT}	4.7μF	Murata GRM31CR61C475KA01	1206
	3.3μF	Murata GRM31CR71C335KA01	1206
	1.5μF	MuRata GRM31CR71H225KA88	1206
C_{IN}	2.2μF	MuRata GRM188R61A5KE34	0603
FET + schottky diode		Vishay SIA814DJ-T1-GE3	SC-70-6 2.05 x 2.05 x 0.75mm
R1	1.8MΩ	Phycomp 2322 7046 1805	0603
R2	47kΩ	Multicomp MIC 0.063W 0603 1% 47K	0603

Table 117 Recommended External Components - DC-DC4

30.5 LDO REGULATOR EXTERNAL COMPONENTS

The recommended connections to the LDO Regulators are illustrated in Figure 43.



Note: Equivalent circuit applies for LDO2, 3, 4, 5, 7.

Figure 43 LDO Regulators External Components

When selecting suitable capacitors, is it imperative that the effective capacitance is within the required limits at the applicable input/output voltage of the converter. Ceramic X7R or X5R types are recommended.

Wolfson recommends the following external components for use with LDO Regulators 1 to 5.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT}	2.2µF	Kemet C0402C225M9PAC	0402
C_{IN}	1.0µF	MuRata GRM155R61A105KE15	0402

Table 118 Recommended External Components - LDO1 to LDO5

Wolfson recommends the following external components for use with LDO Regulator 7. For this regulator, note that it is important that the output capacitance, C_{OUT}, does not exceed 4.7µF.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT}	1.0µF	MuRata GRM155R61A105KE15	0402
C_{IN}	1.0µF	MuRata GRM155R61A105KE15	0402

Table 119 Recommended External Components - LDO7

Wolfson recommends the following external components for use with LDO Regulators 11 to 13.

COMPONENT	VALUE	PART NUMBER	SIZE
C_{OUT} (LDO11)	0.1µF	MuRata GRM033R60J104KE19	0201
C_{OUT} (LDO12)	0.1µF	MuRata GRM033R60J104KE19	0201
C_{OUT} (LDO13)	2.2µF	Kemet C0402C225M9PAC	0402

Table 120 Recommended External Components - LDO11 to LDO13

30.6 BATTERY TEMPERATURE MONITORING COMPONENTS

Battery temperature monitoring is performed using a reference voltage output on the NTCBIAS pin. A potential divider is formed between the NTC bias resistor and the NTC thermistor component within the battery pack. The voltage present at the NTCMON pin is used to determine the battery temperature. The recommended connections and the derivation of V_{NTCMON} is shown in Figure 44.

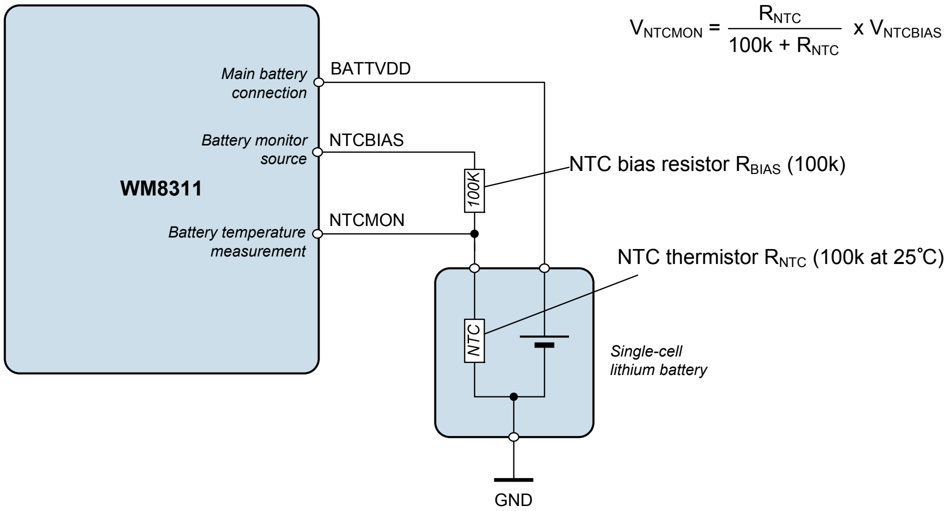


Figure 44 Battery Temperature Monitoring

The voltage thresholds for the Hot/Cold Battery Temperature conditions are fixed in the WM8311:

The Cold Battery condition is detected when $V_{NTCMON} > 0.765 \times V_{NTCBIAS}$

The Hot Battery condition is detected when $V_{NTCMON} < 0.348 \times V_{NTCBIAS}$

If the NTC thermistor has a nominal resistance of 100kΩ at 25°C, and follows the Vishay Resistance-Temperature Curve 1, then the above equations result in the Hot Battery threshold = 40°C and the Cold Battery threshold = 0°C.

For example, if the NTC thermistor resistance is 53.4kΩ at 40°C, then V_{NTCMON} is given by the following equation:

$$V_{NTCMON} = \frac{53.4}{100 + 53.4} \times V_{NTCBIAS}$$

$$V_{NTCMON} = 0.348 \times V_{NTCBIAS}$$

The upper and lower temperature thresholds can be adjusted by modification of the NTC bias resistor and/or the addition of another resistor between the battery pack and the NTCMON pin.

If only the NTC bias resistor is adjusted, then either the upper or lower threshold can be selected, but not both; the other threshold will be determined by the thermistor characteristics.

If an additional resistor is inserted between the battery pack and the NTCMON pin, then the upper and lower thresholds can be independently selected, with the constraint that the upper and lower thresholds must be at least 40°C apart.

To select a specific Hot Battery threshold, the required NTC bias resistor value may be calculated using the following equation:

$R_{BIAS} = (r_{HOT} / 0.534) \times R_{25}$

r_{HOT} is the NTC thermistor resistance ratio at the desired temperature threshold

R_{25} is the NTC thermistor resistance at 25°C

For example, at 60°C the Vishay Curve 1 resistance ratio, r_{HOT}, is 0.2488.

Therefore, to implement a 60°C Hot Battery threshold, assuming a 100kΩ NTC thermistor (at 25°C), the required NTC bias resistor is 46.6kΩ (nearest E12 value 47kΩ).

The resultant Cold Battery threshold is given using the r_{COLD} equation below. The r_{COLD} value needs to be referenced to the Vishay Curve 1 resistance chart in order to find the corresponding temperature.

To select a specific Cold Battery threshold, the required NTC bias resistor value may be calculated using the following equation:

$R_{BIAS} = (r_{COLD} / 3.255) \times R_{25}$

r_{COLD} is the NTC thermistor resistance ratio at the desired temperature threshold

R_{25} is the NTC thermistor resistance at 25°C

For example, at 5°C the Vishay Curve 1 resistance ratio, r_{COLD}, is 2.540.

Therefore, to implement a 5°C Cold Battery threshold, assuming a 100kΩ NTC thermistor (at 25°C), the required NTC bias resistor is 78kΩ (nearest E12 value 82kΩ).

The resultant Hot Battery threshold is given using the r_{HOT} equation below. The r_{HOT} value needs to be referenced to the Vishay Curve 1 resistance chart in order to find the corresponding temperature.

To select both the Hot Battery threshold and the Cold Battery threshold, an additional resistor, R1, is required, as illustrated in Figure 45.

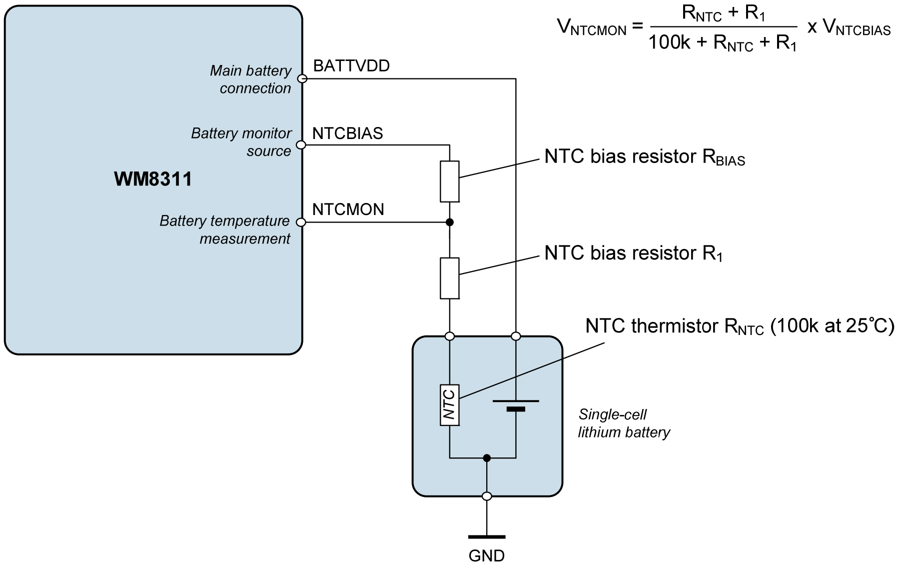


Figure 45 Battery Temperature Threshold Selection

Under the circuit configuration above, the NTC bias resistors R_{BIAS} and R_1 are calculated using the following equations:

$$R_{BIAS} = ((r_{COLD} - r_{HOT}) / 2.721) \times R_{25}$$

$$R_1 = (0.534 \times R_{BIAS}) - (r_{HOT} \times R_{25})$$

For example, to select a 45°C Hot Battery threshold and a 0°C Cold Battery threshold, the applicable resistance ratios are $r_{HOT} = 0.4368$ and $r_{COLD} = 3.266$.

Assuming a 100kΩ NTC thermistor (at 25°C), then R_{25} = 100kΩ.

From the equations above, it follows that R_{BIAS} = 104kΩ (nearest E12 value 100kΩ).

Assuming the E12 (100kΩ) value of R_{BIAS}, then R_1 = 9.72kΩ (nearest E12 value 10kΩ).

30.7 PCB LAYOUT

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. Poor regulation and instability can result.

Simple design rules can be implemented to negate these effects:

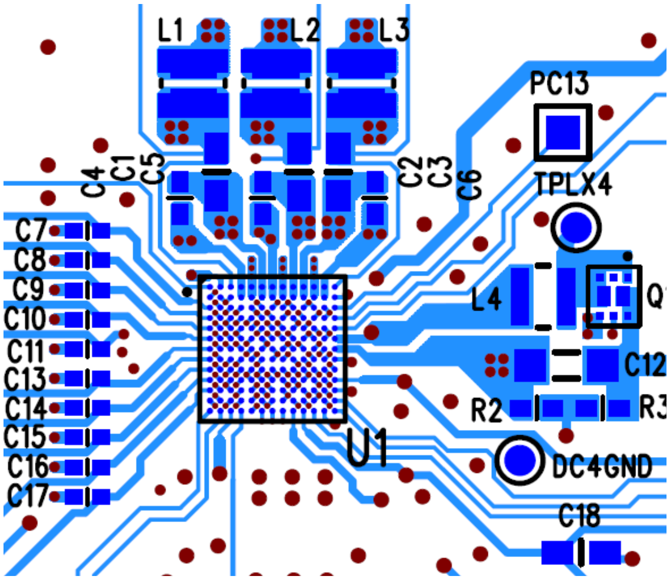
External input and output capacitors should be placed as close to the device as possible using short wide traces between the external power components. For the DC-DC Converters, the input capacitor placement takes priority on the DC-DC converters. (For the LDO Regulators, the placement of the input and output capacitors have equal priority.)

Route the DC-DC converter output voltage feedback as an independent connection to the top of the output capacitor to create a true sense of the output voltage, routing away from noisy signals such as the LX connection.

Use a local ground island for each individual DC-DC converter connected at a single point onto a fully flooded ground plane.

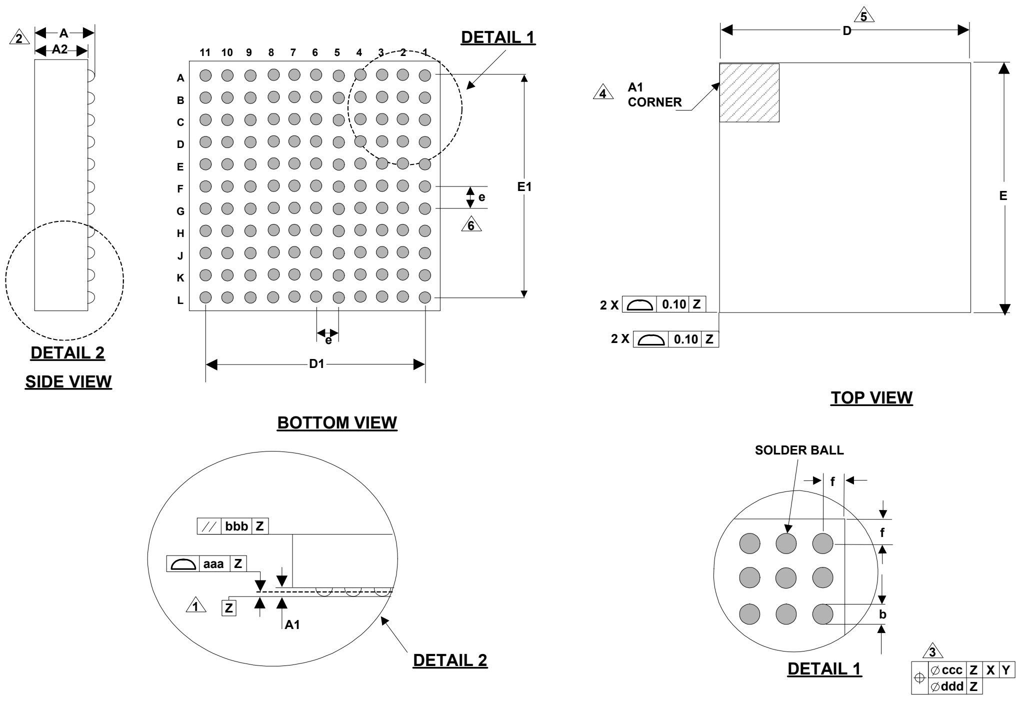
Current loop areas should be kept as small as possible with loop areas changing little during alternating switching cycles.

Studying the layout below shows, for example, DC-DC1 layout with external components C3, L3 and C6. The input capacitor, C6, is close into the IC and shares a small ground island with the output capacitor C3. The inductor, L3, is situated in close proximity to C3 in order to keep loop area small and minimise the trace resistance. Note also the use of short wide traces with all power tracking on a single (top) layer. Note that the illustration below shows the WM8310 device, not the WM8311.



31 PACKAGE DIAGRAM

B: 121 BALL BGA PLASTIC PACKAGE 8 x 8 x 1.17 mm BODY, 0.65 mm BALL PITCH **DM065.A**



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	1.08	1.17	1.27	
A1	0.17	0.21	0.26	
A2	0.91	0.96	1.01	
b	0.25	0.30	0.35	
D		8.00 BSC		
D1		6.50 BSC		
E		8.00 BSC		
E1		6.50 BSC		
e		0.65 BSC		6
f		0.75 BSC		
	Tolerances of Form and Position			
aaa	0.08			
bbb	0.10			
ccc	0.15			
ddd	0.05			
REF:	JEDEC, MO-195			

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT ‘A1’.
3. DIMENSION ‘b’ IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -Z-.
4. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
5. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
6. ‘e’ REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
8. FALLS WITHIN JEDEC, MO-195

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33 REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	CHANGED BY
18/02/10	3.1	Updated definition of DCn_SOFT_START registers RST_DUR description updated Updated description of AUX_CVT_ENA and TCH_CVT_ENA, noting that measurement data is not available until the associated interrupt is set. AUXADC input impedance corrected to 400kohm.	PH
24/06/10	3.1	Amended LDO12 current capability to 2mA. Amended LDO13 current capability to 20mA DC4 maximum current spec restored to 90mA. DC4 Elec Chars updated to include 90mA for Vload ≤ 8V. DC4_RANGE updated to support Vout >= 6.5V only. Amended Test Conditions for LDO4, 5 to be same as others. Clarified (in Section 13) the 32.768kHz GPIO output only supported in OFF state if the selected power domain remains on. Clarified (in Section 21) the External Power Clock is controlled in the power sequences via EPE1 or EPE2. Updated wording and terminology, making consistent with other PMIC datasheets. Review input from WM8321 incorporated as applicable. DORW replaced with DCRW. DBE replaced with InstantConfig™ EEPROM (ICE). Added SDOUT1 pull-up requirement. Typical connections drawing updated to show XOSCGND close to XTI/XTO pins and to include DC-DC output capacitors.	PH
22/07/10	3.1	Noted maximum output capacitance for LDO7 (4.7uF). Updates regarding Battery Charger Interrupts preventing SLEEP transitions - CHG_START_EINT must be cleared first. Clarification added to CLKOUT function when XTAL_INH=1. DBVDD1, DBVDD2 domains merged into DBVDD. PVDD1, PVDD2 domains merged into PVDD. Watchdog description updated wrt Device Reset response. SDOUT1 description updated as an Open Drain output, with pull-up resistor required. “Register Map by Address” section updated. Default value of PWRSTATE_DLY corrected.	PH
24/11/10	3.1	CE000609 errata added (OTP Command End Interrupt) CE000610 errata added (DC3 quiescent current in LDO mode) CE000611 errata added (Power Sequence in failure conditions) CE000613 errata added (DC4 Hardware Control) CE000614 errata added (FLL Register readback) CE000649 errata added (Watchdog timeout)	PH
3/12/10	3.1	Undervoltage margin specified for DC-DC converters 1,2,3. Overvoltage margin specified for DC-DC converters 1,2. Chip Temperature (AUX_DATA) equation updated. NTCBIAS voltage added to Electrical Characteristics.	PH
7/3/11	3.1	RTC_PINT_FREQ definition updated. Added notes that SLEEP > OFF is not a controlled transition; converters and regulators are disabled immediately. RESET pin description updated to note integrated pull-up. IRQ description updated to note pull-up in Open Drain mode. System Reset and Device Reset descriptions updated, consistent with the Summary Table. Recommended external pull-up resistances added in Pin Description. Internal pull-up / pull-down resistances added in Electrical Characteristics. CE000612 errata added (GPn_POL in development mode)	PH

DATE	REV	DESCRIPTION OF CHANGES	CHANGED BY
28/03/11	3.1	Noted maximum limit on Software Resets. Also clarification of the maximum number of Watchdog / Undervoltage Device Resets. CE000607 errata added (Device start-up, USB_ILIM < 100mA). CE000608 errata added (Power up failure, USB100MA_STARTUP = 10 or 11).	PH
28/06/11	3.1	DC-DC output inductor saturation limit recommendations added. SYSOK_THR register description updated.	PH
21/09/11	3.1	Backup battery power updated; Backup charger control registers deleted. LDO11 output amended for LDO11_VSEL_SRC=1 and DC-DC1 disabled.	PH
02/05/12	3.1	Electrical Characteristics updated LDO7, 8, 9, 10 input voltage range updated. LDO11 current rating updated.	PH