ALC5628

I²S/PCM STEREO DAC WITH HEADPHONE AND MONO CLASS-D SPEAKER AMPLIFIER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5628 Audio DAC IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	-	Preliminary release.
1.1	-	Preliminary release.
1.2	2009/06/26	First release.

Table of Contents

List of Tables

List of Figures

1. General Description

The ALC5628 is a highly-integrated I^2S/PCM interface audio DAC with multiple input/output ports and is designed for Multimedia and Communication handheld devices. It provides a Stereo Hi-Fi DAC for playback via the I^2S/PCM interface and is controlled by the I^2C interface.

To reduce component count, the device can connect to:

- LINE_IN stereo Single-Ended analog inputs (can be configured to mono Differential analog input)
- Single-Ended stereo Headphone
- MONO or Stereo Bridge-Tied Load (BTL) Speaker

Multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices. Differential input/output connections efficiently reduce noise interference, providing better sound quality. The Class-D amplifier can be directly connected to a 2.4 Watt Mono Speaker, removing the need for an additional amplifier, further cutting both cost and required board area.

The ALC5628 AVDD operates at supply voltages from 2.3V to 3.6V. DCVDD and DBVDD operate from 1.8V to 3.6V, and SPKVDD operates from 2.3V to 5V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10μA.

The ALC5628 is available in a 4x4mm 'Green' QFN-24 package, making it ideal for use in handheld portable systems.

2. Features

- Digital-to-Analog Converter with 100dB SNR and –86dB THD+N at 3.3V
- Two analog stereo single-ended or one stereo differential input, LINEIN_L/R
- BTL (Bridge-Tied Load) Class-D Speaker output with on-chip 2.4W speaker driver (SPKVDD=5V, 4Ω load)
- Supports playback soft-mute, digital volume, digital AVC
- Stereo headphone output with on-chip 45mW headphone driver (AVDD=3.3V, 16Ω load)
- Supports pop noise suppression with external capacitor
- Digital power supplied from 1.8V to 3.6V
- Analog power and headphone power supplied from 2.3V to 3.6V
- Power management and enhanced power saving
- Internal PLL can receive wide range of clock inputs
- Supports crystal oscillator
- Supports sampling rate 8KHz ~ 192KHz
- Supports I^2C control interface
- Supports three programmable data interfaces
  - I^2S, left justified or DSP
  - 16/20/24-bit word lengths
  - Master or Slave clock mode
- Speaker amplifier power supplies from 2.3V to 5V
- 24-pin QFN 4x4mm package for small footprint

3. System Applications

- Portable media player
- MP3 player
- Bluetooth A2DP (Advanced Audio Distribution Profile) headsets
- Portable Navigation Device (PND)

4. Block Diagram

4.1. Function Block

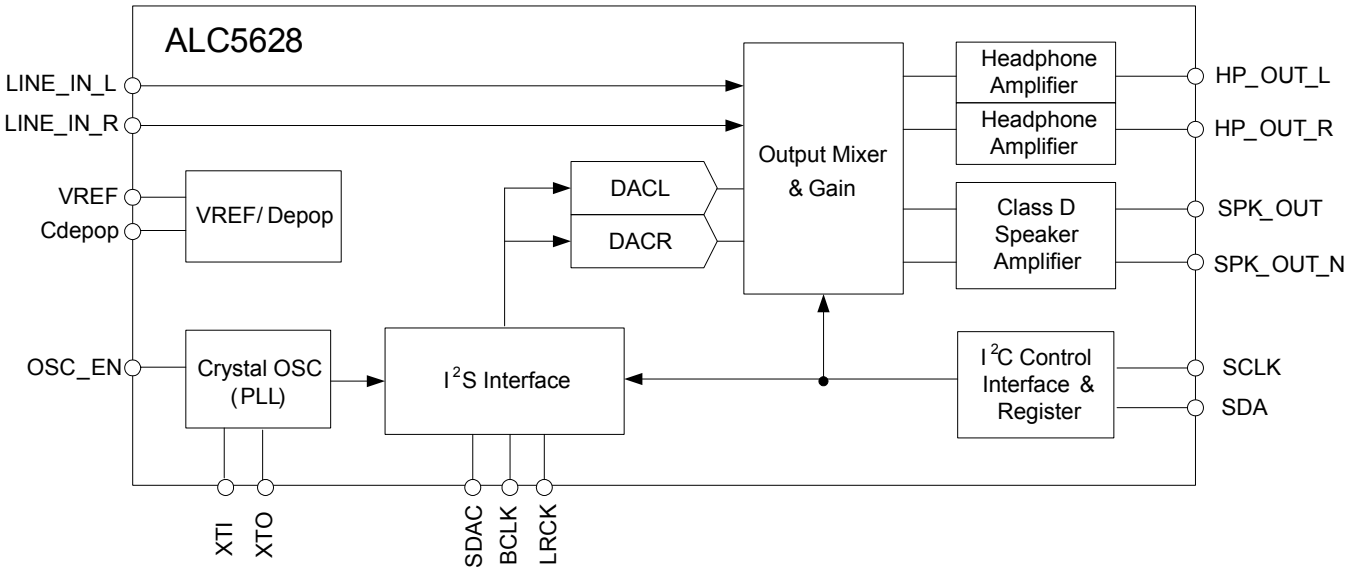


Figure 1. Block Diagram

4.2. Audio Mixer Path

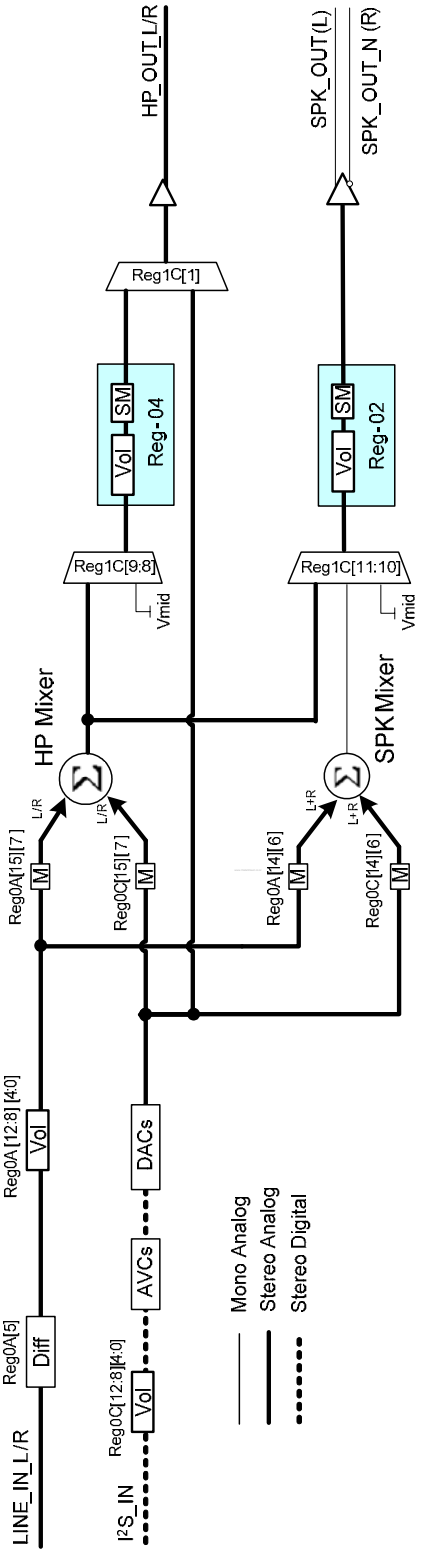


Figure 2. Audio Mixer Path

5. Pin Assignments

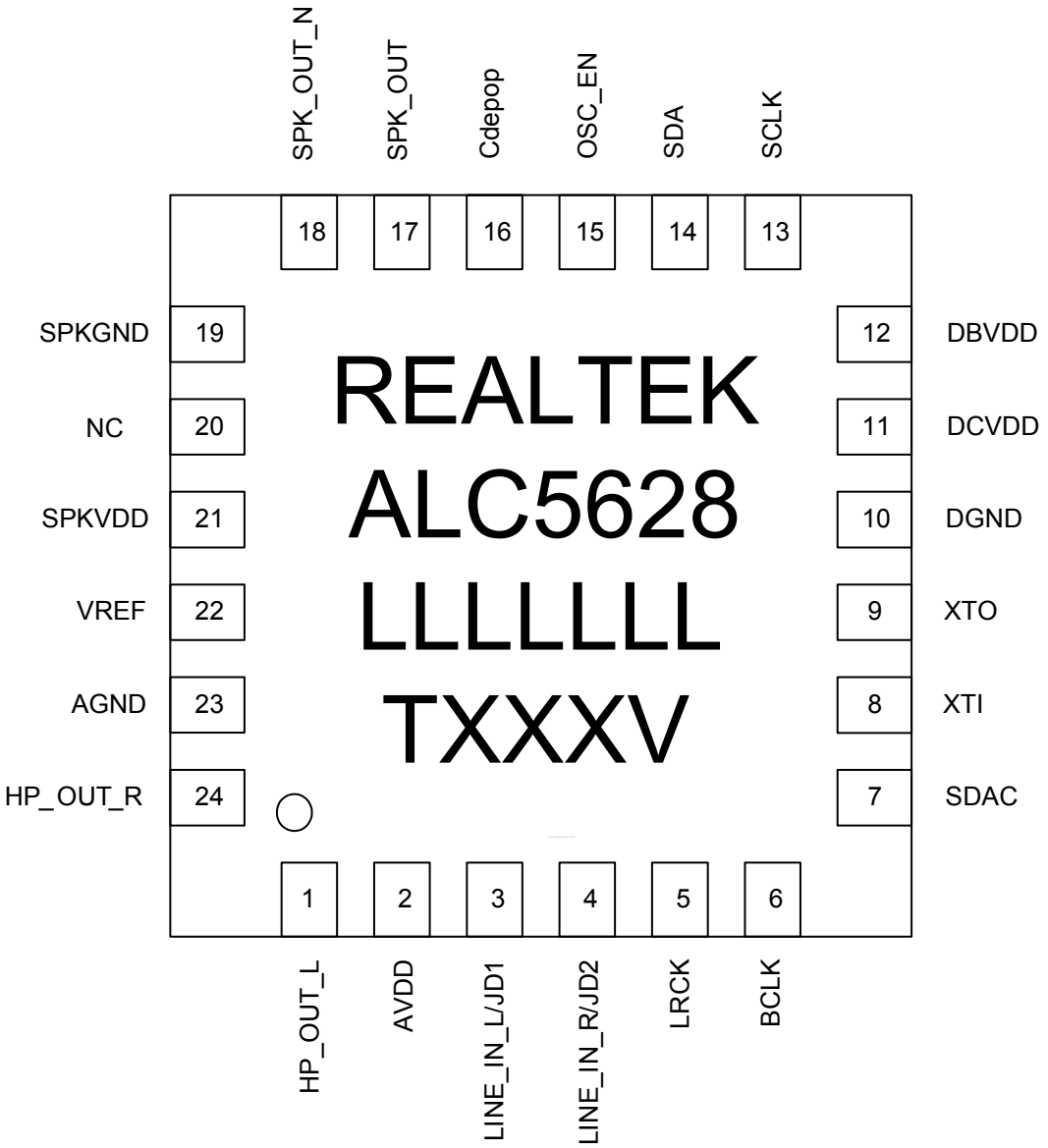


Figure 3. Pin Assignments

5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3.

6. Pin Descriptions

6.1. Digital I/O

Table 1. Digital I/O Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
LRCK	IO	5	Digital Audio Input Frame Sync	Schmitt Trigger Input, Output
BCLK	IO	6	Digital Audio Serial Clock	Schmitt Trigger Input, Output
SDAC	I	7	Digital Audio Serial Data Input	Schmitt Trigger Input
XTI	I	8	Crystal Input	Schmitt Trigger Input
XTO	O	9	Crystal Output	Schmitt Trigger Output
SCLK	I	13	I^2C: Clock Input	Schmitt Trigger Input
SDA	IO	14	I^2C: Data Input And Output	Schmitt Trigger Input, Output
OSC_EN	I	15	Crystal Oscillator Enable Control, Connect to VDD or GND VDD: Crystal enabled GND: Crystal disabled	Schmitt Trigger Input

6.2. Analog I/O

Table 2. Analog I/O Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
LINE_IN_L/JD1	I	3	Line Input Left Channel, Jack Detect_1	Analog Input
LINE_IN_R/JD2	I	4	Line Input Right Channel, Jack Detect_2	Analog Input
SPK_OUT	O	17	Speaker Out Left Channel or Positive Out	Speaker Amplifier Output
SPK_OUT_N	O	18	Speaker Out Right Channel, Negative Right Channel, or Negative Output	Speaker Amplifier Output
HP_OUT_L	O	1	Headphone Out Left Channel	Analog Amplifier Output
HP_OUT_R	O	24	Headphone Out Right Channel	Analog Amplifier Output

6.3. Filter/Reference

Table 3. Filter/Reference Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
Cdepop	IO	16	De-Pop Capacitor, Connect 1µF Capacitor to Analog GND	Capacitor to Analog Ground
VREF	O	22	Reference Voltage Output, Connect 4.7µF Capacitor to Analog GND	Capacitor to Analog Ground

6.4. Power/Ground

Table 4. Power/Ground Pins

Pin Name	Type	Pin No	Description	Characteristic Definition
DGND	P	10	Digital GND	-
DCVDD	P	11	Digital VDD	1.8V~3.6V (Core)
DBVDD	P	12	Digital VDD	1.8V~3.6V (IO Buffer)
SPKGND	P	19	Speaker Amplifier GND	-
SPKVDD	P	21	Speaker Amplifier VDD	2.3V~5V
AGND	P	23	Analog GND	-
AVDD	P	2	Analog VDD	2.3V~3.6V
SPKGND	P	Exposed Pad	Speaker Amplifier GND Must be Connected to System DGND	-
NC	-	20	Not Connected	-

7. Functional Description

7.1. Power

The ALC5628 has many power blocks. The power supply limit conditions are DBVDD≥DCVDD and SPKVDD≥AVDD≥DCVDD. To prevent pop noise, we suggest that DCVDD is powered on before AVDD.

7.2. Reset

There are two types of reset operation: Power-On-Reset (POR) and Register reset.

Table 5. Reset Operation

Reset Type	Trigger Condition	Codec Response
POR	Monitor Digital Power Supply Voltage Reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write Reg00	Reset all registers to default values.

7.2.1. Power-On Reset (POR)

When power is on, DCVDD passes through the V_{POR} band of the ALC5628 (V_{PORH}~V_{PORL}). A Power-On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 6. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note: The V_{POR_OFF} must be below V_{POR_ON}.

7.3. Clocking

The ALC5628 supports a Crystal as internal system clock. When the OSC_EN pin is kept high or floating, the audio system clock can be selected from XTI/XTO or PLL. When a crystal is applied, 256/384/512/768Fs is required from XTI/XTO. If using internal PLL as audio internal clock, set the PLL output to 512Fs.

A Phase-Lock Loop (PLL) is used to provide a flexible input clock from 2.048MHz (64Fs of 32kHz) to 40MHz. Typical choices are 2.048MHz, 4.096MHz, and 13MHz. The source of the PLL can be set to XTI or BCLK by setting sel_pll_sour (Reg42[14]). Firmware can setup the PLL to output the desired frequency for the system clock.

The PLL transmit formula is: F_{OUT} = (XTI*(N+2)) / ((M+2)*(K+2)) (Typical K=2)

Table 7. PLL Clock Setting Table for 48K (Unit: MHz)

XTI	M Code	N Code	Fvco	K Code	Fout
2.048	0	94	98.304	2	24.576
3.6864	1	78	98.304	2	24.576
4.096	0	46	98.304	2	24.576
12	14	129	98.25	2	24.5625
13	14	119	98.3125	2	24.57812
15.36	3	30	98.304	2	24.576
16	5	41	98.28571	2	24.57143
19.2	15	85	98.25882	2	24.5647
19.68	0	8	98.4	2	24.6

Table 8. PLL Clock Setting Table for 44.1K (Unit: MHz)

XTI	M Code	N Code	Fvco	K Code	Fout
2.048	0	86	90.112	2	22.528
3.6864	0	47	90.3168	2	22.5792
4.096	9	241	90.48436	2	22.62109
12	15	126	90.35294	2	22.58824
13	15	116	90.23529	2	22.55882
15.36	15	98	90.35294	2	22.58824
16	12	77	90.28571	2	22.57143
19.2	15	78	90.35294	2	22.58824
19.68	15	76	90.29647	2	22.57412

7.4. I²C Control Interface

I²C is a 2-wire half-duplex serial communication interface, supporting only slave mode.

7.4.1. Addressing Setting

(MSB)			BIT				(LSB)
0	0	1	1	0	0	0	RW

7.4.2. Complete Data Transfer

Data Transfer over I²C Control Interface

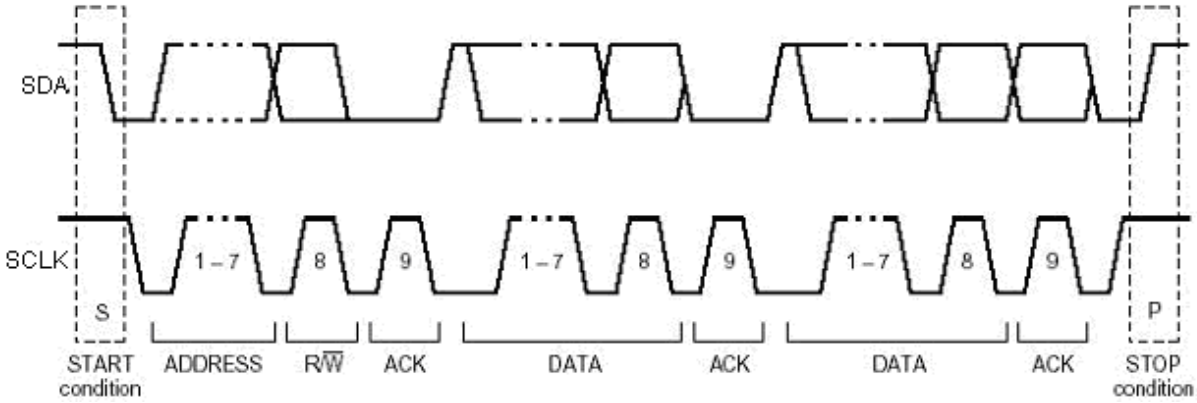


Figure 4. Data Transfer Over I²C Control Interface

Write WORD Protocol

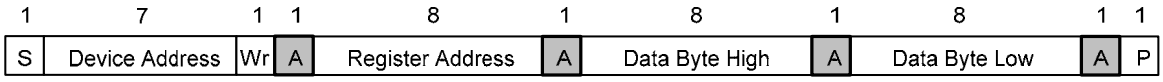
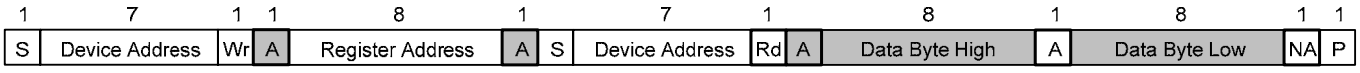


Figure 5. Write WORD Protocol

Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

Figure 6. Read WORD Protocol

7.4.3. Odd-Addressed Register Access

The ALC5628 will return '0000h' when odd-addressed and unimplemented registers are read.

7.5. Digital Data Interface

7.5.1. I²S/PCM Interface

The Digital to Analog Converter (DAC) serial data is input via the SDAC pin. The serial data is shifted in on the rising edge of BCLK (ctrl_i2s_bclk_polarity=0'b) or the falling edge (ctrl_i2s_bclk_polarity=1'b). The Left/Right Clock (LRCK) signal is the frame sync signal. Left/Right data can be swapped by en_dac_lrck_swap.

The ALC5628 I²S/PCM interface can be configured to Master mode or Slave mode. In Master mode (sel_i2s_mode=0'b), BCLK and LRCK are configured as output. In Slave mode (sel_i2s_mode=1'b), BCLK and LRCK are configured as input. The XTI provides BCLK synchronized clock externally as Stereo System Clock.

The ALC5628 supports three independent I²S/PCM interfaces for Stereo Audio data formats:

- PCM/DSP mode
- Left justified mode
- I²S mode

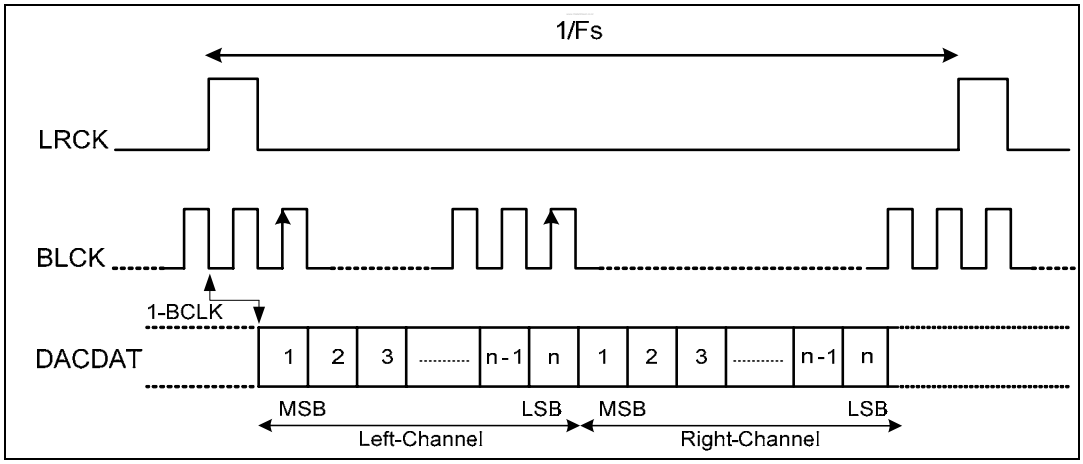


Figure 7. PCM Stereo Data Mode A Format-1 (sel_i2s_data_format=10'b, ctrl_i2s_bclk_polarity=0'b)

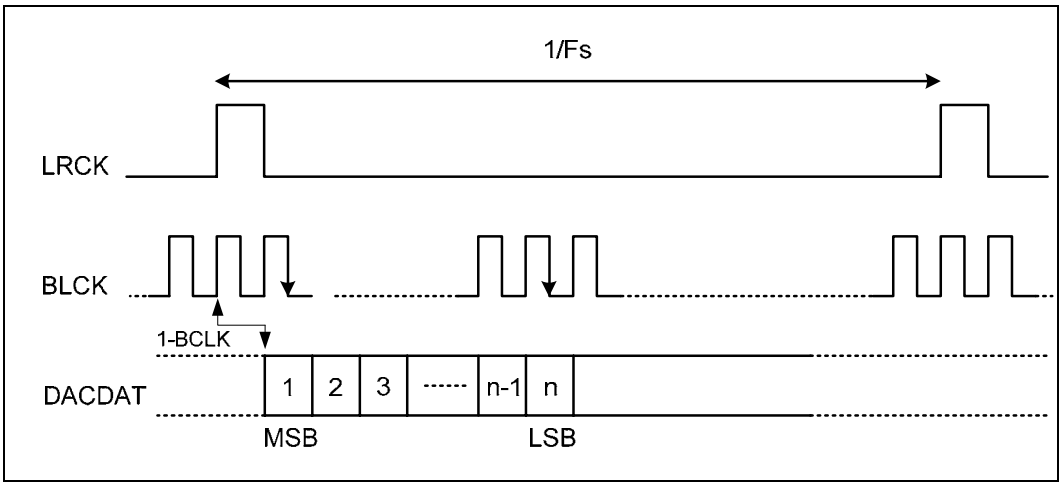


Figure 8. PCM Stereo Data Mode A Format-2 (sel_i2s_data_format=10'b, ctrl_i2s_bclk_polarity=1'b)

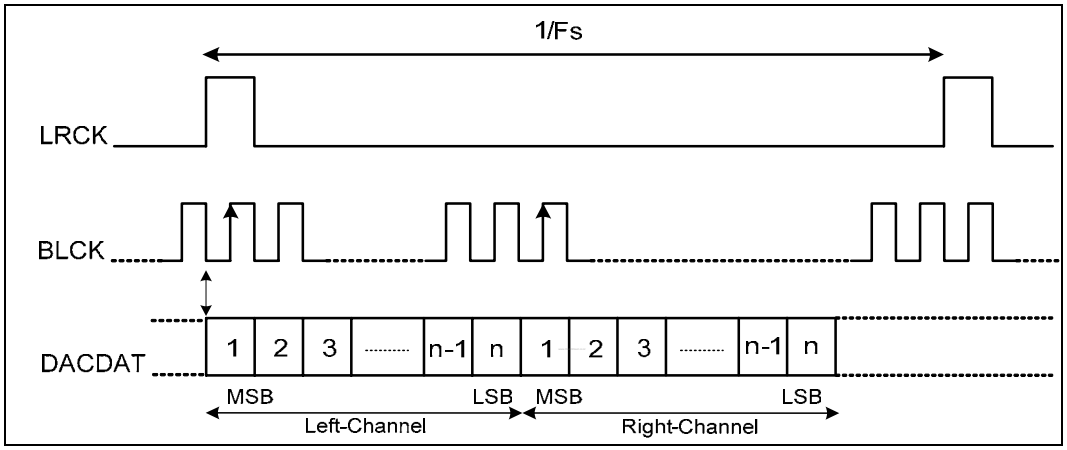


Figure 9. PCM Stereo Data Mode B Format (sel_i2s_data_format=11'b, ctrl_i2s_bclk_polarity=0'b)

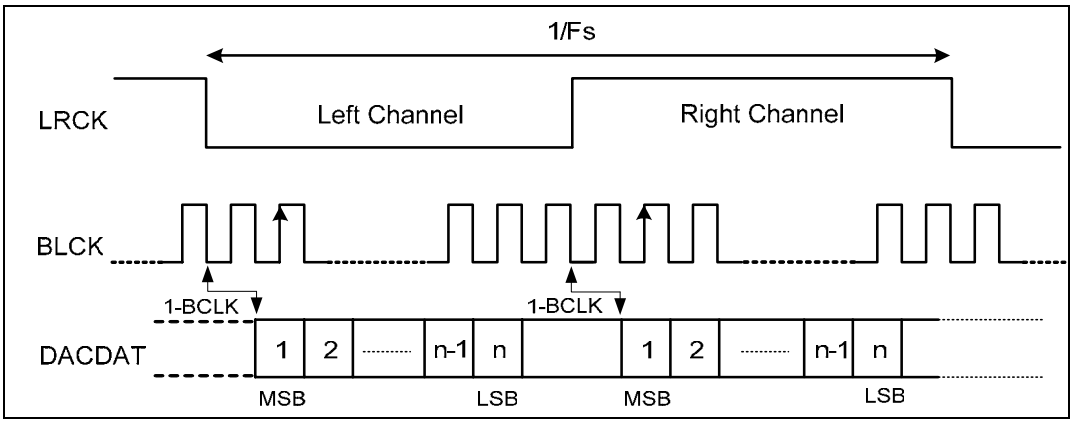


Figure 10. I²S Data Format (sel_i2s_data_format=00'b)

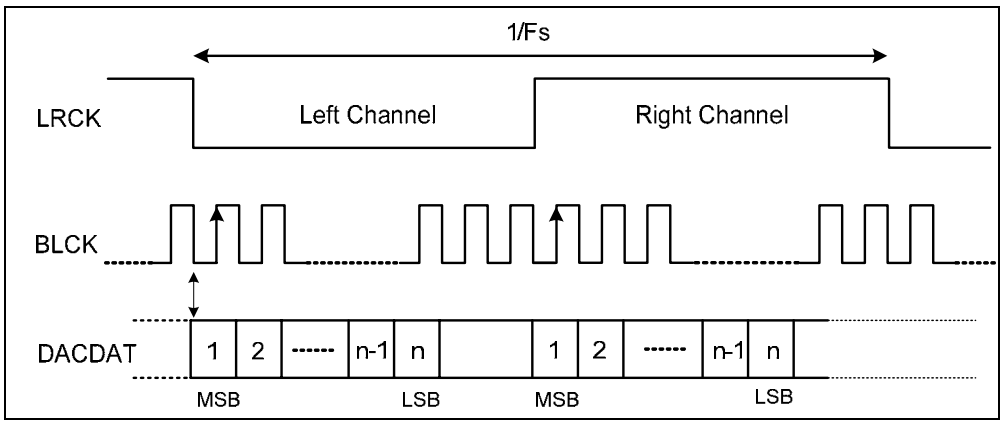


Figure 11. Left-Justified Data Format (sel_i2s_data_format=01'b, ctrl_i2s_bclk_polarity=0'b)

7.6. Analog Signal Path

7.6.1. Line Input

LINE_IN_L and LINE_IN_R provide 2-channel stereo single-ended inputs that can be mixed into any analog output mixer. In addition, LINE_IN_L and LINE_IN_R can be configured as mono channel differential input by Reg0A[5]: en_li_diff, which only can output to the HP mixer.

- LINE_IN_L/R volume and mute are controlled by Reg0A
- sel_li_l_vol and sel_li_r_vol can be used to power down LINE_IN volume control
- LINE_IN_L is pin shared with JD1 and can be configured by sel_jd_source
- LINE_IN_R is pin shared with JD2 and can be configured by sel_jd_source

7.6.2. Speaker Output

SPK_OUT provides one-channel differential output and can be configured to dual single-ended output.

The SPK_OUT source is selected in sel_spk_vol_in, as listed below:

- No Input (V_{MID})
- Headphone mixer
- Speaker mixer

The ALC5628 Speaker-out supports a Class-D type amplifier. As the power voltage of SPKVDD is usually higher than AVDD, it must set Class-D V_{MID} ratio at spk_ampd_ratio_clsd in order to extend the output level.

The SPK_OUT volume and mute are controlled by Reg02. Reg3E[12]: pow_spk_vol can be used to power down Speaker output. Reg3C[14]: pow_clsd is used to power down the Class-D amplifier.

SPK_OUT supports 'Soft Volume Delay Mute' and 'Zero-Crossing Detect' functions which can be enabled by Reg5C[15]:en_sp_l_dezero, Reg5C[14]:en_sp_l_softvol, Reg5C[13]:en_sp_r_dezero, and Reg5C[12]:en_sp_r_softvol.

7.6.3. Headphone Output

HP_OUT_L/R provides 2-channel single-ended output. The source of HP_OUT_L/R can be selected from sel_hp_l_in & sel_hp_r_in as below.

- V_{MID}
- Headphone mixer

The HP_OUT_L/R volume and mute are controlled by Reg04. Besides, Reg3E[10]: pow_hp_l_vol and Reg3E[9]: pow_hp_r_vol can be used to power down the HP output volume.

HP_OUT supports 'Soft Volume Delay Mute' and 'Zero-Crossing Detect' functions which can be enabled by Reg5C[11]:en_hp_l_dezero, Reg5C[10]:en_hp_l_softvol, Reg5C[9]:en_hp_r_dezero, and Reg5C[8]:en_hp_r_softvol.

HP_OUT_L/R source can be selected from DAC Stereo output (Reg1C[1]: en_dac_hp) for high quality performance playback.

7.6.4. Stereo DAC

The stereo DAC can be configured to different sample rates by driving 256Fs/384Fs into audio SYSCLK, and individually set by sel_i2s_bclk_ms (Reg38[12]).

dac_l_vol & dac_r_vol can be used to control the DAC output volume.

7.6.5. Headphone Mixer

The headphone (HP) mixer is used to drive stereo output, including HP_OUT_L/R and SPK_OUT (P/N) (SPK_OUT_L/R).

The following signals can be mixed into the headphone mixer:

- LINE_IN_L/R (Controlled by Reg0A)
- Stereo DAC output (Controlled by Reg0C)

When the SPK_OUT source is from HP mixer, SPK_OUT can be configured to stereo single-ended or mono differential output by setting spkon_source_clsd (Reg1C[15:14]). The headphone mixer can be powered down by setting pow_mix_hp_l (Reg3C[5]) & pow_mix_hp_r (Reg3C[4]).

7.6.6. Speaker Mixer

The speaker (SPK) mixer is used to drive SPK_OUT.

The following signals can be mixed into the speaker mixer:

- LINE_IN_L/R (Controlled by Reg0A)
- Stereo DAC output (Controlled by Reg0C)

Note: The speaker mixer can be powered down by setting pow_mix_spk (Reg3C[3]).

7.7. Power Management

The ALC5628 supports detailed Power Management control registers within Reg3A, 3C, and 3E. Each particular block will be active only when individual bits of Reg3A, 3C, and 3E are set to enable.

7.8. Headphone Depop

The ALC5628 provides a headphone depop mechanism in order to eliminate the pop noise of headphone out. An external 1μF Capacitor is required in this application. Refer to the ALC5628 Application Notes (separate document) for details.

7.9. AVC Control

The Automatic Volume Control (AVC) function dynamically adjusts the input signal quantized by DAC to an expected sound level by setting THmax and THmin.

When the average level of input signal quantized by DAC is higher than THmax, the AVC will decrease the selected analog gain to attenuate the quantized Pulse Code Modulation (PCM) signal to a lower amplitude than THmax. When the average level of input signal quantized by DAC is lower than THmin, the AVC will increase the selected analog gain to amplify the input signal. The quantized PCM signal is then set to a higher amplitude than THmin. The quantized PCM has an average level between THmin and THmax.

In order to avoid outputting a strong amplified signal when the gain detector input level is transiting from a very small signal to a normal signal, the AVC block will limit the selected analog gain to unit gain (=0dB) when the input level of the gain detector is lower than THnonact.

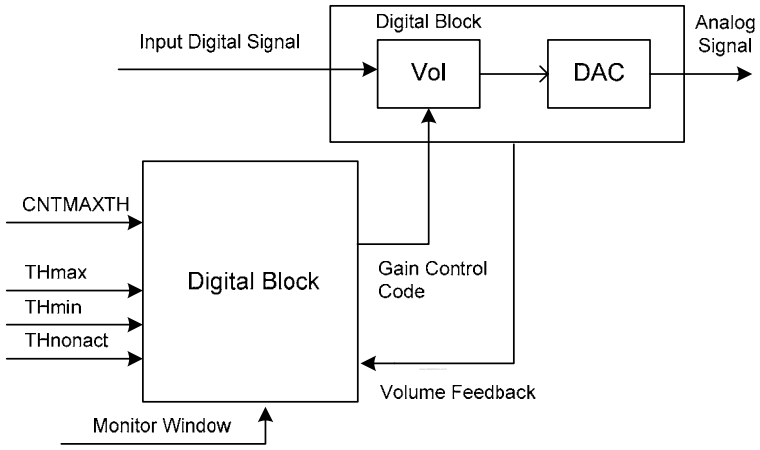


Figure 12. AVC Block of DAC Module

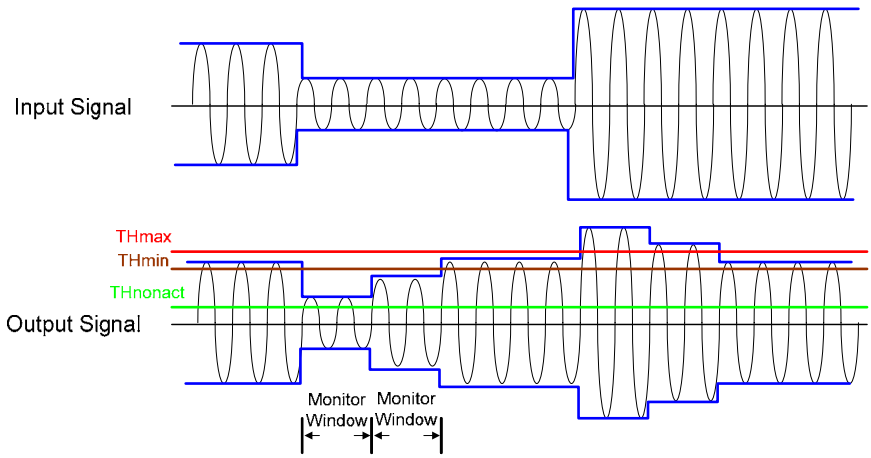


Figure 13. AVC Behavior

7.10. Zero Cross

When Zero-Cross detect is enabled, the ALC5628 will change each output volume or mute only if the signal swing crosses the zero point. This function can avoid pop noise when volume is changed or muted.

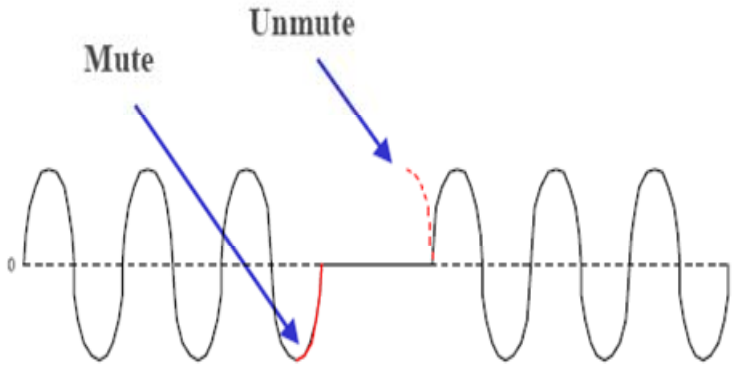


Figure 14. Zero Cross Disabled when Output Muted

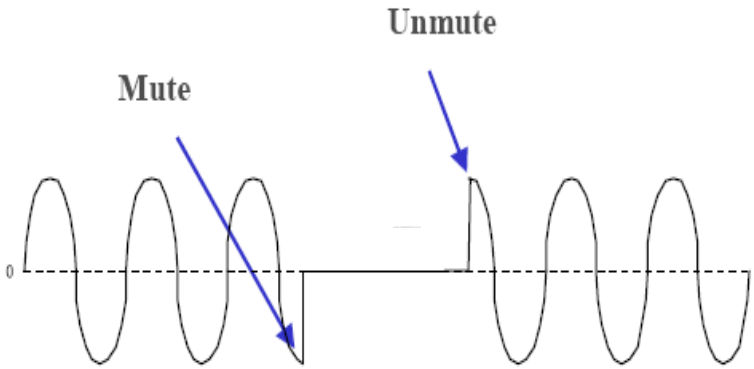


Figure 15. Zero Cross Enabled when Output Muted

8. Register Descriptions

8.1. Reg-00h: Software Reset

Default: 0003'h

Table 9. MX00 Software Reset

Name	Bits	RW	Default	Description
id	15:8	R	00'h	Chip ID
Reserved	7:0	R	03'h	Reserved

8.2. Reg-02h: Speaker Output Volume

Default: 9F9F'h

Table 10. MX02 Speaker Output Volume

Name	Bits	RW	Default	Description
mute_sp_l	15	RW	1'h	Mute Speaker Output Positive/Negative 0: On 1: Mute (-∞ dB)
Reserved	14:13	R	0'h	Reserved
sel_sp_l_vol	12:8	RW	1F'h	SPK Left Output Volume (SPKL[4:0]) in 1.5dB Steps
mute_sp_r	7	RW	1'h	Mute SPK Right Channel Reg1C[15:14] = 01'b, Mute by Reg02[15] 0: On 1: Mute (-∞ dB)
Reserved	6:5	R	0'h	Reserved
sel_sp_r_vol	4:0	RW	1F'h	SPK Right Output Volume (SPKR[4:0]) in 1.5dB Steps *Note: For SPKR/SPKL: 00h: 0dB attenuation.* *1Fh: 46.5dB attenuation.*

8.3. Reg-04h: Headphone Output Volume

Default: 9F9F'h

Table 11. MX04 Headphone Output Volume

Name	Bits	RW	Default	Description
mute_hp_l	15	RW	1'h	Mute Left Headphone Amp Control 0: On 1: Mute Left Channel (-∞ dB)
Reserved	14:13	R	0'h	Reserved
sel_hp_l_vol	12:8	RW	1F'h	Headphone Output Left Volume (HPL[4:0]) in 1.5dB Steps
mute_hp_r	7	RW	1'h	Mute Right Headphone Amp Control 0: On 1: Mute Left Channel (-∞ dB)
Reserved	6:5	R	0'h	Reserved
sel_hp_r_vol	4:0	RW	1F'h	Headphone Output Right Volume (HPR[4:0]) in 1.5dB Steps *Note: For HPR/HPL: 00h: 0dB attenuation.* *1Fh: 46.5dB attenuation.*

8.4. Reg-0Ah: LINE Input Volume

Default: C8C8'h

Table 12. MX0A LINE Input Volume

Name	Bits	RW	Default	Description
mute_lil2hp	15	RW	1'h	Mute Left Volume Output to Headphone Left Mixer Control 0: On 1: Mute
mute_lil2spk	14	RW	1'h	Mute Left Volume Output to Speaker Mixer Control 0: On 1: Mute
Reserved	13	R	0'h	Reserved
sel_li_l_vol	12:8	RW	08'h	Line-In Left Volume (NLV[4:0]) in 1.5dB Step
mute_lir2hp	7	RW	1'h	Mute Right Volume Output to Headphone Right Mixer Control* 0: On 1: Mute
mute_lir2spk	6	RW	1'h	Mute Right Volume Output to Speaker Mixer Control* 0: On 1: Mute
en_li_diff	5	RW	0'h	Line-In Differential Input Control 0: Disable 1: Enable. Only output to HP left mixer
sel_li_r_vol	4:0	RW	08'h	Line-In Right Volume (NRV[4:0]) in 1.5dB Steps* *Note: For NRV/NLV: 00h: +12 dB gain* *08h: 0 dB attenuation* *1Fh: 34.5 dB attenuation*

Note: '' indicates no function when Reg-0A[5] = 1'b.*

8.5. Reg-0Ch: Stereo DAC Digital Volume

Default: FFFF'h

Table 13. MX0C Stereo DAC Digital Volume

Name	Bits	RW	Default	Description
mute_dacl2hp	15	RW	1'h	Mute DAC Left Channel Digital Volume Output to Headphone Mixer Control 0: On 1: Mute (-∞ dB)
mute_dacl2spk	14	RW	1'h	Mute DAC Left Channel Digital Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞ dB)
dac_l_vol	13:8	RW	3F'h	DAC Left Channel Digital Volume (PLV[5:0]) in 0.75dB Steps
mute_dacr2hp	7	RW	1'h	Mute Right Channel DAC Digital Volume Output to Headphone Mixer Control 0: On 1: Mute (-∞ dB)
mute_dacr2spk	6	RW	1'h	Mute Right Channel DAC Digital Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞ dB)
dac_r_vol	5:0	RW	3F'h	DAC Right Channel Digital Volume (PRV[5:0]) in 0.75dB Steps *Note: For PRV/PLV: 00h: +12dB gain* *10h: 0dB attenuation* *3Fh: 35.25dB attenuation*

8.6. Reg-16h: Soft Delay Volume Control Time

Default: 0009'h

Table 14. MX16 Soft Delay Volume Control Time

Name	Bits	RW	Default	Description
Reserved	15:4	R	0'h	Reserved
sel_sync_softvol	3:0	RW	1001'b	Soft Volume Change Delay Time (Default=1001b) 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved

Note: SVSYNC=1/Fs, Step: -1.5dBFS.

8.7. Reg-1Ch: Output Mixer Control

Default: 8004'h

Table 15. MX1C Output Mixer Control

Name	Bits	RW	Default	Description
spkon_source_clsd	15:14	RW	2'h	
Reserved	13:12	R	0'h	Reserved
sel_spk_vol_in	11:10	RW	00'h	SPK Volume Output Source Select 00: VMID (No input) 01: HP Mixer 10: Speaker mixer (diff out) 11: Reserved
sel_hp_l_in	9	RW	0'h	HPL Volume Output Source Select 0: VMID (No input) 1: HP Left Mixer
sel_hp_r_in	8	RW	0'h	HPR Volume Output Source Select 0: VMID (No input) 1: HP Right Mixer
Reserved	7:3	R	0'b	Reserved
en_spk_vol_diff	2	RW	1'h	SPK Volume Differential Negative Signal Output Enable 0: Disable negative signal 1: Enable negative signal
en_dac_hp	1	RW	0'b	DAC Direct Output to HP Amplifier Control 0: Normal 1: Enable direct output
Reserved	0	R	0'b	Reserved

Reg1C [15:14]	Any Mixer to SPKOUT			
	SPK_OUT		SPK_OUT_N	
	Config	Control Register	Config	Control Register
00'b	VOL_LP	Reg02[15:8]	VOL_RN	Reg02[7:0]
01'b	VOL_LP	Reg02[15:8]	VOL_RP	Reg02[7:0]
10'b	VOL_LP	Reg02[15:8]	VOL_LN	Reg02[15:8]
11'b	MUTE	MUTE	MUTE	MUTE

8.8. Reg-34h: Stereo Audio Serial Data Port Control

Default: 8000'h

Table 16. MX34 Stereo Audio Serial Data Port Control

Name	Bits	RW	Default	Description
sel_i2s_mode	15	RW	1'h	Main Serial Data Port Mode Selection 0: Master 1: Slave
Reserved	14:8	R	0'h	Reserved
ctrl_i2s_bclk_polarity	7	RW	0'h	Stereo I²S BCLK Polarity Control 0: Normal 1: Invert
Reserved	6:5	R	0'h	Reserved
en_dac_lrck_swap	4	RW	0'h	DAC Data L/R Swap 0: DAC data appears at left phase of LRCK 1: DAC data appears at right phase of LRCK *Note: Supports I²S & PCM.*
sel_i2s_data_len	3:2	RW	0'h	Data Length Selection 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
sel_i2s_data_format	1:0	RW	0'h	Stereo PCM Data Format Selection 00: I²S format 01: Left justified 10: PCM Mode A (LRCK One Plus at Master Mode) 11: PCM Mode B (LRCK One Plus at Master Mode)

8.9. Reg-38h: Stereo DAC Clock Control

Default: 2000'h

Table 17. MX38 Stereo DAC Clock Control

Name	Bits	RW	Default	Description
sel_i2s_pre_div	15:13	RW	1'h	I²S Pre-Divider 000b: ÷1 001b: ÷2 010b: ÷4 011b: ÷8 100b: ÷16 101b: ÷32 Others: Reserved
sel_i2s_bclk_ms	12	RW	0'b	Master Mode Clock Relative to BCLK and LRCK 0b: 32bits (64FS) 1b: 16bits (32FS)
Reserved	11:3	R	0'h	Reserved
sel_dac_filter_clk	2	RW	0'b	Stereo DAC Filter Clock Select 0b: 256Fs 1b: 384Fs
Reserved	1:0	R	0'h	Reserved

8.10. Reg-3Ah: Power Management Addition 1

Default: 0000'h

Table 18. MX3A Power Management Addition 1

Name	Bits	RW	Default	Description
en_main_i2s	15	RW	0'h	I^2S Digital Interface Enable 0: Disable 1: Enable
pow_zcd	14	RW	0'h	All Zero Cross Detect Power Down (Includes Digital) 0: Disable 1: Enable
Reserved	13:9	R	0'h	Reserved
pow_softgen	8	RW	0'h	Power on Softgen 1: Power on 0: Power down *Note: When pow_softgen=1, whether the HP can be driven depends on the level on Cdepop (depneds in depop mode selection)*
Reserved	7:6	R	0'h	Reserved
en_hp_out_amp	5	RW	0'h	1: Enable HP Output buffer for normal loading (used to drive High Impedance) 0: Disable (DPOP mode)
en_hp_enhance_amp	4	RW	0'h	1: Enable HP Enhance Output buffer 0: Disable (DPOP mode or normal loading mode)
Reserved	3:0	R	0'h	Reserved

The following table describes Bit 4 & Bit 5:

Table 19. Headphone Drive Ability Selection

en_hp_out_amp	en_hp_enhance_amp	Description
0'b	0'b	HP Output Off
0'b	1'b	Not Used
1'b	0'b	HP Output for High-Impedance Loading (>KOhm)
1'b	1'b	HP Output for Low-Impedance Loading (<100Ohm)

8.11. Reg-3Ch: Power Management Addition 2

Default: 0000'h

Table 20. MX3C Power Management Addition 2

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
pow_clsd	14	RW	0'b	0: Disable 1: Enable All Class-D Power
pow_vref	13	RW	0'h	0: Disable 1: Enable VREF for All analog circuit (control to Vref pin)
pow_pll	12	RW	0'h	0: Disable 1: Enable PLL
Reserved	11	RW	0'h	Reserved (Must be Set to 0)
pow_dac_ref	10	RW	0'h	0: Disable 1: Enable DAC reference circuit (Vref+/Vref-)
pow_dac_l	9	RW	0'h	0: Disable 1: Enable left STEREO DAC and its filter clock
pow_dac_r	8	RW	0'h	0: Disable 1: Enable right STEREO DAC and its filter clock
pow_dacl2mixer_direct	7	RW	0'h	0: Disable 1: Enable left DAC to mixer and direct path power
pow_dacr2mixer_direct	6	RW	0'h	0: Disable 1: Enable Right DAC to mixer and direct path power
pow_mix_hp_l	5	RW	0'h	0: Disable 1: Enable left headphone mixer
pow_mix_hp_r	4	RW	0'h	0: Disable 1: Enable right headphone mixer
pow_mix_spk	3	RW	0'h	0: Disable 1: Enable Speaker mixer
Reserved	2:0	R	0'h	Reserved

8.12. Reg-3Eh: Power Management Addition 3

Default: 0000'h

Table 21. MX3E Power Management Addition 3

Name	Bits	RW	Default	Description
pow_main_bias	15	RW	0'h	0: Disable 1: Enable Main bias of analog circuit
Reserved	14:13	R	0'h	Reserved
pow_spk_vol	12	RW	0'h	0: Disable 1: Enable SPK_OUT output *Note: Power speaker volume controls the Class-D speaker output.*
Reserved	11	R	0'h	Reserved
pow_hp_l_vol	10	RW	0'h	0: Disable 1: Enable HP_OUT_L Volume control & HP_L Amplifier
pow_hp_r_vol	9	RW	0'h	0: Disable 1: Enable HP_OUT_R Volume control & HP_R Amplifier
Reserved	8	R	0'h	Reserved
pow_li_l_vol	7	RW	0'h	0: Disable 1: Enable LINE_IN Left Volume control
pow_li_r_vol	6	RW	0'h	0: Disable 1: Enable LINE_IN Right Volume control
Reserved	5:0	R	0'h	Reserved (Must be set to '0')

8.13. Reg-40h: General Purpose Control

Default: 0100'h

Table 22. MX40 General Purpose Control

Name	Bits	RW	Default	Description
Reserved	15:12	R	0'h	Reserved
spk_ampd_ratio_clsd	11:9	RW	0'h	Speaker Class-D Amplifier V_{MID} Ratio Control (Output Gain Control) 000: 2.25Vdd 001: 2.00Vdd 010: 1.75Vdd 011: 1.5Vdd 100: 1.25Vdd 101: 1Vdd Others: Not allowed
en_dac_hpf	8	RW	1'h	STEREO DAC High Pass Filter 0: Disable 1: Enable
Reserved	7:0	R	0'h	Reserved

8.14. Reg-42h: Global Clock Control

Default: 0000'h

Table 23. MX42 Global Clock Control

Name	Bits	RW	Default	Description
sel_sysclk	15	RW	0'h	Clock Source MUX Control 0: XTI 1: PLL
sel_pll_sour	14	RW	0'h	PLL Source Select 0: From XTI 1: From BIT_CLK
Reserved	13:3	R	0'h	Reserved
sel_pll_pre_div	0	RW	0'b	PLL Pre Divider 0b: ÷1 1b: ÷2

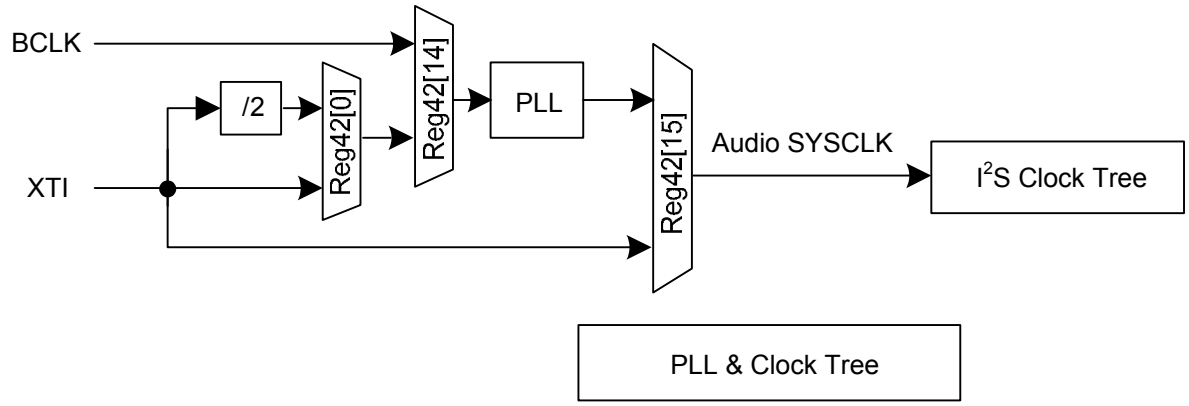


Figure 16. Global Clock Control

8.15. Reg-44h: PLL M/N Code Control

Default: 0000'h

Table 24. MX44 PLL M/N Code Control

Name	Bits	RW	Default	Description
sel_pll_n_code	15:8	RW	00'h	N[7:0] Code for Analog PLL 00000000: Div 2 00000001: Div 3 …… 11111111: Div 257
sel_pll_m_bypass	7	RW	0'h	Bypass PLL M 0b: No bypass 1b: Bypass
sel_pll_k_code	6:4	RW	0'h	K[2:0] Code for Analog PLL 000: Div 2 001: Div 3 …… 111: Div 9
sel_pll_m_code	3:0	RW	0'h	M[3:0] Code for Analog PLL 0000: Div 2 0001: Div 3 …… 1111: Div 17

8.16. Reg-5Ah: Jack Detect Control

Default: 0000’h

Table 25. MX5A Jack Detect Control

Name	Bits	RW	Default	Description
SEL_JD_SOURCE	15:14	RW	0’h	Jack Detect Select 00: OFF 01: Reserved 10: JD1 and enable Line in Left Ch. pin share 11: JD2 and enable Line in Right Ch. pin share
en_jd_vref	13	RW	0’b	Enable Jack Detect Trigger Vref 0: Disable 1: Enable
polarity_jd_tri_vref	12	RW	0’b	Selected Jack Detect Polarity Trigger Vref 0: Low trigger 1: High trigger
en_jd_hpout	11	RW	0’h	Enable Jack Detect Trigger HPOUT 0: Disable 1: Enable
polarity_jd_tri_hpout	10	RW	0’h	Select Jack Detect Polarity Trigger HPOUT 0: Low trigger 1: High trigger
en_jd_spkout	9	RW	0’h	Enable Jack Detect Trigger SPKOUT 0: Disable 1: Enable
polarity_jd_tri_spkout	8	RW	0’h	Select Jack Detect Polarity Trigger SPKOUT 0: Low trigger 1: High trigger
Reserved	7:4	R	0’b	Reserved
polarity_jd_out	3	RW	0’h	Jack Detect Polarity 0: Normal 1: Output Invert
status_jd_internal	2	R	0’h	Jack Detect Status Read: Return status of Jack Detect Select output
Reserved	1:0	R	0’b	Reserved

8.17. Reg-5Ch: MISC1 Control

Default: 0000’h

Table 26. MX5C MISC1 Control

Name	Bits	RW	Default	Description
en_sp_l_dezero	15	RW	0’h	SPK Volume Zero Cross Detector Control (SPK Left Volume Zero Cross Detector when Reg1C[15:14] = 01’b) 0: Disable 1: Enable
en_sp_l_softvol	14	RW	0’h	SPK Soft Volume Change Enable (SPK Left Soft Volume Change Enable when Reg1C[15:14] = 01’b) 0: Disable 1: Enable
en_sp_r_dezero	13	RW	0’h	SPK Right Zero Cross Detector 0: Disable 1: Enable

Name	Bits	RW	Default	Description
en_sp_r_softvol	12	RW	0'h	SPK Right Soft Volume Change Enable 0: Disable 1: Enable
en_hp_l_dezero	11	RW	0'h	HP Out Left Zero Cross Detector Control 0: Disable 1: Enable
en_hp_l_softvol	10	RW	0'h	HP Out Left Soft Volume Change Control 0: Disable 1: Enable
en_hp_r_dezero	9	RW	0'h	HP Out Right Zero Cross Detector Control 0: Disable 1: Enable
en_hp_r_softvol	8	RW	0'h	HP Out Right Soft Volume Control 0: Disable 1: Enable
Reserved	7:4	R	0'h	Reserved
en_dac_zc	3	RW	0'b	Enable DAC Digital Volume Zero Crossing Detect 0: Disable 1: Enable
en_dac_soft_vol	2	RW	0'b	Enable DAC Digital Soft Volume 0: Disable 1: Enable
Reserved	1:0	R	0'h	Reserved

Note: When zero cross detector is enabled, change mute volume only on zero crossing or after timeout.

8.18. Reg-5Eh: MISC2 Control

Default: 0000'h

Table 27. MX5E MISC2 Control

Name	Bits	RW	Default	Description
en_vref_fastb	15	RW	0'b	Enable Fast Vref (This Bit must be Disabled in Normal Use) 0: Enable fast Vref 1: Disable fast Vref
en_thermal_shutdown	14	RW	0'b	Thermal Shut Down Enable 0: Disable 1: Enable
Reserved	13:10	R	0'h	Reserved
en_dp2_hp	9	RW	0'h	Enable De-Pop Mode 2 of HP_Out 0: Disable 1: Enable
en_dp1_hp	8	RW	0'h	Enable De-Pop Mode 1 of HP_Out 0: Disable 1: Enable
en_smt_hp_l	7	RW	0'h	Enable HP_L Mute-Unmute Depop 0: Disable 1: Enable
en_smt_hp_r	6	RW	0'h	Enable HP_R Mute-Unmute Depop 0: Disable 1: Enable
smt_en	5	RW	0'h	Mute-Unmute Depop 0: Disable 1: Enable
Reserved	4	R	0'h	Reserved
mute_dac_l	3	RW	0'h	Mute Main DAC Left Input 0: On 1: Mute (-∞ dB)
mute_dac_r	2	RW	0'h	Mute Main DAC Right Input 0: On 1: Mute (-∞ dB)
Reserved	1:0	R	0'h	Reserved

8.19. Reg-68h: Automatic Volume Control (AVC) Control

Default: 100B'h

Table 28. MX68 Automatic Volume Control (AVC) Control

Name	Bits	RW	Default	Description
EN_AVC	15	RW	0'b	AVC Enable (Default: 00b) 0: Disable AVC 1: Enable AVC to control Digital gain
sel_avc_ref_ch	14	RW	0'b	AVC Reference Channel Selection 0: Left Channel 1: Right Channel
sel_nonact_action	13	RW	0'b	Gain Action of Non-active Region 0: Keep previous Gain 1: Unit Gain
Reserved	12:5	R	80'h	Reserved
sel_monitor_window	4:0	RW	0B'h	Monitor Window Control (Unit: 2^(n+1) Samples) (Default: 01011b) 00000b: 2^(1) samples 00001b: 2^(2) samples 00010b: 2^(3) samples …… 10000b: 2^(17) samples Others: Reserved (Maximum=1000000000000000=2^17)

8.20. Reg-6Ah: Private Register Index

Default: 0000'h

Table 29. MX6A Private Register Index

Name	Bits	RW	Default	Description
Reserved	15:7	R	0'h	Reserved
private_reg_index	6:0	RW	0'h	Private Register Index

8.21. Reg-6Ch: Private Register Data

Default: 0000'h

Table 30. MX6C Private Register Data

Name	Bits	RW	Default	Description
private_reg_data	15:0	RW	0'h	Private Register Data Port

8.22. Private-21h: Auto Volume Control Register 1

Default: 0400'h

Table 31. PR21 Auto Volume Control Register 1

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
sel_avc_thmax	14:0	RW	0400'h	The Maximum PCM Absolute Level After AVC, Thmax (=0 ~ 2^15-1)

8.23. Private-22h: Auto Volume Control Register 2

Default: 0390'h

Table 32. PR22 Auto Volume Control Register 2

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
sel_avc_thmin	14:0	RW	0390'h	The Minimum PCM Absolute Level After AVC, Thmin (=0 ~ 2^15-1)

8.24. Private-23h: Auto Volume Control Register 3

Default: 0040'h

Table 33. PR23 Auto Volume Control Register 3

Name	Bits	RW	Default	Description
Reserved	15	R	0'h	Reserved
sel_avc_thnonact	14:0	RW	0040'h	The Non-Active PCM Absolute Level AVC Will Keep Analog Unit Gain, Thnonact (=0 ~ 2^15-1)

8.25. Private-24h: Auto Volume Control Register 4

Default: 03FF'h

Table 34. PR24 Auto Volume Control Register 4

Name	Bits	RW	Default	Description
sel_avc_cntminth	15:0	RW	03FF'h	CNTMAXTH1 Controls the Sensitivity to Increased Gain (unit:2^1) This value should be less than CNTMAXTH2 (Max=1111111111111110=2^17-2)

8.26. Private-25h: Auto Volume Control Register 5

Default: 0400'h

Table 35. PR25 Auto Volume Control Register 5

Name	Bits	RW	Default	Description
sel_avc_cntmaxth	15:0	RW	0400'h	CNTMAXTH2 Controls the Sensitivity to Decreased Gain (Unit: 2^1) This value should be less than Monitor Window (Optimal: 1/2 Monitor Window) (Max=1111111111111110=2^17-2)

8.27. Private-39h: Digital Internal Register

Default: 8800'h

Table 36. PR39 Digital Internal Register

Name	Bits	RW	Default	Description
sel_pad_drive	15	RW	1'h	Pad Drive Capability 0b: 5mA 1b: (5+6) 11mA
Reserved	14:12	R	0'b	Reserved
osc_curr	11:9	RW	100'b	Oscillator Drive Current Control 000: 1x bias current 001: 2x 010: 4x 011: 8x 100: 16x …….. 111: 128x *Note: The oscillator startup current is set to maximum, and controlled by osc_curr after 512 clocks. The digital clock input is enabled after 1024 clocks.*
Reserved	8:0	R	0'b	Reserved

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 37. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital Power for Core	DCVDD	-0.3	-	3.63	V
Digital Power for IO and PLL	DBVDD	-0.3	-	3.63	V
Analog and HP Amplifier Power	AVDD	-0.3	-	3.63	V
Speaker Amplifier Power	SPKVDD	-0.3	-	7	V
Ambient Operating Temperature	Ta	-20	-	+85	°C
Storage Temperature	Ts	-40	-	+125	°C

9.1.2. Recommended Operating Conditions

Table 38. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.8	3.3	3.6	V
Digital Core	DCVDD	1.8	3.3	3.6	V
Analog	AVDD	2.3	3.3	3.6	V
Speaker	SPKVDD*	2.3	3.3	5	V

Note: A 10μF Capacitor must be connected from SPKVDD to SPKGND, and should be placed as close as possible to the SPKVDD pin of the ALC5628.

9.1.3. Static Characteristics

DBVDD= 3.3V, $T_{ambient}$=25°C, with 25pF external load.

Table 39. Threshold Voltage

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Voltage Range	V_{in}	-0.30	-	DBVDD +0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.33*DBVDD	V
High Level Input Voltage	V_{IH}	0.66*DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9*DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1*DBVDD	V
Low Level Input Voltage (JD2)	V_{IL}	-	-	0.33*AVDD	V
High Level Input Voltage(JD2)	V_{IH}	0.66*AVDD	-	-	V

9.2. Analog Performance Characteristics

Standard Test Conditions

- $T_{ambient}$=25°C, DBVDD=DCVDD=1.8V, AVDD=3.3V, SPKVDD=5V, 1kHz input sine wave; Sampling frequency=48kHz; 0dB=1Vrms, 10KΩ/50pF load; Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation

Table 40. Analog Performance Characteristics

Parameter	Minimum	Typical	Maximum	Units
Full Scale Input Voltage				
LINE_IN Inputs (Gain=0dB)	-	1.0	-	Vrms
Full Scale Output Voltage				
DAC Outputs	-	1.0	-	Vrms
HP_OUT Outputs	-	1.0	-	Vrms
SPK_OUT Outputs	-	1.5	-	Vrms
S/N (A Weighted)				
DAC	-	100	-	dBFS
Headphone Amplifier Output (RL=32Ω, PO=20mW)	-	95	-	dBFS
THD+N				
DAC	-	-86	-	dBFS
Headphone Amplifier Output (RL=32Ω, PO=20mW)	-	-80	-	dBFS
Power Supply Rejection (217Hz)	-	-50	-	dB
Amplifier Gain Step	-	1.5	-	dB
Crosstalk Between Input Channels	-	-80	-	dB
HP Amplifier Quiescent Current (RL=32Ω @ 3.3V)	-	600	-	µA
HP Amplifier Output Power (RL=16Ω)	25	45	-	mW
SPK Class-D Amplifier Quiescent Current (RL=8Ω @ 5V)	-	4	-	mA
SPK Class-D Amplifier Output Power (RL=4Ω @ 5V, 0.1% THD+N)	-	1.6	-	W
SPK Class-D Amplifier Output Power (RL=8Ω @ 5V, 0.1% THD+N)	-	1	-	W
SPK Class-D Amplifier Output Power (RL=4Ω @ 5V, 1% THD+N)	-	1.7	-	W
SPK Class-D Amplifier Output Power (RL=8Ω @ 5V, 1% THD+N)	-	1.1	-	W
SPK Class-D Amplifier Output Power (RL=4Ω @ 5V, 10% THD+N)	-	2.4	-	W
SPK Class-D Amplifier Output Power (RL=8Ω @ 5V, 10% THD+N)	-	1.5	-	W
Digital Power Supply Current (Power Down Mode)				
DCVDD=1.8V, DBVDD=1.8V (Include POR Circuit)	-	-	10	µA
Analog Power Supply Current (DAC to Headphone Without Load)				
AVDD=DCVDD=DBVDD=SPKVDD=3.3V	-	8	-	mA
Analog Power Supply Current (Power Down Mode)				
AVDD=3.3V	-	-	1	µA
VREF Output Voltage	-	0.5	-	AVDD
VREF Rising Time at Fast Mode (C=4.7µF)	-	-	50	ms

9.3. AC Timing Characteristics

9.3.1. I²C Control Interface

Table 41. I²C Control Interface Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Clock Pulse Duration	$t_{w(9)}$	1.3	-	-	µs
Clock Pulse Duration	$t_{w(10)}$	600	-	-	ns
Clock Frequency	f	0	-	400K*	Hz
Re-Start Setup Time	$t_{su(6)}$	600	-	-	ns
Start Hold Time	$t_{h(5)}$	600	-	-	ns
Data Setup Time	$t_{su(7)}$	100	-	-	ns
Data Hold Time	$t_{h(6)}$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su(8)}$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

Note: '' indicates the host must provide MCLK higher than 4MHz to the ALC5628 during I²C control interface access. If MCLK provides 128*8KHz, the I²C clock frequency can only support 100KHz.*

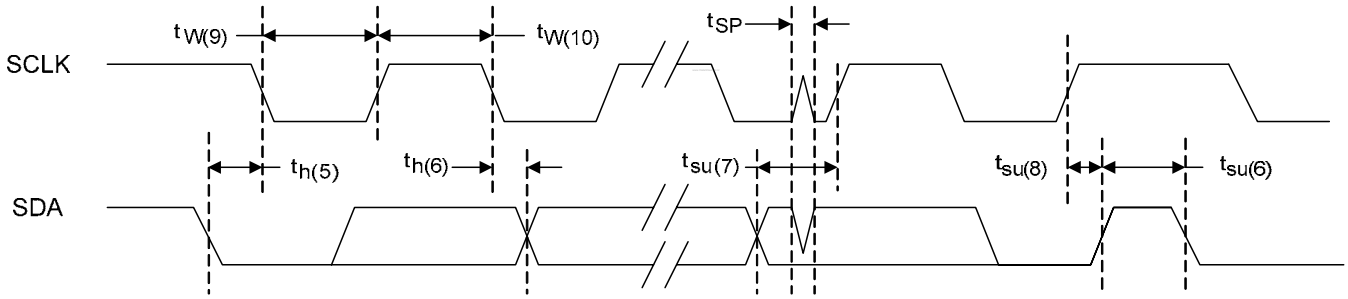


Figure 17. I²C Control Interface Waveform

9.3.2. I²S/PCM Interface Master Mode

Table 42. I²S Master Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

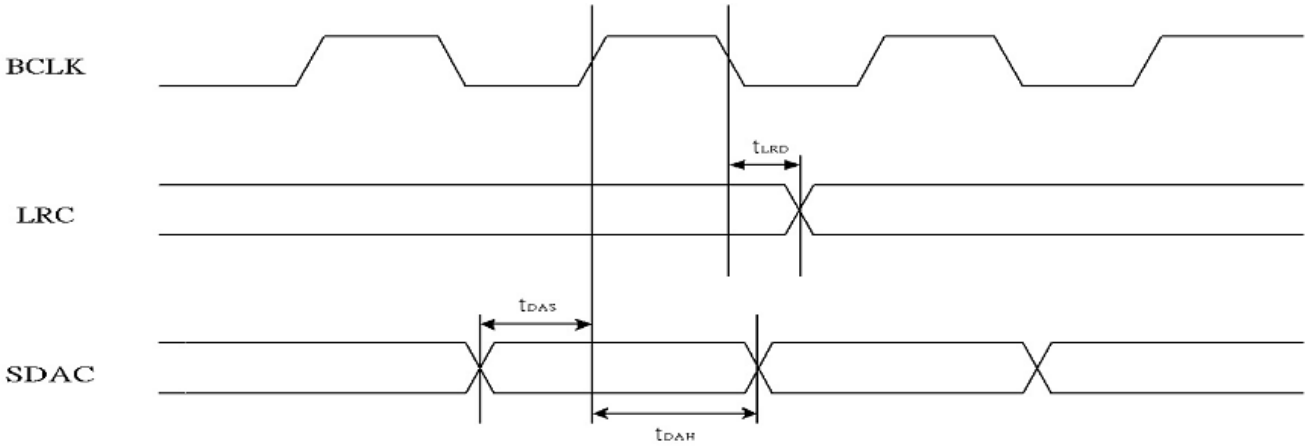


Figure 18. I²S Master Mode Waveform

9.3.3. I²S/PCM Interface Slave Mode

Table 43. I²S Slave Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

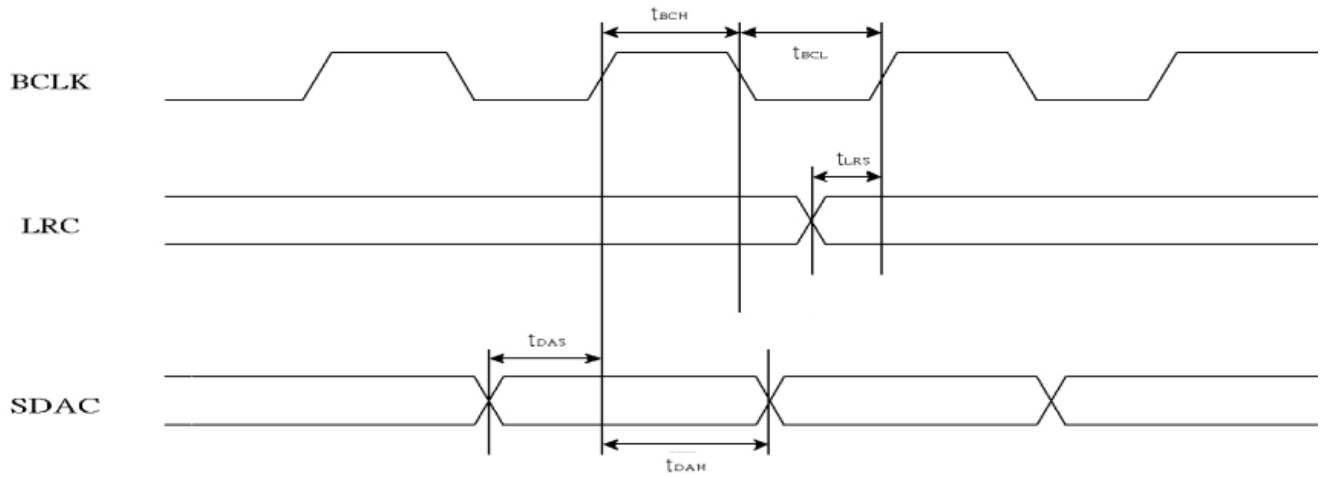


Figure 19. I²S Slave Mode Waveform

10. Application Circuits

Application circuits are for design reference only. System designers are suggested to visit Realtek's web site to download the latest application circuits. To get the best compatibility in hardware design and software driver, Realtek should confirm modifications of application circuits.

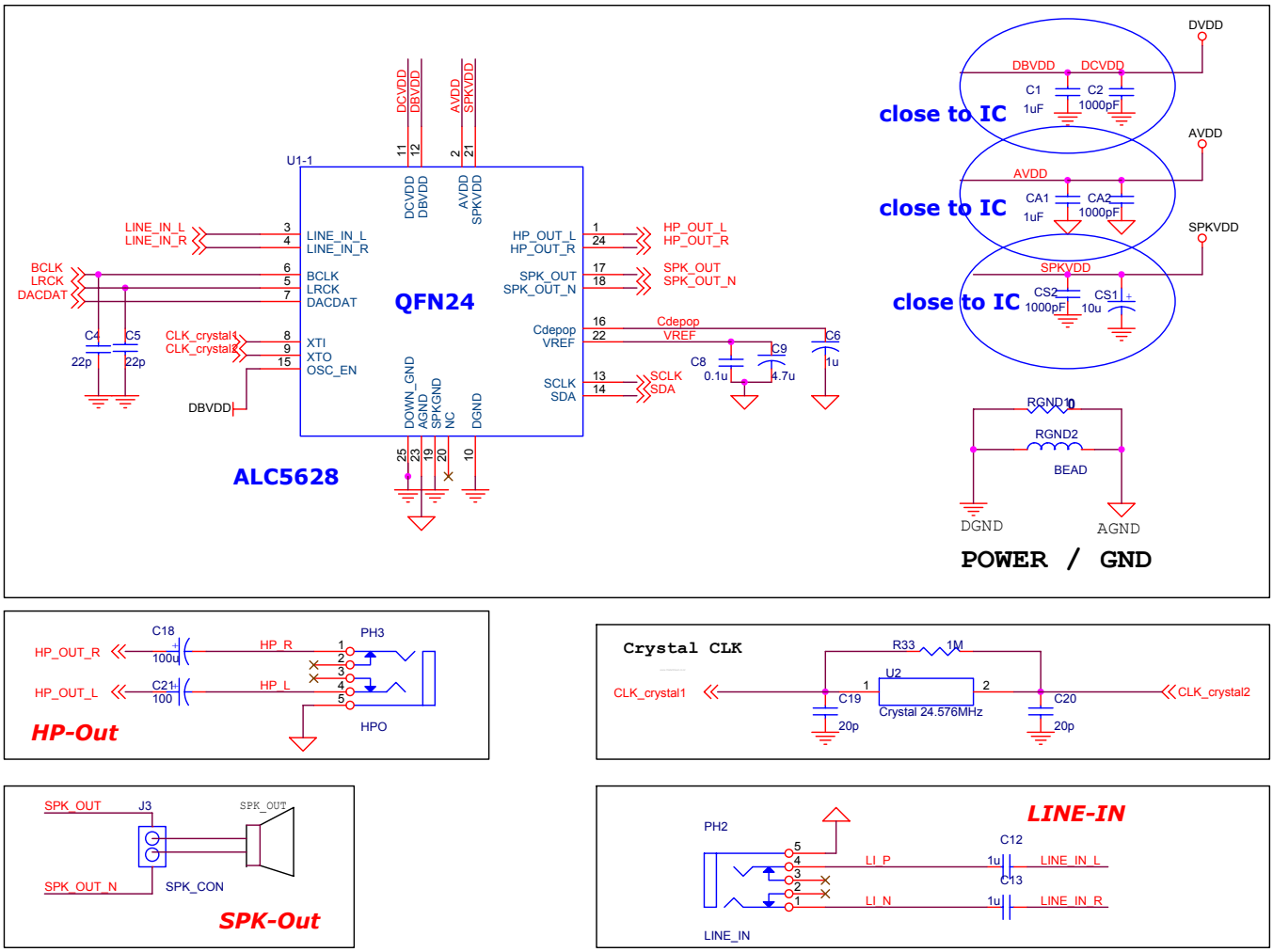
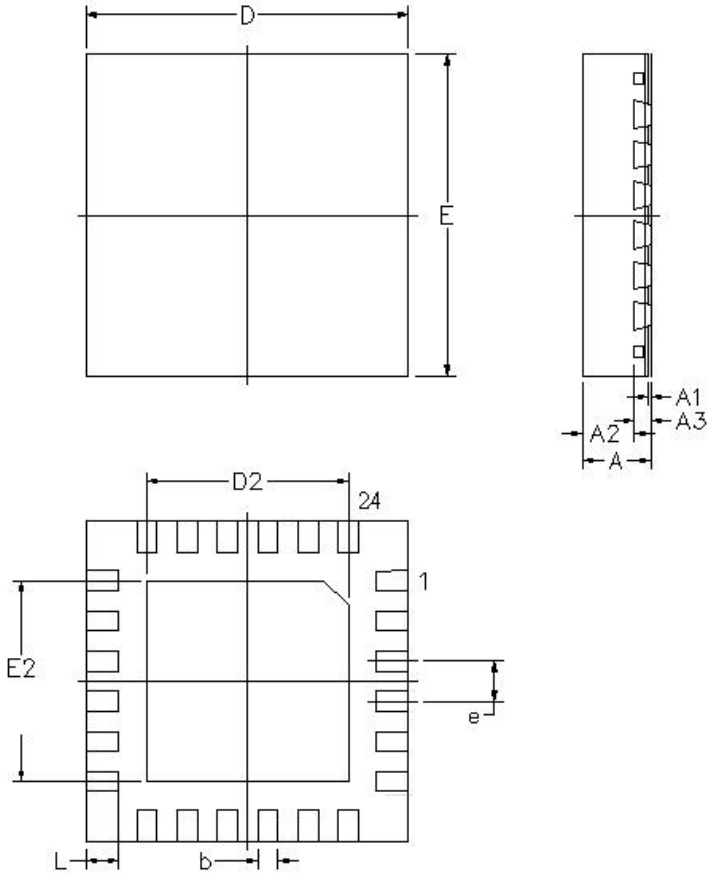


Figure 20. Application Circuits

11. Mechanical Dimensions

QFN-24 Package; 4x4mm Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	-	0.65	0.70	-	0.026	0.028
A_3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	4.00 BSC			0.158 BSC		
D_2/E_2	2.00	2.25	2.50	0.078	0.088	0.098
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Ordering Information

Table 44. Ordering Information

Part Number	Package	Status
ALC5628-GR	QFN-24 in 'Green' Package (Tray)	Mass Production
ALC5628-GRT	QFN-24 in 'Green' Package (Tape & Reel)	Mass Production

Note: See page 6 for package and version identification.

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