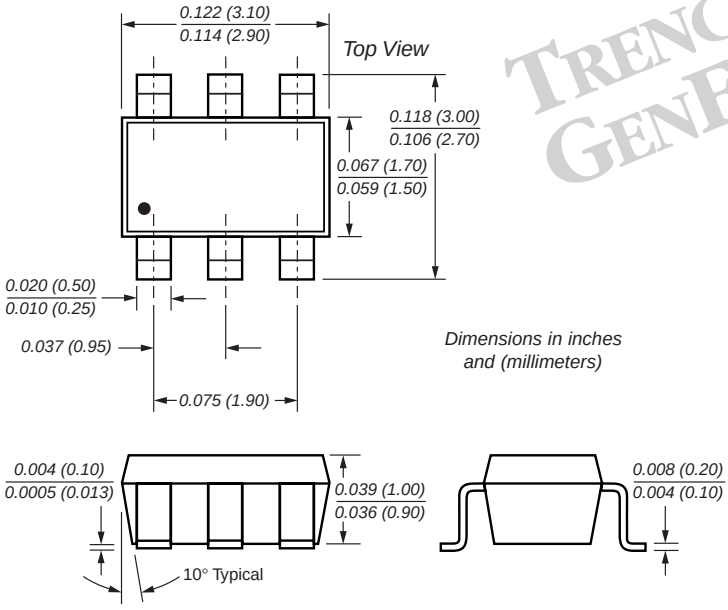
P-Channel Enhancement-Mode MOSFET

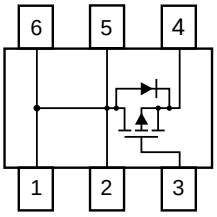
V_{DS} –30V
$R_{DS(ON)}$ 75mΩ
I_D –3.6A

SOT-23-6L

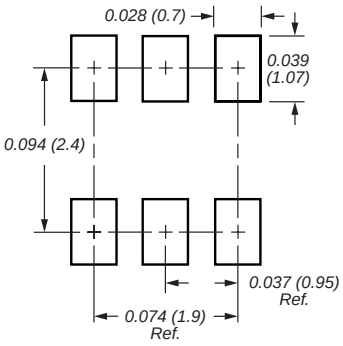


TRENCH GENFET®

Pin Configuration (Top View)



Mounting Pad Layout



Mechanical Data

Case: SOT-23-6L package

Terminals: Leads solderable per MIL-STD-750, Method 2026

Marking Code: 54

Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Popular SOT-23-6L package with copper lead-frame for superior thermal and electrical capabilities
- Compact and low profile

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[2] T_J = 150°C	T_A = 25°C T_A = 70°C	I_D	–3.6 –2.9	A
Pulsed Drain Current[1]		I_{DM}	–10	
Power Dissipation[2] T_J = 150°C	T_A = 25°C T_A = 70°C	P_D	2.0 1.3	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Junction-to-Ambient Thermal Resistance[2]		$R_{\theta JA}$	62.5	°C/W

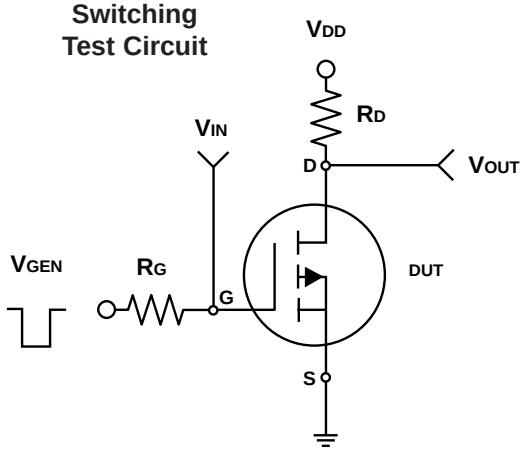
Notes: (1) Pulse width limited by maximum junction temperature
(2) Surface mounted on FR4 board, t ≤ 5 sec.

Electrical Characteristics (T_J = 25°C unless otherwise noted)

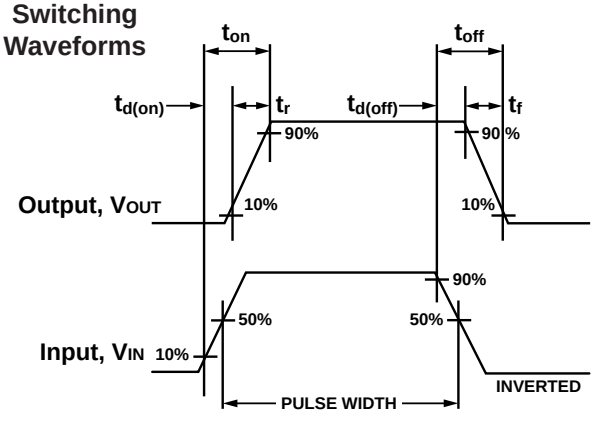
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = –250µA	–30	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250µA	–1	–	–3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –24V, V_{GS} = 0V	–	–	–1.0	µA
		V_{DS}=–20V, V_{GS}=0V, T_J=55°C	–	–	–10.0	
On-State Drain Current[1]	$I_{D(on)}$	V_{DS} = –5V, V_{GS} = –4.5V	–5	–	–	A
Drain-Source On-State Resistance[1]	$R_{DS(on)}$	V_{GS} = –10V, I_D = –3.6A	–	55	75	mΩ
		T_J = 125°C	–	75	127	
		V_{GS} = –4.5V, I_D = –2.7A	–	86	125	
Forward Transconductance[1]	g_{fs}	V_{DS} = –10V, I_D = –3.6A	–	3	–	S
Dynamic						
Total Gate Charge[1]	Q_g	V_{DS} = –15V, V_{GS} = –10V, I_D = –3.6A	–	12.5	15	nC
Gate-Source Charge[1]	Q_{gs}		–	2.0	–	
Gate-Drain Charge[1]	Q_{gd}		–	2.5	–	
Turn-On Delay Time[1]	$t_{d(on)}$	V_{DD} = –15V, I_D ≈ –1A, V_{GEN} = –10V, R_G = 6Ω	–	5	18	ns
Rise Time[1]	t_r		–	5.5	14	
Turn-Off Delay Time[1]	$t_{d(off)}$		–	40	60	
Fall Time[1]	t_f		–	19	29	
Input Capacitance	C_{iss}	V_{DS} = –15V, V_{GS} = 0V, f = 1.0MHz	–	670	–	pF
Output Capacitance	C_{oss}		–	125	–	
Reverse Transfer Capacitance	C_{rss}		–	70	–	
Source-Drain Diode						
Maximum Diode Forward Current	I_S	T_A = 25°C	–	–	–1.3	A
Maximum Pulsed Diode Forward Current[2]	I_{SM}		–	–	–10	
Diode Forward Voltage[1]	V_{SD}	I_S = –1.3A, V_{GS} = 0V	–	–0.85	–1.2	V
		T_J = 125°C	–	–0.64	–1	

Note: (1) Pulse test, pulse width ≤ 300 µs, duty cycle ≤ 2%
(2) Pulse width limited by maximum junction temperature

Switching Test Circuit



Switching Waveforms



Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

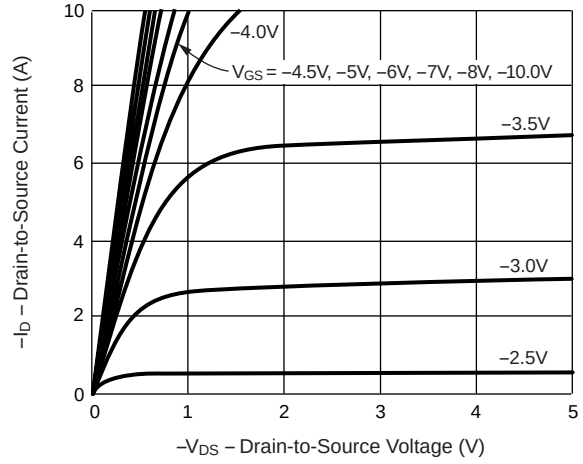


Fig. 2 – Transfer Characteristics

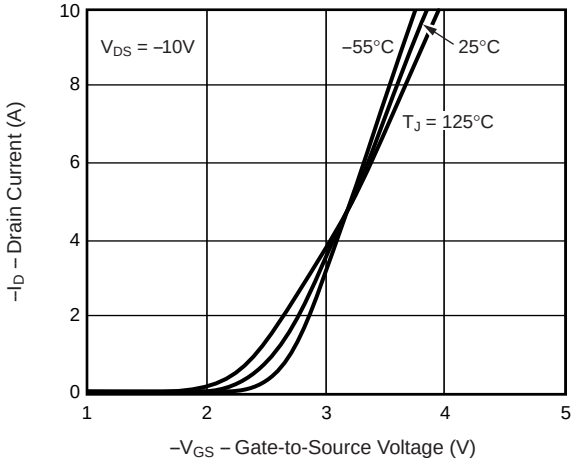


Fig. 3 – Threshold Voltage

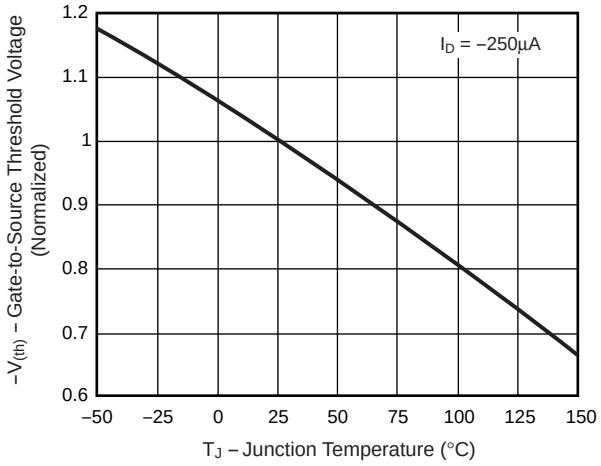


Fig. 4 – On-Resistance vs. Drain Current

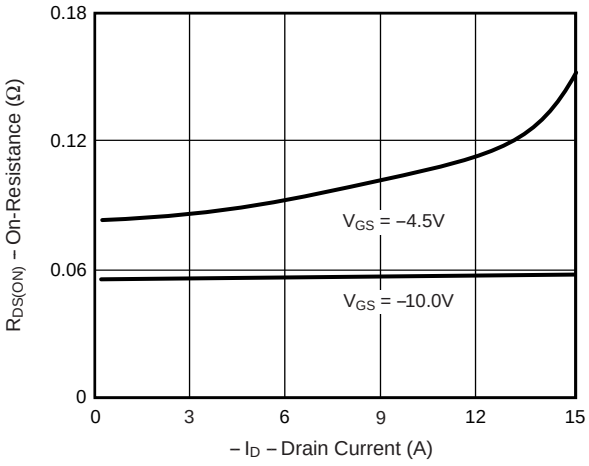


Fig. 5 – On-Resistance vs. Junction Temperature

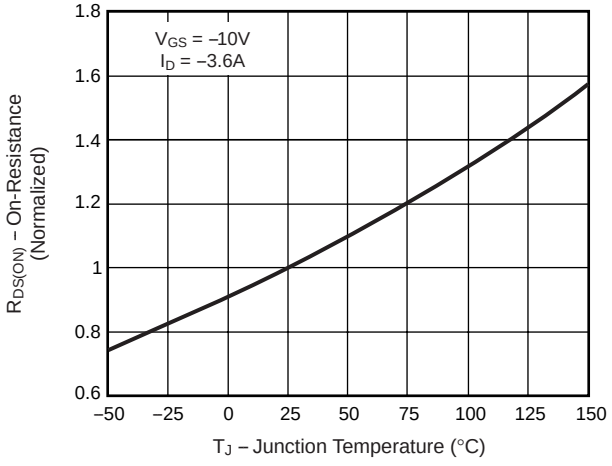
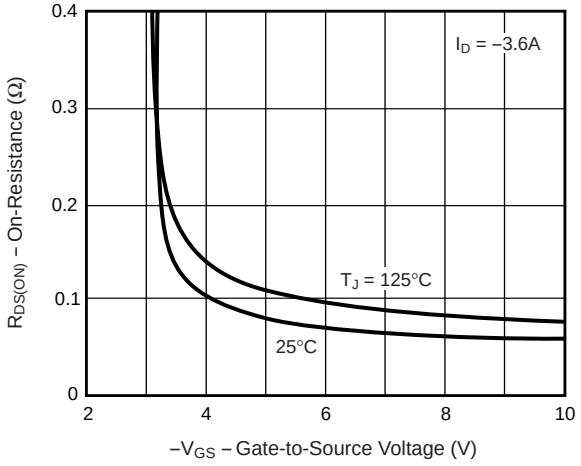


Fig. 6 – On-Resistance vs. Gate-to-Source Voltage



Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 7 – Gate Charge

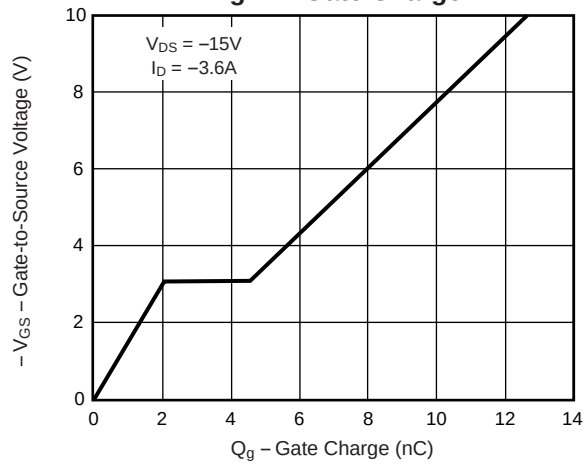


Fig. 8 – Capacitance

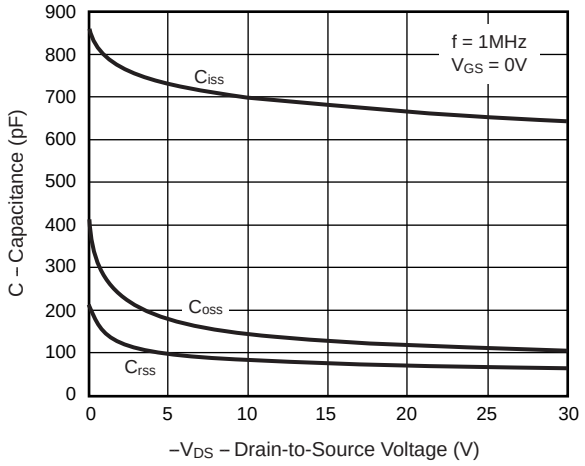


Fig. 9 – Source-Drain Diode Forward Voltage

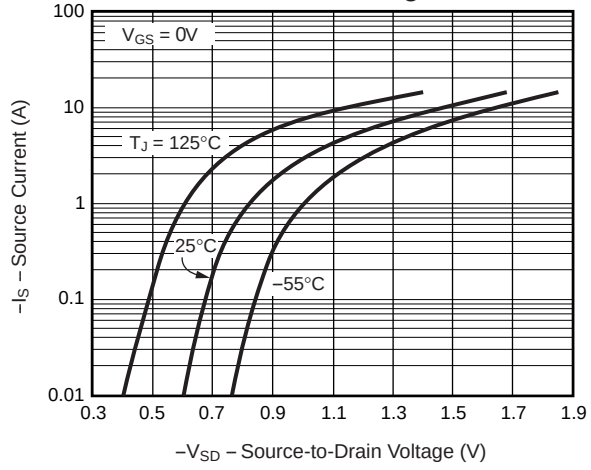


Fig. 10 – Transient Thermal Impedance

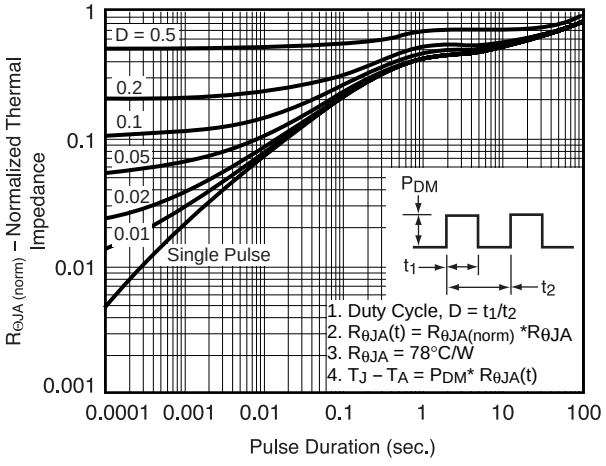


Fig. 11 – Power vs. Pulse Duration

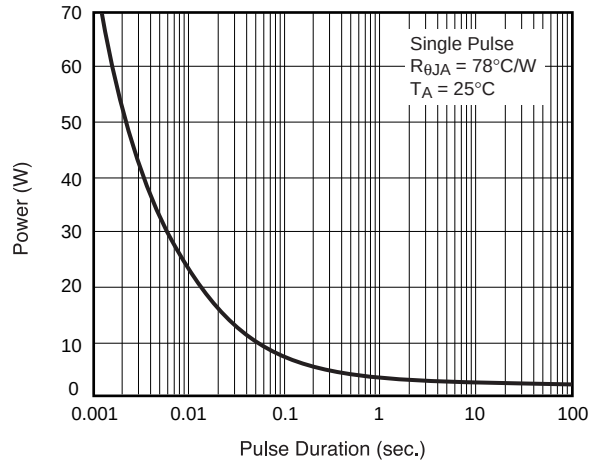


Fig. 12 – Maximum Safe Operating Area