REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change to package dimension for case outline letter Y. Change to figure 4, and parameter t_{OLQV} of table I. Editorial changes throughout.	1990 JUN 01	

REV																								
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SHEET																								
REV STATUS OF SHEETS	REV	A	A	A		A	A	A		A	A	A	A	A	A	A								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15								

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Kenneth S Rice

CHECKED BY: Wm Johnson

APPROVED BY:

DRAWING APPROVAL DATE: 8 FEBRUARY 1989

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, MEMORY, DIGITAL, CMOS
2K x 8 STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88740

SHEET 1

DESC FORM 193
SEP 87

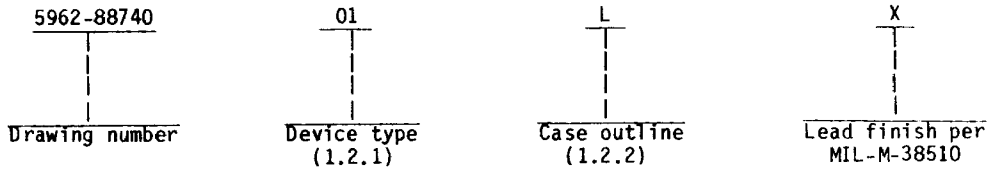
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1463

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(See 6.6)	2K X 8 low power CMOS SRAM	35 ns
02	(See 6.6)	2K X 8 low power CMOS SRAM	25 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-Lead, 1.280" x .310" x .200"), dual-in-line package
X	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package
Y	Figure 1 (24-lead, .308" x .408" x .120"), rectangular chip carrier package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to 7 V dc
Input voltage range 2/	0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range in high impedance state	-0.5 V dc to 7 V dc
Output current	20 mA
Storage temperature range	-65°C to +150°C
Power dissipation (P_D)	1 W
Lead temperature (soldering, 10 seconds)	+275°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage (V_{IH})	2.2 V dc minimum to V_{CC} + 0.5 V dc maximum
Low level input voltage (V_{IL}) 2/	-0.5 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ All voltages are with respect to GND.

2/ V_{IL} (minimum) of -3 V dc for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below -1 V dc will result in excessive currents that may damage the device.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

Bulletin

MILITARY

MIL-BUL-103 - List of Standardized Military Drwaings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Load circuit and switching waveforms. The load circuit and switching waveforms shall be as specified on figure 4.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-M-38510, inspection lot - class B paragraph) shall be subjected to and pass the internal water vapor test (method 1018 of MIL-STD-883), the frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, $V_{SS} = 0\ V$, unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current	I_{CC1}	$t_{AVAV} = t_{AVAV}$ (minimum), $V_{CC} = 5.5\ V$, $\overline{CE} = V_{IL}$, all other inputs at V_{IL}	1, 2, 3	01		105	mA
				02		115	
Standby power supply current TTL	I_{CC2}	$\overline{CE} \ge V_{IH}$, all other inputs $\le V_{IL}$ or $\ge V_{IH}$, $V_{CC} = 5.5\ V$, $f = 0$ MHz	1, 2, 3	01		30	mA
				02		40	
Standby power supply current CMOS	I_{CC3}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, $f = 0$ MHz, $V_{CC} = 5.5\ V$, all other inputs $< 0.2\ V$ or $> (V_{CC} - 0.2\ V)$	1, 2, 3	All		0.9	mA
Data retention current	I_{CC4}	$\overline{CE} \ge (V_{CC} - 0.2\ V)$, $f = 0$ MHz, $V_{CC} = 2.0\ V$, all other inputs $< 0.2\ V$ or $> (V_{CC} - 0.2\ V)$	1, 2, 3	All		300	µA
Input leakage current, any input	I_{ILK}	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ to $5.5\ V$	1, 2, 3	All	-10	10	µA
Off-state output leakage current	I_{OLK}	$V_{CC} = 5.5\ V$, $V_{IN} = 0\ V$ to $5.5\ V$	1, 2, 3	All	-10	10	µA
Output high voltage	V_{OH}	$I_{OUT} = -4.0$ mA, $V_{CC} = 4.5\ V$, $V_{IL} = 0.8\ V$, $V_{IH} = 2.2\ V$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	$I_{OUT} = 8.0$ mA, $V_{CC} = 4.5\ V$, $V_{IL} = 0.8\ V$, $V_{IH} = 2.2\ V$	1, 2, 3	All		0.4	V
Input capacitance 3/	C_{IN}	$V_{IN} = 0\ V$, $f = 1.0$ MHz, $T_A = +25°C$, See 4.3.1c	4	All		8.0	pF
Output capacitance 3/	C_{OUT}	$V_{OUT} = 0\ V$, $f = 1.0$ MHz, $T_A = +25°C$, See 4.3.1c	4	All		8.0	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Read cycle time	t_{AVAV}	4/ 5/	9,10,11	01	35		ns
				02	25		
Address access time	t_{AVQV}		9,10,11	01		35	ns
				02		25	
Output hold after address change 3/	t_{AVQX}		9,10,11	01	0		ns
				02	0		
Output enable to output active 3/	t_{OLQX}		9,10,11	01	0		ns
				02	0		
Output enable access time	t_{OLQV}		9,10,11	01		20	ns
				02		16	
Chip enable to output active 3/	t_{ELQX}		9,10,11	01	0		ns
				02	0		
Chip enable access time	t_{ELQV}		9,10,11	01		35	ns
				02		25	
Chip enable to output in high-Z 3/	t_{EHQZ}		9,10,11	01		20	ns
				02		15	
Write recovery time	t_{WHAV}		9,10,11	01	0		ns
				02	0		
Chip enable to end-of-write	t_{ELWH}		9,10,11	01	30		ns
				02	20		
Address valid to end-of-write	t_{AVWH}		9,10,11	01	30		ns
				02	20		
Address to $\overline{WE}$ setup time	t_{AVWL}		9,10,11	01	0		ns
				02	0		
Address to $\overline{CE}$ setup time	t_{AVEL}		9,10,11	01, 02	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output enable to output in high Z 3/	t_{OHQZ}	4/ 5/	9,10,11	01		20	ns
				02		16	
Write enable pulse width	t_{WLWH}		9,10,11	01	25		ns
				02	20		
Data setup to end-of-write	t_{DVWH}		9,10,11	01	20		ns
				02	15		
Data hold after end-of-write	t_{WHDX}		9,10,11	01	0		ns
				02	0		
Chip-enable pulse width during write	t_{ELEH}		9,10,11	01	30		ns
				02	20		
Write enable pulse setup time	t_{WLEH}		9,10,11	01	25		ns
				02	20		

1/ All voltages referenced to V_{SS}.

2/ Negative undershoots to a minimum of -0.3 V are allowed with a maximum of 50 ns pulse width.

3/ Tested initially, and after any design or process change which could affect these parameters, and therefore shall be guaranteed to the limits specified in table I.

4/ AC measurements assume transition time ≤ 5 ns and input levels are from V_{SS} to 3.0 V. Output load is specified on figure 4. Reference timing levels are at 1.5 V.

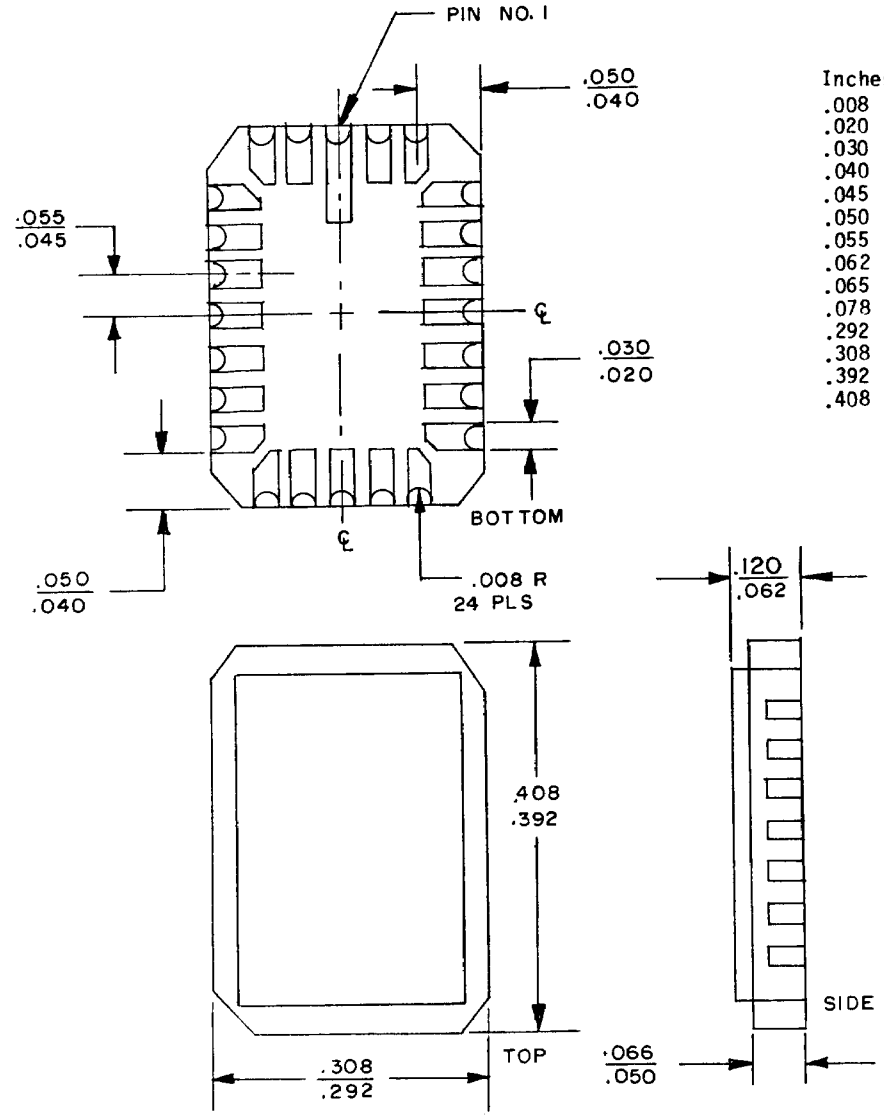
5/ For timing waveforms, see figure 4.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

24 PIN RECTANGULAR LEADLESS CHIP CARRIER



Inches	mm
.008	0.20
.020	0.50
.030	0.76
.040	1.01
.045	1.14
.050	1.27
.055	1.39
.062	1.57
.065	1.67
.078	1.98
.292	7.41
.308	7.82
.392	9.95
.408	10.36

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outline Y (24-lead, 308" x .408" x .120"), rectangular chip carrier package).

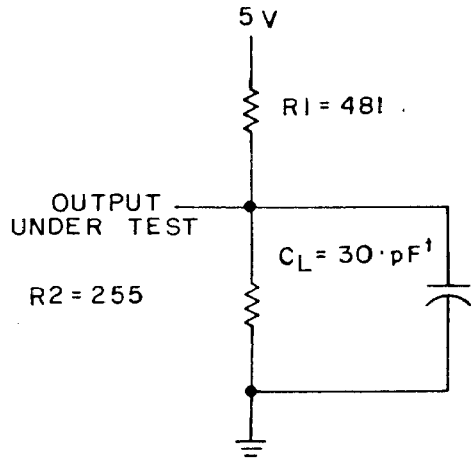
Device types	01 and 02		
Case outlines	J,K,L,Y	X	3
Terminal Number	Terminal symbol		
1	A7	A7	NC
2	A6	A6	NC
3	A5	A5	NC
4	A4	A4	A7
5	A3	A3	A6
6	A2	A2	A5
7	A1	NC	A4
8	A0	NC	A3
9	I/O 0	A1	A2
10	I/O 1	A0	A1
11	I/O 2	I/O 1	A0
12	V_{SS}	I/O 2	NC
13	I/O 3	I/O 3	I/O 0
14	I/O 4	V_{SS}	I/O 1
15	I/O 5	I/O 4	I/O 2
16	I/O 6	I/O 5	V_{SS}
17	I/O 7	I/O 6	NC
18	$\overline{CE}$	I/O 7	I/O 3
19	A10	I/O 8	I/O 4
20	$\overline{OE}$	$\overline{CE}$	I/O 5
21	$\overline{WE}$	NC	I/O 6
22	A9	NC	I/O 7
23	A8	A10	$\overline{CE}$
24	V_{CC}	$\overline{OE}$	A10
25	---	$\overline{WE}$	$\overline{OE}$
26	---	A9	$\overline{WE}$
27	---	A8	NC
28	---	V_{CC}	A9
29	---	---	A8
30	---	---	NC
31	---	---	NC
32	---	---	V_{CC}

FIGURE 2. Terminal connections.

Inputs			I/O	Mode	Power
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O 0 - I/O 7		
H	X	X	HI-Z	Standby	Standby
L	H	L	Data Output	Read	Active
L	H	H	HI-Z	Read	Active
L	L	X	Data Input	Write	Active

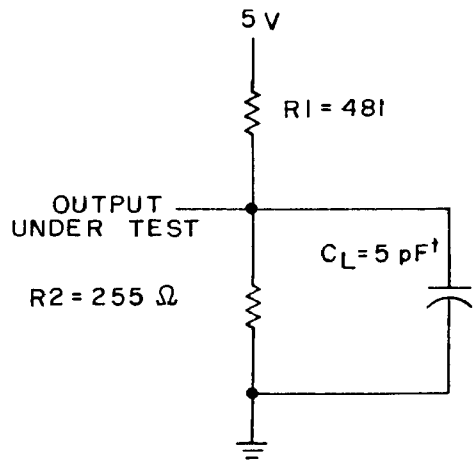
FIGURE 3. Truth table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1989—749-033



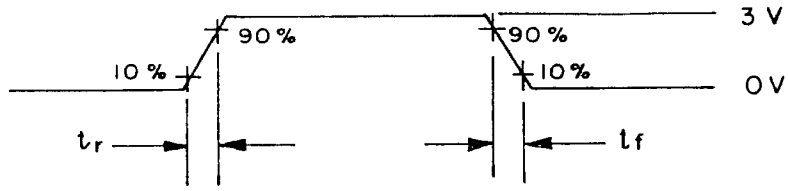
CONFIGURATION (a)

† C_L INCLUDES JIG AND SCOPE CAPACITANCES



CONFIGURATION (b)

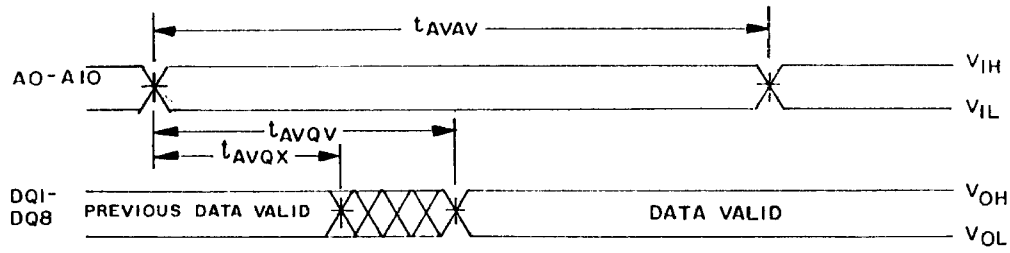
(FOR t_{ELQX}, t_{EHQZ}, t_{WLQZ} AND t_{OHQZ})



NOTE:
1. t_r and $t_f \leq 5$ ns.
2. All switching characteristics and timing requirements assume test conditions as depicted in configuration (a) and configuration (b) with timing references of 1.5 V (50% reference point) as shown in the subsequent timing diagrams.

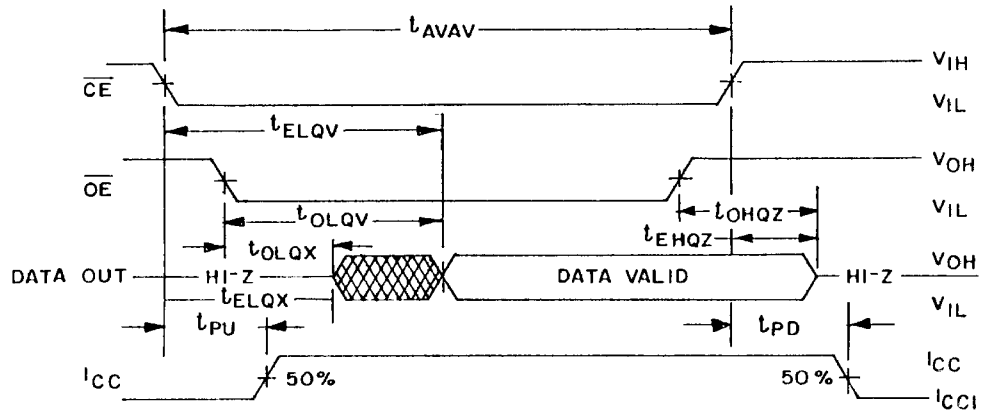
FIGURE 4. Load circuit and switching waveforms.

read cycle timing from address †



† When $\overline{WE}$ is high, $\overline{CE}$ is low, and $\overline{OE}$ is low, device is continuously selected.

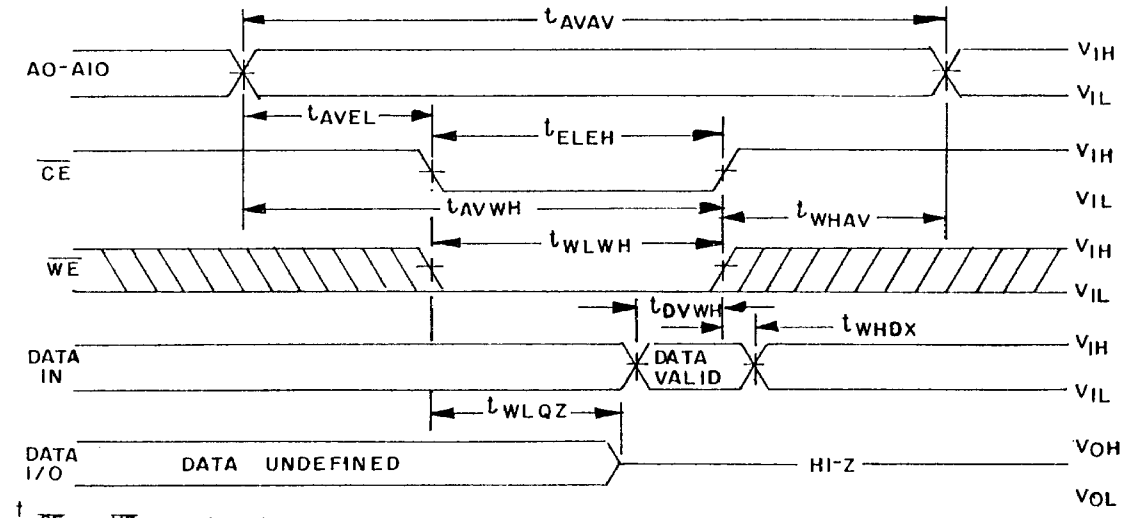
read cycle timing from chip enable ‡



‡ When $\overline{WE}$ is high, address is valid prior to or simultaneously with the high to low transition of $\overline{CE}$.

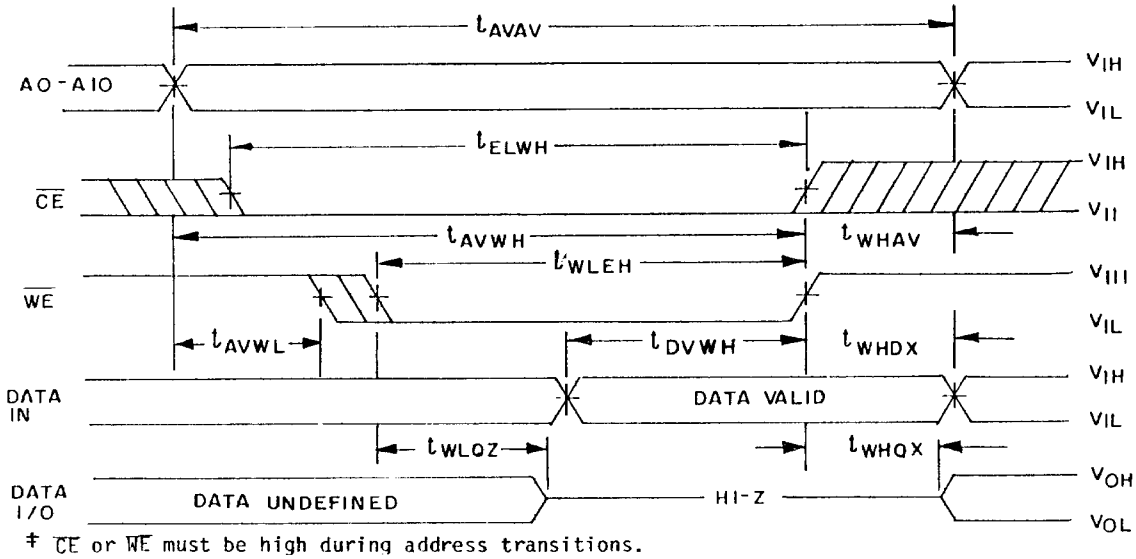
FIGURE 4. Load circuit and switching waveforms - Continued.

Write cycle timing controlled by from chip enable †



† $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
Data I/O pins enter high-impedance state, as shown when $\overline{CE}$ is held low during write.

Write cycle timing controlled by write enable ‡



‡ $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

The internal write time of the memory if defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold timing should be referenced o the rising edge of the signal that terminates the write.

FIGURE 4. Load circuit and switching waveforms - Continued.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for the initial charaterization and after any process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 tests sufficient to verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform the Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8874001JX	61772	6116LA35DB
5962-8874001KX	61772	6116LA35EB
5962-8874001LX	01295 61772	SMJ68CE16L-35JD 6116LA35TBD
5962-8874001XX	01295 61772	SMJ68CE16L-35FG 6116LA35L32B
5962-8874001YX	61772	6116LA35L24B
5962-88740013X	61772	6116LA35L28B
5962-8874002JX	61772	6116LA25DB
5962-8874002KX	61772	6116LA25EB
5962-8874002LX	01295 61772	SMJ68CE16L-25JD 6116LA25TBD
5962-8874002XX	01295 61772	SMJ68CE16L-25FG 6116LA25L32B
5962-8874002YX	61772	6116LA25L24B
5962-88740023X	61772	6116LA25L28B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 North Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448
61772	Integrated Device Technology, Incorporated 1566 Moffett Boulevard Salinas, CA 93905 Point of contact: 3236 Scott Boulevard Santa Clara, CA 95054