Ordering number : ENN7735

SANYO Semiconductors
DATA SHEET

CMOS IC

LC78605E — Compact Disc Player DSP with Built-in Microcontroller

Overview

The LC78605E CMOS IC implements the signal processing, servo control, LCD display, button state acquisition, and remote controller handling required by compact disc players without requiring a separate microcontroller. It provides the following basic functions: demodulation of the EFM signal from the optical pickup, deinterleaving, error detection and correction, 8× oversampling audio filters, D/A converter (with built-in analog low-pass filter), LCD display drivers, key acquisition (A/D) and control processing, and automatic discrimination and playback of CD-RW discs. Thus the LC78604E is ideal for implementing low-end CD players that support playback of CD-RW discs.
The LC78604E also provides a radio tuner frequency display function, and allows digital display of the selected frequency in manual tuning CD radio/cassette players.

Functions

- Implements the CD play/pause, stop, track selection, fast forward/fast rewind, repeat 1/repeat all, program setup/play/clear for up to 30 tracks, and shuffle play functions controlled from CD player buttons.

<Signal-Processing Block>

- The signal-processing block applies slicing at the correct level to the input HF signal, and converts that signal to an EFM signal. At the same time it generates a PLL clock signal with an average frequency of 4.3218MHz by comparing the phase with that of the internal VCO.
- A reference clock signal and all necessary timings can be generated using an external 16.9344MHz crystal.
- The disc motor speed is controlled by a frame phase difference signal created from the playback clock and the reference clock.
- Performs frame sync signal detection, protection, and interpolation to assure stable data readout.
- Demodulates the EFM signal and converts the result to 8-bit symbol data.
- Separates the subcode data from the EFM signal and outputs that data to the internal control processing block.
- After applying a CRC check to the subcode Q data, outputs that data to the internal control processing block.
- Buffers the demodulated EFM signal in internal RAM and compensates for up to ±4 frames of jitter due to fluctuations in the disc speed.
- Applies unscrambling and deinterleaving to the demodulated EFM signal in the stipulated order.
- Performs error detection, correction, and flag processing (C1: double, C2: double).
- Sets the C2 flags according to the C1 flags and the C2 check and applies interpolation and previous value hold processing to the output signal according to the C2 flags. This interpolation circuit implements 2-value interpolation. A previous value hold operation is applied if the C2 flags indicate errors for over 2 consecutive samples.
- The internal control processing block controls the track jump, focus start, disc motor start/stop, muting on/off, track count, and other operations.

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- Uses 8× oversampling digital filters to produce output data with improved continuity for the D/A converter.
- Built-in third-order noise shaper ΔΣ D/A converter and built-in analog low-pass filters
- Digital deemphasis function
- Zero cross muting
- Automatic discrimination and playback of CD-RW discs

<Display Block>

- Built-in LCD display driver supports 7-segment 3-digit plus symbol displays
- Monitor display for the play, program, repeat, random, and tuner functions

<Control Processing Block>

- A/D based key acquisition for play/pause, stop, forward scan, backward scan, repeat, program, and random functions.

Features

- 64-pin QIP
- Supply voltage: 3.3V single source

Specifications

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{SS} – 0.3 to V_{SS} + 4.0	V
Input voltage	V_{IN}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pdmax		300	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta=–20 to +75°C, V_{DD}=3.0V to 3.6V, V_{SS}=0V

Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}	DV_{DD}, XV_{DD}, LRV_{DD}, AV_{DD}		3.0		3.6	V
Input high-level voltage	V_{IH} (1)	DRF, DEFI		0.7V_{DD}		V_{DD}	V
	V_{IH} (2)	HFL, TES, FMAMB, REMOTE, PUIN, CLOSE, CDRESB, TUNERESB, MONI1 to 3		0.8V_{DD}		V_{DD}	V
	V_{IH} (3)	EFMI		0.6V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL} (1)	DRF, DEFI		0		0.3V_{DD}	V
	V_{IL} (2)	HFL, TES, MODE, FMAMB, REMOTE, PUIN, CLOSE, CDRESB, TUNERESB, MONI1 to 3		0		0.2V_{DD}	V
	V_{IL} (3)	EFMIN		0		0.4V_{DD}	V
Input level	V_{IN} (1)	EFMIN	Slice level control	0.66			Vp-p
	V_{IN} (2)	XIN16M, XIN32K	Capacitor coupled input	1.0			Vp-p
	V_{IN} (3)	Input amplitude applied to the coupling capacitor connected to the TUNERIN pin	* Conditions 1 * Conditions 2	0.05			Vrms
Operating frequency range	Fop	EFMIN				10	MHz
	Fam	TUNERIN	FMAMB="L"	0.5		5	MHz
	Ffm	TUNERIN	FMAMB="H"	50		120	MHz
Crystal oscillator frequency	FX16	XIN16M, XOUT16M			16.9344		MHz
Crystal oscillator frequency	FX32	XIN32K, XOUT32K			32.768		kHz

* Conditions 1: The coupling capacitor must be located as close as possible to the TUNERIN pin.

* Conditions 2: Coupling capacitor: 100pF ±20 pF

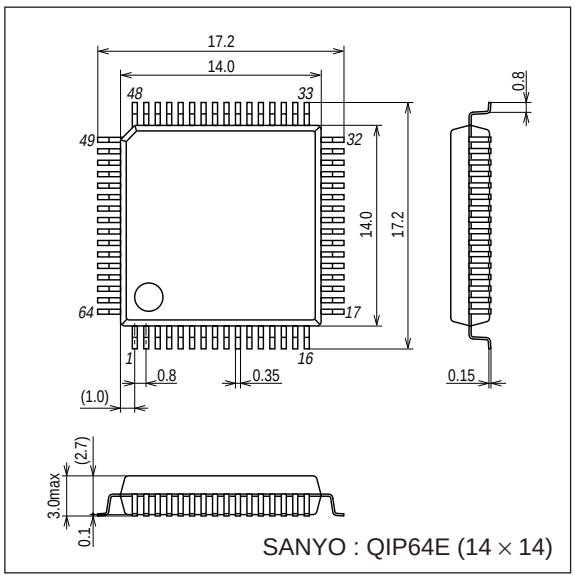
Electrical Characteristics at Ta=–20 to +75°C, V_{DD}=3.0V to 3.6V, V_{SS}=0V

Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				min	typ	max	
Current drain	I_{DD}	DV_{DD}, XV_{DD}, LRV_{DD}, AV_{DD}			20	30	mA
Input high-level current	I_{IH} (1)	DRF, DEFI, HFL, TES, FMAMB, REMOTE, PUIN, CLOSE, CDRESB, TUNERSB, EFMIN, TUNERIN	$V_{IN}=V_{DD}$			5	µA
	I_{IH} (2)	MONI1 to 3	$V_{IN}=V_{DD}$			100	µA
Input low-level current	I_{IL} (1)	DRF, DEFI, HFL, TES, FMAMB, REMOTE, CDRESB, TUNERSB, MONI1 to 3, MODE, EFMIN, TUNERIN	V_{IN}=0V	–5			µA
	I_{IL} (2)	PUIN, CLOSE	V_{IN}=0V	–100			µA
Output high-level voltage	V_{OH} (1)	CLK, RWB, RWC, COIN, CQCKB, DEFINT, TOFF, TGL, AMUTEB, DMUTEB	I_{OH}=–1mA	V_{DD}–0.4			V
	V_{OH} (2)	CLVO, JPO, SL+, SL–, MONI1 to 3	I_{OH}=–2mA	V_{DD}–0.4			V
	V_{OH} (3)	SEG1 to SEG7	I_{OH}=–0.01mA	V_{DD}–0.5			V
	V_{OH} (4)	COM1 to COM4	I_{OH}=–0.01mA	V_{DD}–0.5			V
Output low-level voltage	V_{OL} (1)	CLK, RWB, RWC, COIN, CQCKB, DEFINT, TOFF, TGL, AMUTEB, DMUTEB	I_{OL}=1mA			0.4	V
	V_{OL} (2)	CLVO, JPO, SL+, SL–, MONI1 to 3	I_{OL}=2mA			0.4	V
	V_{OL} (3)	SEG1 to SEG7	I_{OL}=0.01mA			0.5	V
	V_{OL} (4)	COM1 to COM4	I_{OL}=0.01mA			0.5	V
Output off leakage current	IOFF	PDO, CLVO, JPO	In the high-impedance output state	–5		+5	µA
Pull-up resistance	RPU	PUIN, CLOSE			80		kΩ
Pull-down resistance	RDW	MONI1 to 3			80		kΩ
Charge pump output current	IPDOH	PDO	ISET=100kΩ	80	100	120	µA
	IPDOL	PDO		–120	–100	–80	µA

Package Dimensions

unit : mm

3159A



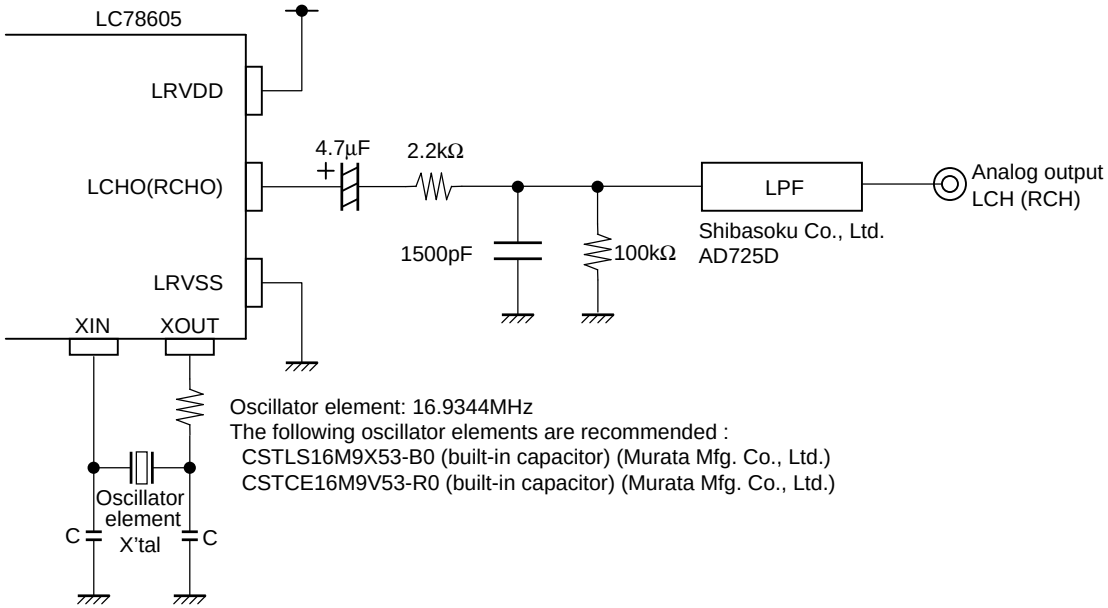
SANYO : QIP64E (14 × 14)

1-Bit D/A Converter Block Analog Characteristics at Ta=25°C, V_{DD}=3.3V, V_{SS}=0V

Parameter	Symbol	Pin name	Conditions	Ratings			Unit
				min	typ	max	
Total harmonic distortion	THD+N	LCHO, RCHO	With a 1kHz, 0dB signal input With the 20kHz low-pass filter (built into the AD725D) used		0.025	0.04	%
Dynamic range	DR	LCHO, RCHO	With a 1kHz, –60dB signal input With the 20kHz low-pass and A filters (built into the AD725D) used	85	87		dB
Signal-to-noise ratio	S/N	LCHO, RCHO	With a 1kHz, 0dB signal input With the 20kHz low-pass and A filters (built into the AD725D) used	88	90		dB
Crosstalk	CT	LCHO, RCHO	With a 1kHz, 0dB signal input With the 20kHz low-pass filter (built into the AD725D) used	80	82		dB

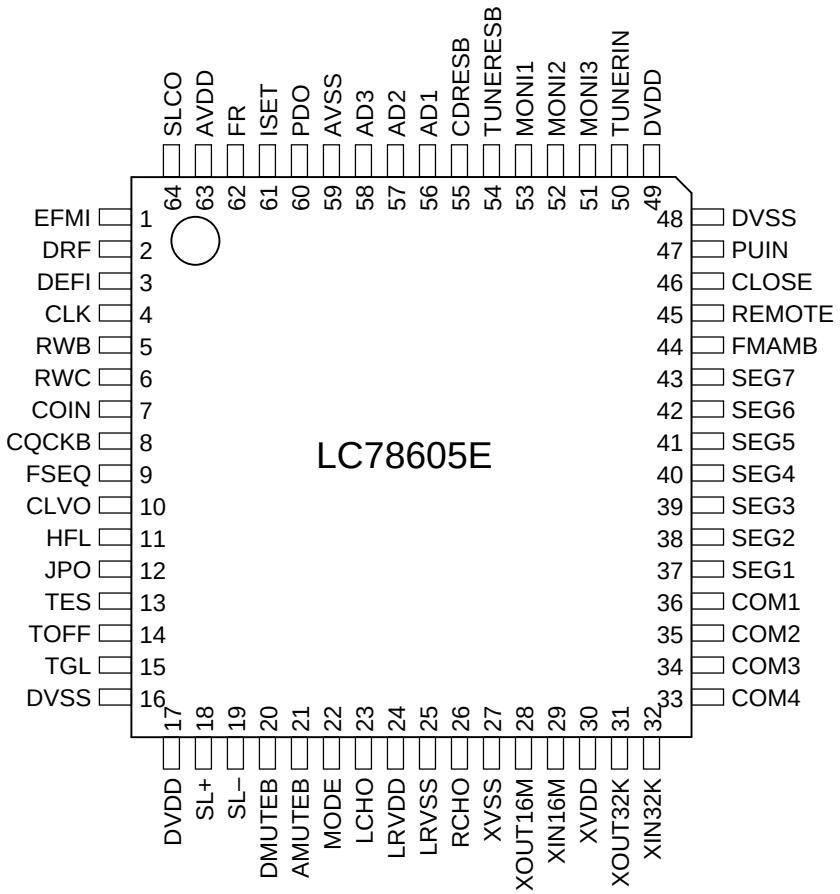
* : Measured in normal playback mode in the Sanyo 1-bit D/A converter reference circuit.

1-bit D/A converter output block reference circuit



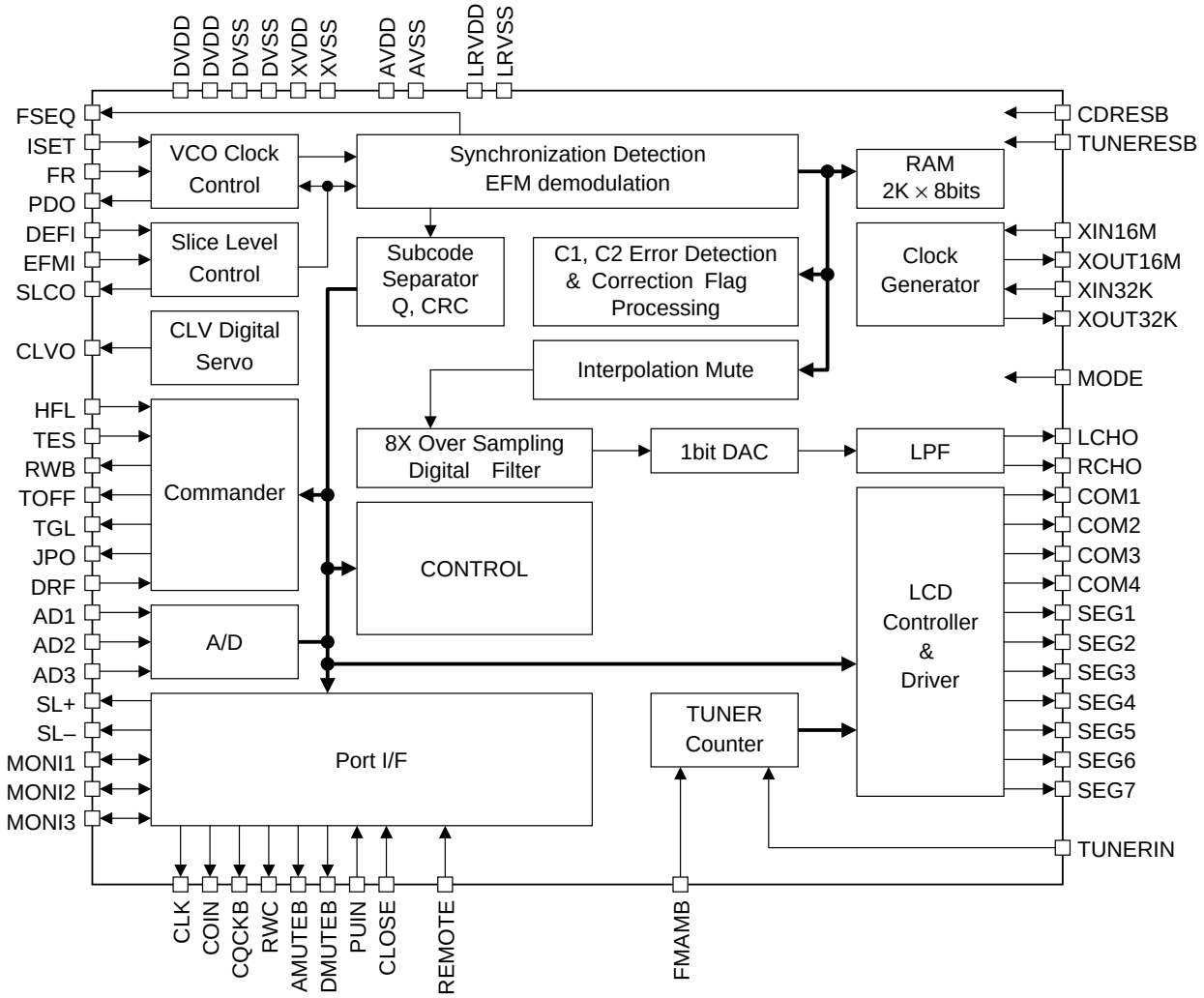
Oscillator element: 16.9344MHz
The following oscillator elements are recommended :
CSTLS16M9X53-B0 (built-in capacitor) (Murata Mfg. Co., Ltd.)
CSTCE16M9V53-R0 (built-in capacitor) (Murata Mfg. Co., Ltd.)

Pin Assignment



Top view

Equivalent Block Diagram



Pin Functions

Pin No.	Pin Name	I/O	Function	Pin state when CDRESB is low	Pin state when TUNERESB is low
1	EFMI	I	EFM signal input	—	—
2	DRF	I	DRF signal input	—	—
3	DEFI	I	Defect detection signal (DEF) input (Must be connected to ground if unused.)	—	—
4	CLK	O	ASP system clock output (132.3kHz [16.9344MHz/128])	Clock output	Undefined
5	RWB	O	RW support control signal Low-level output: Indicates that a CD-RW disc is being played High-level output: Indicates that a CD-DA/R disc is being played	Low-level output	Undefined
6	RWC	O	Command write control signal output	Low-level output	Undefined
7	COIN	O	Command data signal output	High-level output	Undefined
8	CQCKB	O	Command data transfer clock signal output	High-level output	Undefined
9	FSEQ	O	Sync signal detection output monitor A high level is output when the sync signal detected from the EFM signal matches the internally generated sync signal.	Low-level output	Undefined
10	CLVO	O	Spindle motor control signal output Low-level output: Decelerate High-level output: Accelerate High-impedance output: Neither accelerate nor decelerate	High-impedance output	Undefined
11	HFL	I	Track detection signal input (Schmitt trigger input)	—	—
12	JPO	O	Track jump control signal output Low-level output: When moving away from the center: decelerate When moving towards the center: accelerate High-level output: When moving away from the center: accelerate When moving towards the center: decelerate High-impedance output: Neither accelerate nor decelerate	High-impedance output	Undefined
13	TES	I	Tracking error signal input (Schmitt trigger input)	—	—
14	TOFF	O	Tracking off signal output Low-level output: Tracking on High-level output: Tracking off	High-impedance output	Undefined
15	TGL	O	Tracking gain switching signal output Low-level output: Gain increase	Undefined	Undefined
16	DVSS	—	Digital system ground. This pin must be connected to the 0V level.	—	—
17	DVDD	—	Digital system power supply	—	—
18	SL+	O	Sled feed signal outputs	Low-level output	Undefined
19	SL–	O		Low-level output	Undefined
20	DMUTEB	O	Driver muting control signal output Low-level output: When the driver is muted	Low-level output	Undefined
21	AMUTEB	O	Audio muting control signal output Low in audio mute mode	Low-level output	Undefined
22	MODE	I	Operating mode selection This pin must be connected to the 0V level.	—	—
23	LCHO	O	D/A converter left channel signal output	Undefined	Undefined
24	LRVDD	—	D/A converter power supply	—	—
25	LRVSS	—	D/A converter ground. This pin must be connected to the 0V level.	—	—
26	RCHO	O	D/A converter right channel signal output	Undefined	Undefined
27	XVSS	—	Digital system ground. This pin must be connected to the 0V level.	—	—
28	XOUT16M	O	Connections for a 16.9344MHz crystal oscillator element.	Clock output	Undefined
29	XIN16M	I	(Oscillation is stopped when TUNERESP is high.)	—	—
30	XVDD	—	Digital system power supply	—	—
31	XOUT32K	O	Connections for a 32.768kHz crystal oscillator element.	Undefined	Clock output
32	XIN32K	I	(Oscillation is stopped when CDRESB is high.)	—	—
33	COM4	O	Common driver output (4)	High-level output	High-level output
34	COM3	O	Common driver output (3)	High-level output	High-level output
35	COM2	O	Common driver output (2)	High-level output	High-level output
36	COM1	O	Common driver output (1)	High-level output	High-level output
37	SEG1	O	Segment output (1)	High-level output	High-level output
38	SEG2	O	Segment output (2)	High-level output	High-level output
39	SEG3	O	Segment output (3)	High-level output	High-level output
40	SEG4	O	Segment output (4)	High-level output	High-level output
41	SEG5	O	Segment output (5)	High-level output	High-level output
42	SEG6	O	Segment output (6)	High-level output	High-level output
43	SEG7	O	Segment output (7)	High-level output	High-level output

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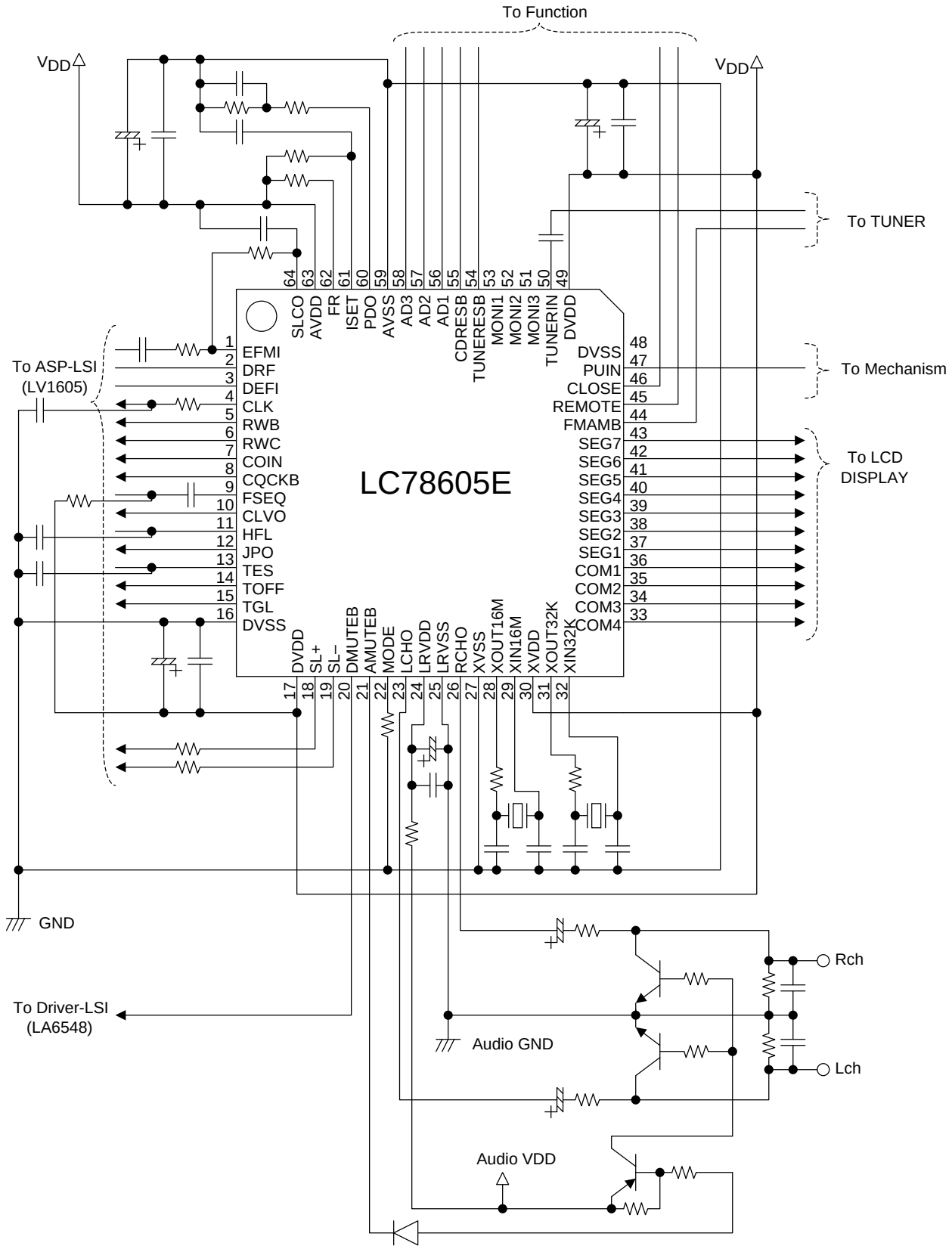
Pin No.	Pin Name	I/O	Function		Pin state when CDRESB is low	Pin state when TUNERESB is low
44	FMAMB	I	Tuner display switching selection input (Schmitt trigger input)		—	—
45	REMOTE	I	Remote control signal input (Schmitt trigger input)		—	—
46	CLOSE	I	Close switch detection signal input. A pull-up resistor is built in. (Schmitt trigger input)		—	—
47	PUIN	I	Limit switch detection signal input. A pull-up resistor is built in. (Schmitt trigger input)		—	—
48	DVSS	—	Digital system ground. This pin must be connected to the 0 V level.		—	—
49	DVDD	—	Digital system 3.3V power supply		—	—
50	TUNERIN	I	Tuner frequency display input		—	—
51	MONI3	I/O	Internal signal monitor pin 3. (Schmitt trigger input) A pull-down resistor is built in. (Default: input mode)		(Low-level output)	Undefined
52	MONI2	I/O	Internal signal monitor pin 2. (Schmitt trigger input) A pull-down resistor is built in. (Default: input mode)		(Low-level output)	Undefined
53	MONI1	I/O	Internal signal monitor pin 1. (Schmitt trigger input) A pull-down resistor is built in. (Default: input mode)		(Low-level output)	Undefined
54	TUNERESB	I	Reset input for this IC's tuner display block. A pull-down resistor is built in. This pin must be set low briefly after power is first applied.		—	—
55	CDRESB	I	Reset input for this IC's CD playback block. A pull-down resistor is built in. This pin must be set low briefly after power is first applied.		—	—
56	AD1	AI	Key operation A/D converter input 1		—	—
57	AD2	AI	Key operation A/D converter input 2		—	—
58	AD3	AI	Key operation A/D converter input 3		—	—
59	AVSS	—	Analog system ground. This pin must be connected to the 0V level.		—	—
60	PDO	AO	PLL system pins	External VCO control phase comparator output	Undefined	Undefined
61	ISET	AI		PDO output current adjustment resistor connection	—	—
62	FR	AI		VCO frequency range adjustment An external resistor must be connected between this pin and AVDD.	—	—
63	AVDD	—	Analog system power supply		—	—
64	SLCO	AO	Slice level control output		Undefined	Undefined

Sample Application Circuit



Notes on Application Design

While it goes without saying that this IC's absolute maximum ratings and allowable operating ranges (and recommended operating conditions) must be strictly observed to achieve reliability as a total system, adequate care is also required with respect to the operating environment and mounting conditions such as ambient temperature and static electricity. This section presents notes on items that require care during end product design and IC mounting.

- Handling Unused Pins
  If any unused input pins on this IC are left open the related internal circuits may become unstable. The instructions on handling unused pins for specific pins given in the technical documentation must be followed. Also note that unused output pins must not be shorted to power, ground, or other outputs.

- Latchup Prevention
  — The stipulated supply voltage must be applied to each power supply pin. If there are multiple pins for which the same supply voltage is stipulated, the same potential must be applied to all those pins.
  — Overvoltages and abnormal noise must not be applied to this IC.
  — In general, latchup can be prevented by holding unused input pins fixed at either V_{DD} or V_{SS}. However, the handling of each pin must follow the specific instruction in the pin functions documentation.
  — The outputs must not be shorted.

- Interface Notes
  When the inputs and outputs of different devices are connected, malfunctions may occur if the input V_{IL}/V_{IH} levels do not match the corresponding output V_{OL}/V_{OH} levels. Level shifters must be inserted to prevent destruction of the devices if devices with differing supply voltages, such as may occur in two power supply system applications, are connected.

- Load Capacitance and Output Current
  — When connected to high capacitance loads, lines may be melted since the effect of such loads is the same as the load being shorted for an extended period. Also, charge/discharge currents may result in noise that may degrade equipment performance and cause malfunctions. The recommended load capacitance ratings must be observed.
  — Excessive output sink or source currents can cause similar problems. Observe the maximum allowable power dissipation ratings and use this IC within the recommended current value range.

- Notes on Power Application and Power-on Reset
  — There are cases where special care is required at power on, during a reset, and after a reset is cleared. Refer to the device specifications and design applications taking these concerns into account.
  — This IC's output pin states, I/O settings, and register values are undefined when power is first applied. The operation of items that are defined by a reset operation or mode settings is only guaranteed after the corresponding reset or setting operation. A reset must be applied to this IC after power is first applied. The states immediately after power on of pins and registers that are not explicitly defined cannot be relied on: they may differ from versions of the same product purchased at different times.

- Notes on thermal design
  The failure rate of semiconductor devices is accelerated greatly by increases in ambient temperature or power consumption. To assure high reliability, design the application heat dissipation system to provide adequate margin for variations in ambient conditions.

- Notes on PCB pattern design
  — Ideally, there should be separate power supply and ground lines for each system to reduce the influence of shared impedances.
  — The power supply and ground lines should be as wide and as short as possible, and the impedance to high frequencies should be as small as possible. Ideally, decoupling capacitors (0.01 to 1μF) and 100 to 220μF capacitors should be inserted between each power supply/ground pair. However, note that latchup may occur if the values of these capacitors are too large.
  *: In the servo systems, the same handling is required for the V_{REF} reference voltage line as well as for the driver V_{CC} and ground lines. The driver ground lines must be especially wide and located under the device to provide a heat dissipating effect.

*: If a current output type pickup is used, the photoreceptor connector must be located as close as possible to the ASP RF input. If a voltage output type pickup is used, the I/V conversion resistors located at the ASP input must be located as close as possible to the ASP RF input.

— The EFM signal line must be made as short as possible, and must either be located well away from adjacent lines or must be run between ground or power supply level lines as shield lines. Since the slice level controller output (SLCO) can easily introduce noise in the EFM signal line, the resistor connected to the output pin must be located as close to that pin as possible. Note that if that resistor has a relatively small value, spurious radiation problems may be aggravated and that if the resistor has a larger value, the output level may become problematic.

— The crystal oscillator circuit must be surrounded by the ground pattern.

— The TUNER pin coupling capacitor must be located as close to the IC as possible.

• Other Notes

If there are any points that are unclear or if you have any questions, contact your Sanyo representative during the design phase.

This IC is a special-purpose device designed for CD player applications, and has specifications that differ from those of general-purpose logic devices. End products must be designed to operate in a failsafe manner appropriate for the application, and application operation must be verified using test equipment.