16-bit bus transceiver/register (3-State)

74ABT16646
74ABTH16646

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power–up 3-State
- Power–up reset
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA
- Latch–up protection exceeds 500mA per JEDEC Std 17
- 74ABTH16646 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16646 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16646 16-bit transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($n\overline{OE}$) and Direction (nDIR) pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (nSAB, nSBA) pins determine whether data is stored or transferred through the device in real-time. The nDIR determines which bus will receive data when the $n\overline{OE}$ is active Low. In the isolation mode ($n\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

Two options are available, 74ABT16646 which does not have the bus-hold feature and 74ABTH16646 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	3.3 2.7	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or V_{CC}; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} =5.5V	550	µA
		Outputs low; V_{CC} =5.5V	9	mA

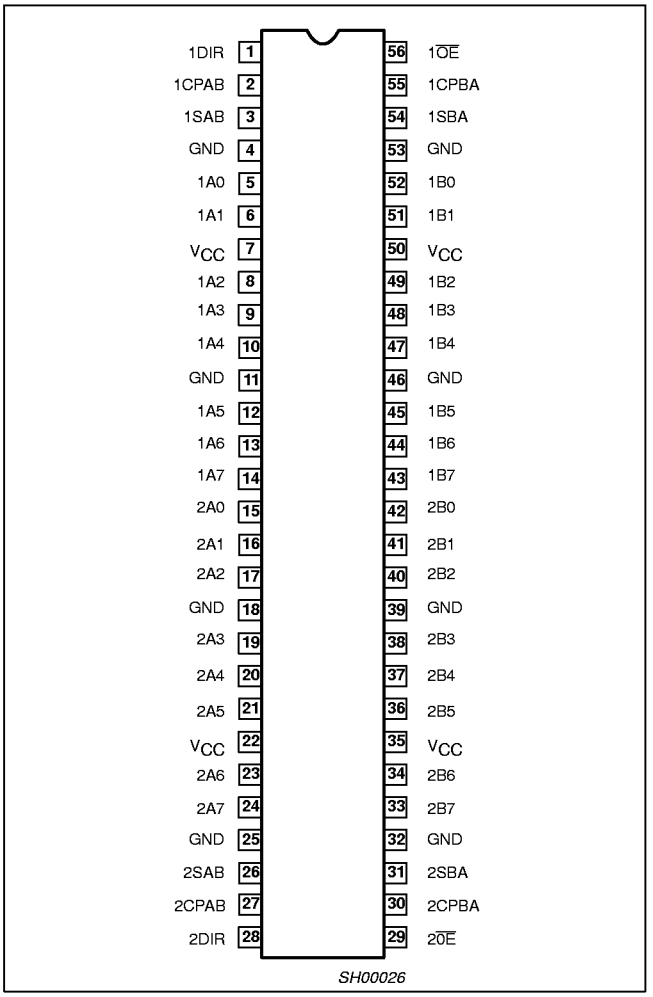
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16646 DL	BT16646 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16646 DGG	BT16646 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16646 DL	BH16646 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16646 DGG	BH16646 DGG	SOT364-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
1, 28	1DIR, 2DIR	Direction control inputs
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
56, 29	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION

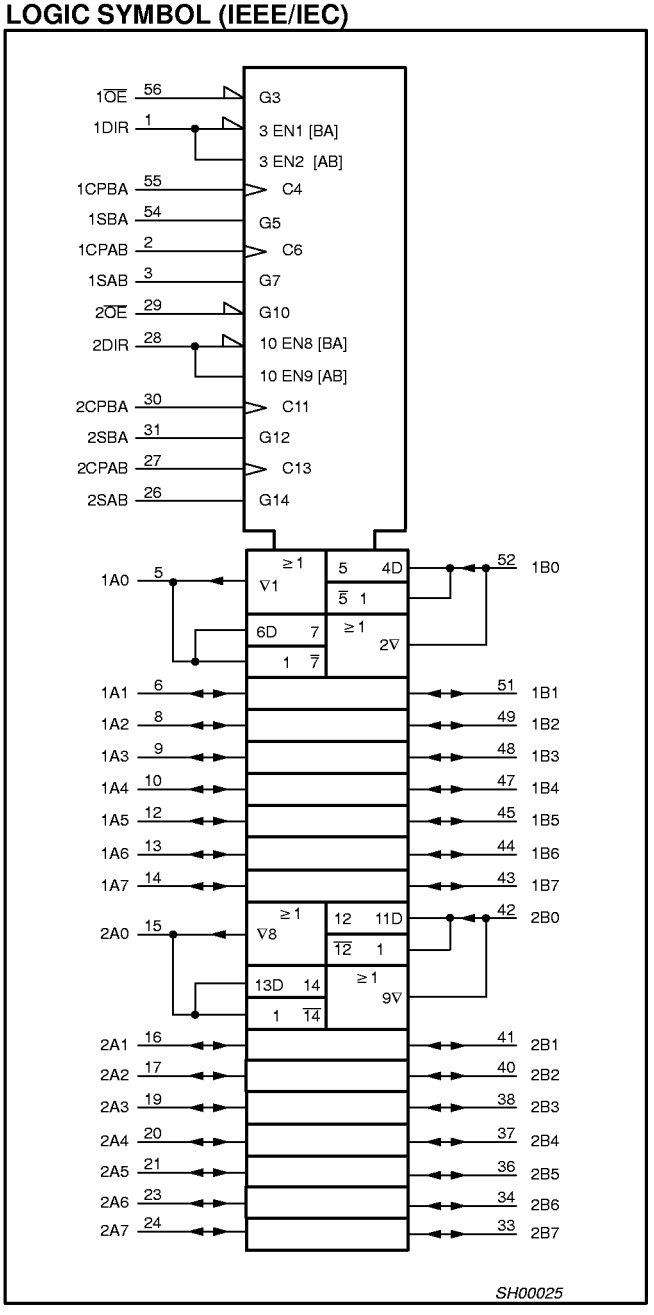


FUNCTION TABLE

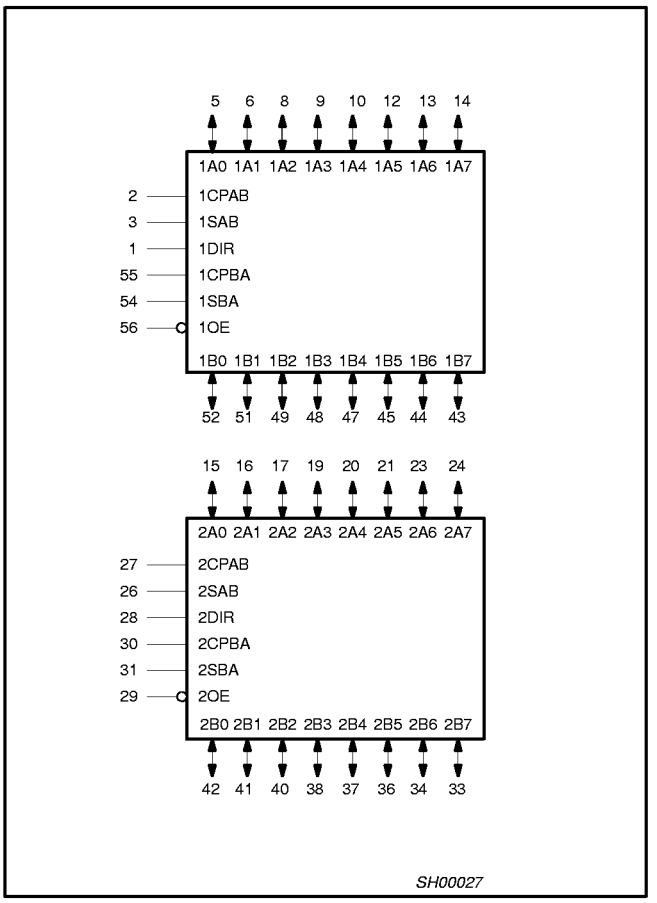
INPUTS						DATA I/O		OPERATING MODE
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low–to–High transition of the clock.

LOGIC SYMBOL (IEEE/IEC)

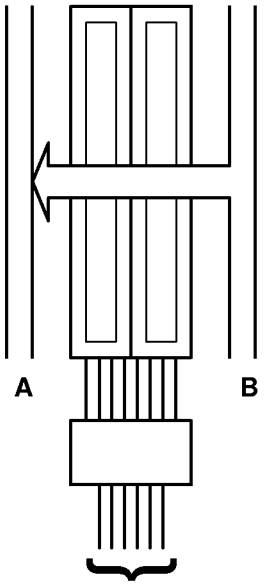


LOGIC SYMBOL



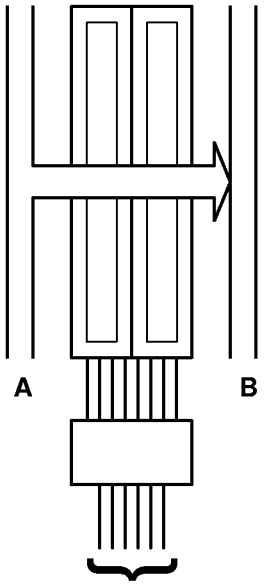
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT16646.

REAL TIME BUS TRANSFER BUS B TO BUS A



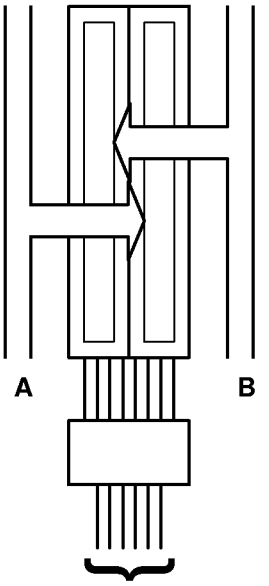
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



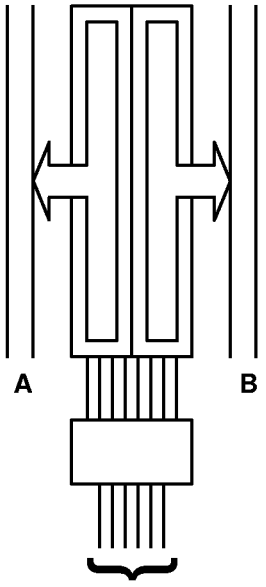
$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	H	↑	X	X	X
L	L	X	↑	X	X
H	X	↑	↑	X	X

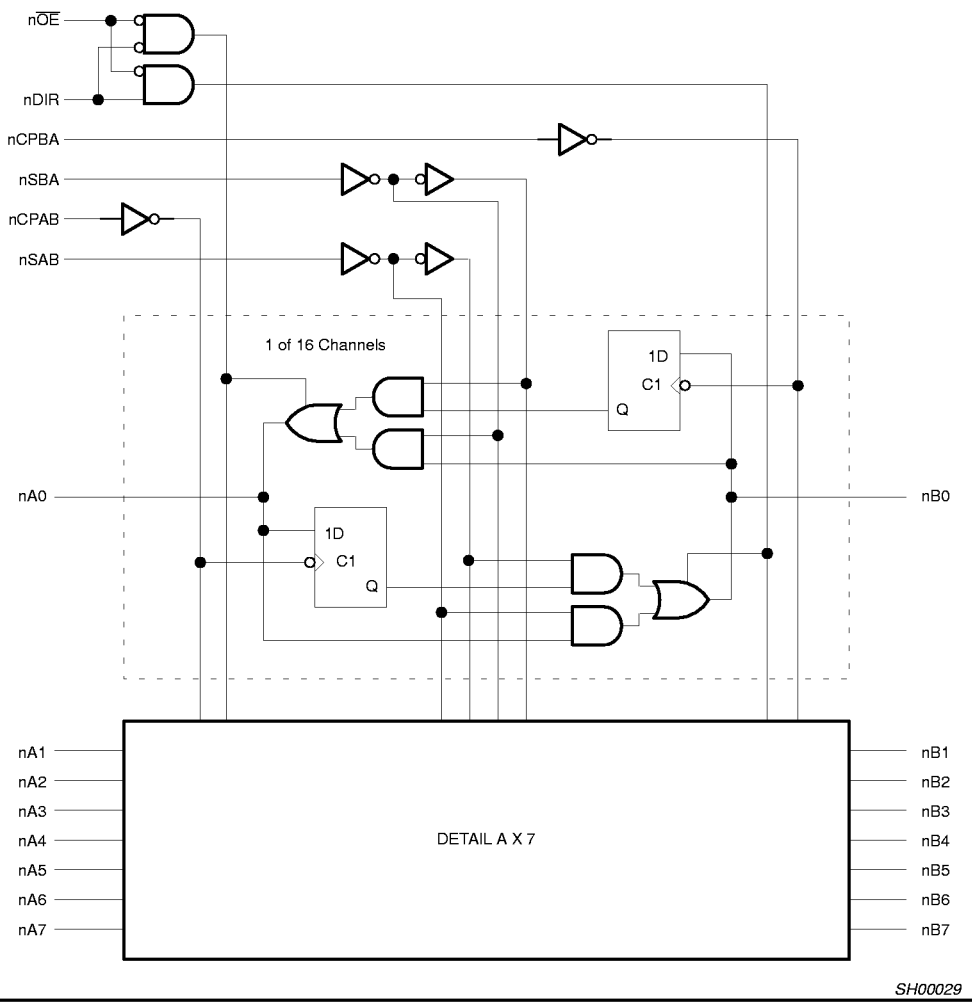
TRANSFER STORED DATA TO A OR B



$n\overline{OE}$	nDIR	nCPAB	nCPBA	nSAB	nSBA
L	L	X	H | L	X	H
L	H	H | L	X	H	X

SH00028

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.35	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V; Control pins		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A or B Ports[5] 74ABTH16646	V_{CC} = 4.5V; V_I = 0.8V	35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V	–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O = 4.5V; V_I = 0.0V or 5.5V		±2.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = X		±1.0	±50		±50	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		1.0	10		10	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.55	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.55	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16646	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16646	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.0V, with a transition time of up to 100msec. From V_{CC} = 21.V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	125			125		MHz
t_{PLH} t_{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	3.3 2.7	4.0 4.1	1.5 1.5	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	2.3 2.0	3.2 4.1	1.0 1.0	3.9 4.6	ns
t_{PLH} t_{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2, 3	1.0 1.0	3.1 2.7	4.3 4.3	1.0 1.0	5.0 5.0	ns
t_{PZH} t_{PZL}	Output enable time $n\overline{OE}$ to nAx or nBx	5, 6	1.0 1.5	3.2 3.3	4.6 4.9	1.0 1.5	5.5 5.7	ns
t_{PHZ} t_{PLZ}	Output disable time $n\overline{OE}$ to nAx or nBx	5, 6	1.5 1.5	3.5 2.7	4.9 4.1	1.5 1.5	5.4 4.5	ns
t_{PZH} t_{PZL}	Output enable time nDIR to nAx or nBx	5, 6	1.0 1.5	4.1 4.3	4.8 4.8	1.0 1.5	5.4 5.6	ns
t_{PHZ} t_{PLZ}	Output disable time nDIR to nAx or nBx	5, 6	2.0 1.5	3.6 2.7	5.7 5.1	2.0 1.5	6.7 5.9	ns

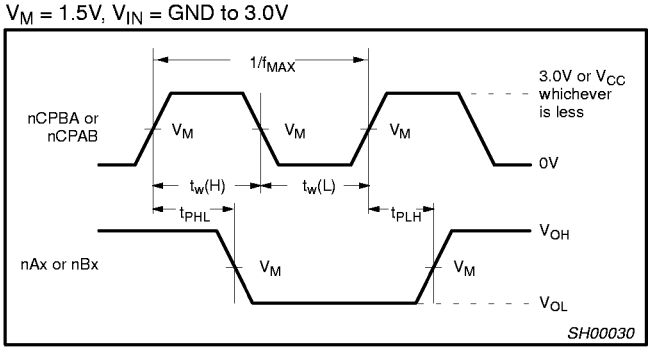
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

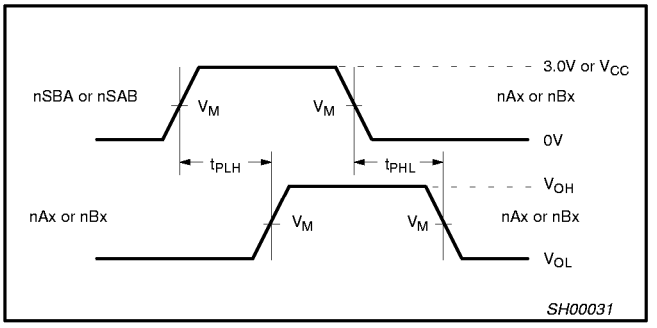
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = -40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time nAx to nCPAB, nBx to nCPBA	4	2.0 1.5	1.0 0.8	2.0 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time nAx to nCPAB, nBx to nCPBA	4	1.5 1.0	0.0 –0.7	1.5 1.0	ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low nCPAB or nCPBA	1	4.5 3.0	2.5 2.0	4.5 3.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



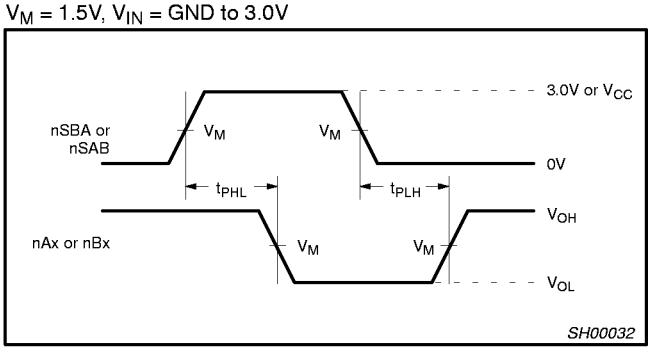
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



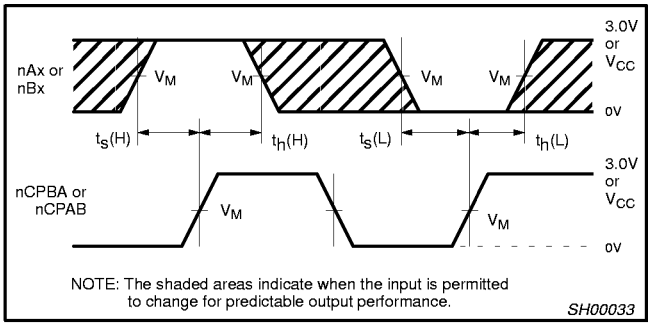
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx

AC WAVEFORMS (Continued)

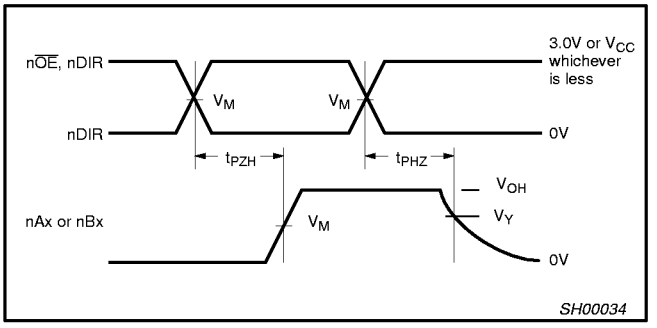
V_M = 1.5V, V_{IN} = GND to 3.0V



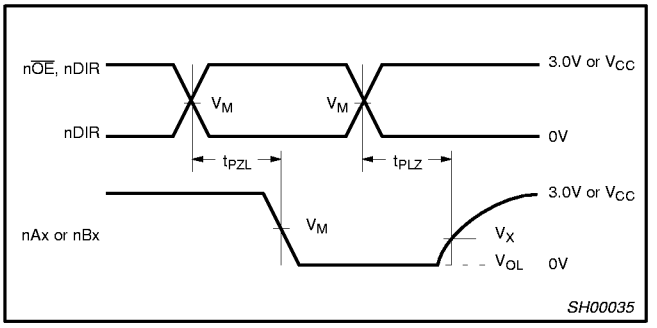
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times

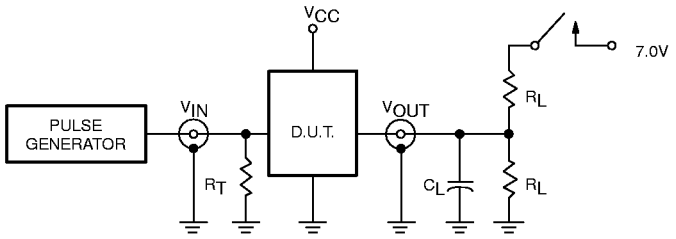


Waveform 5. 3–State Output Enable Time to High Level and Output Disable Time from High Level

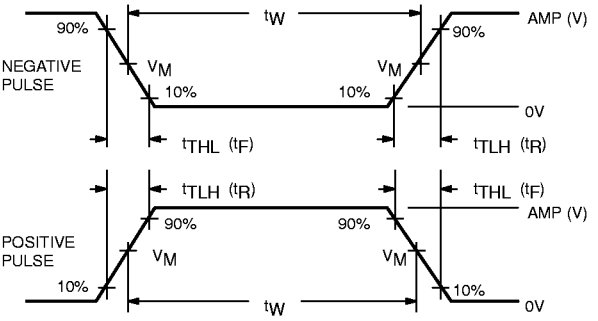


Waveform 6. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

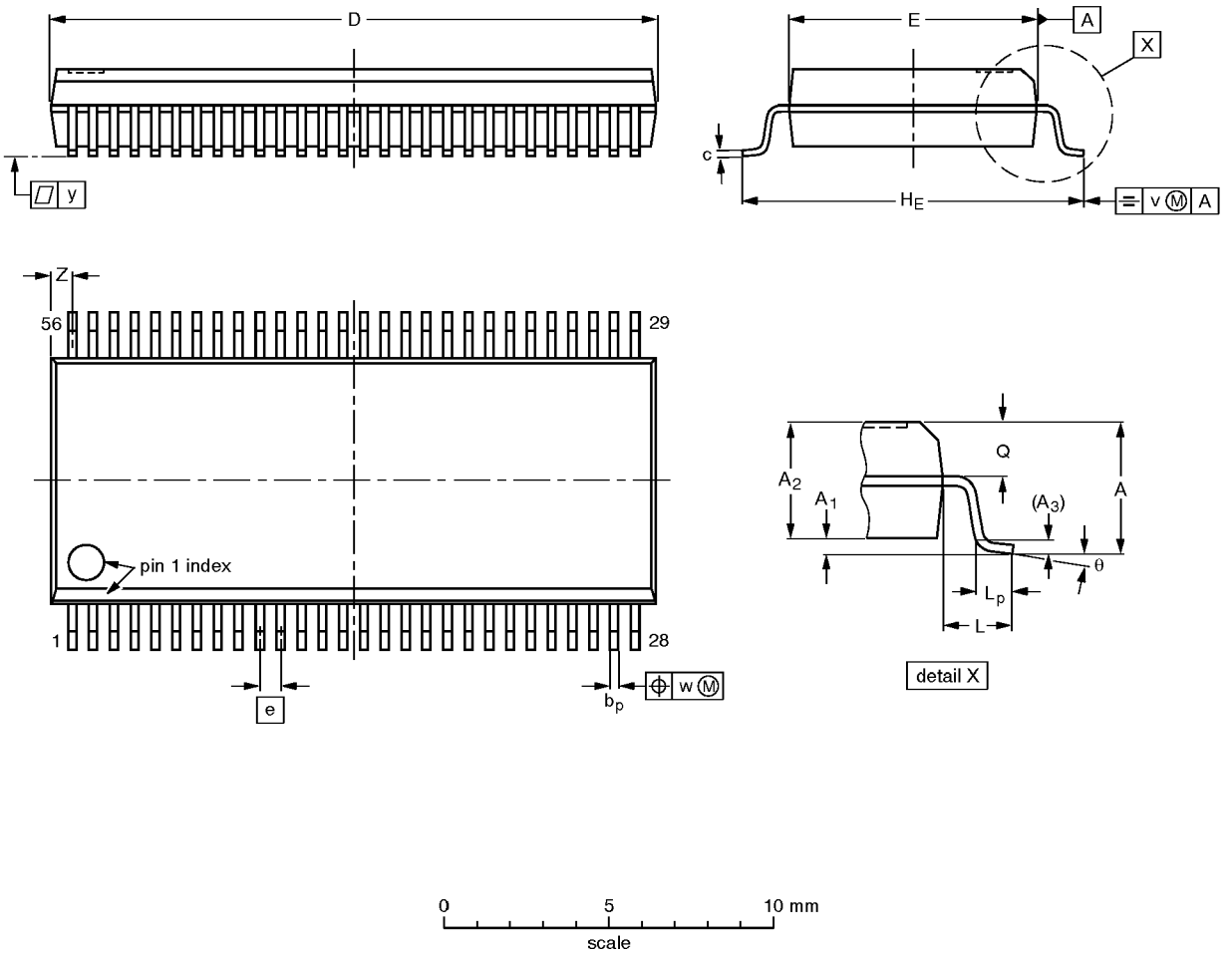
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm SOT371-1



DIMENSIONS (mm are the original dimensions)

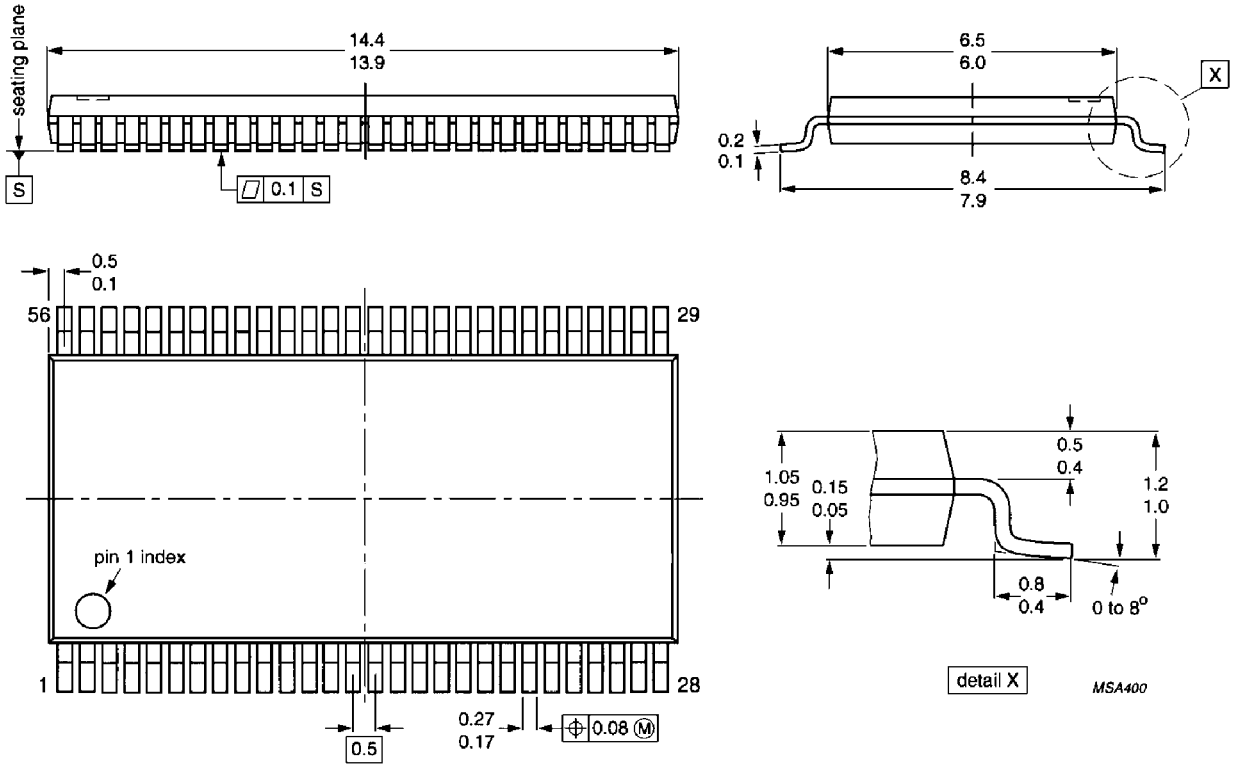
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.