

# IRF737LCPbF

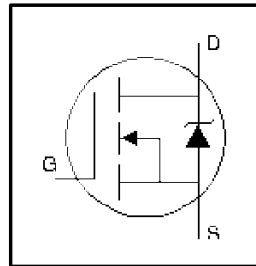
## HEXFET® Power MOSFET

- Reduced Gate Drive Requirement
- Enhanced 30V  $V_{GS}$  Rating
- Reduced  $C_{ISS}$ ,  $C_{OSS}$ ,  $C_{RSS}$
- Extremely High Frequency Operation
- Repetitive Avalanche Rated
- Lead-Free

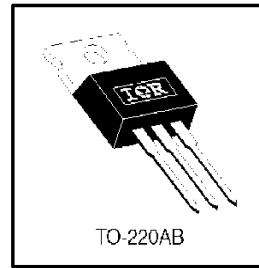
### Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristics of HEXFETs offer the designer a new standard in power transistors for switching applications.



$V_{DSS} = 300V$
$R_{DS(on)} = 0.75\Omega$
$I_D = 6.1A$



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	6.1	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.9	
$I_{DM}$	Pulsed Drain Current ①	24	
$P_D @ T_C = 25^\circ C$	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	120	mJ
$I_{AR}$	Avalanche Current ①	6.1	A
$E_{AR}$	Repetitive Avalanche Energy ①	7.4	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	3.4	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf·in (1.1N·m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.7	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

# IRF737LCPbF

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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	300	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.391	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.75	$\Omega$	$V_{GS} = 10V, I_D = 3.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	2.7	—	—	S	$V_{DS} = 50V, I_D = 3.7A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 300V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 240V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	—	17	nC	$I_D = 6.1A$
$Q_{gs}$	Gate-to-Source Charge	—	—	4.8		$V_{DS} = 240V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	7.6		$V_{GS} = 10V$ , See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	6.6	—	ns	$V_{DD} = 150V$
$t_r$	Rise Time	—	21	—		$I_D = 6.1A$
$t_{d(off)}$	Turn-Off Delay Time	—	13	—		$R_G = 12\Omega$
$t_f$	Fall Time	—	12	—		$R_D = 24\Omega$ , See Fig. 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	430	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	120	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	9.2	—		$f = 1.0\text{MHz}$ , See Fig. 5



## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	6.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ④	—	—	24		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 6.1A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	320	490	ns	$T_J = 25^\circ\text{C}, I_F = 6.1A$
$Q_{rr}$	Reverse Recovery Charge	—	1.5	2.2	$\mu C$	$di/dt = 100A/\mu s$ ④

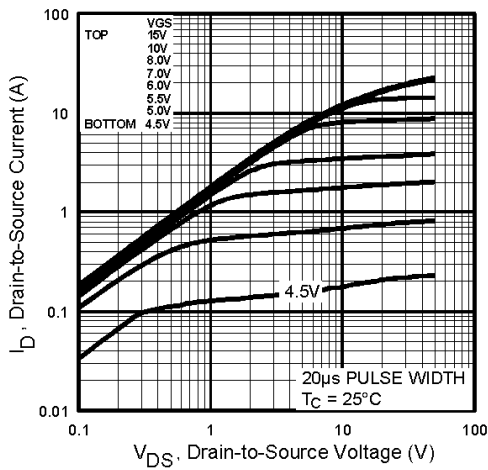
### Notes:

① Repetitive rating: pulse width limited by max. junction temperature. ( See fig. 11 )

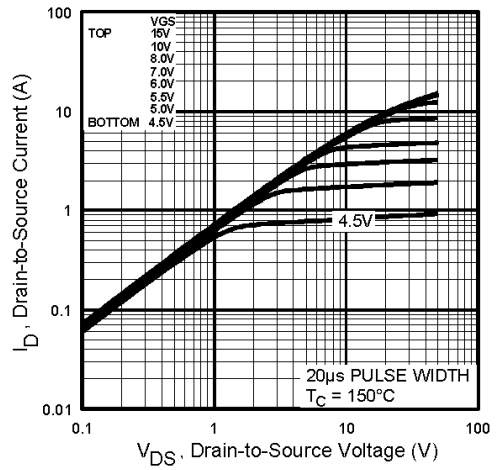
③  $I_{SD} \leq 6.1A, di/dt \leq 270A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

②  $V_{DD} = 25V, \text{ starting } T_J = 25^\circ\text{C}, L = 5.7\text{mH}$   
 $R_G = 25\Omega, I_{AS} = 6.1A.$  (See Figure 12)

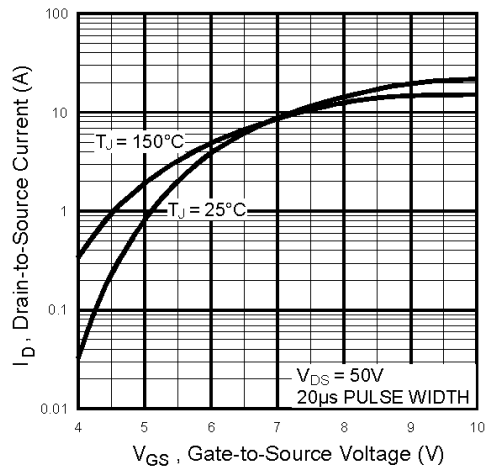
④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .



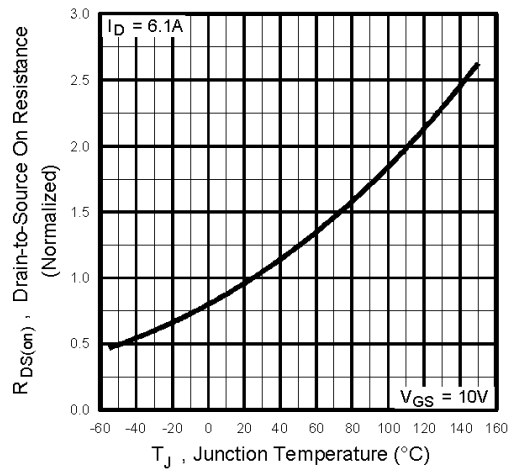
**Fig 1.** Typical Output Characteristics,  
 $T_J = 25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_J = 150^\circ\text{C}$

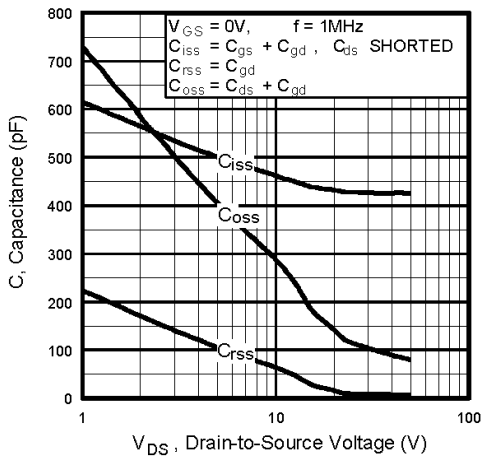


**Fig 3.** Typical Transfer Characteristics

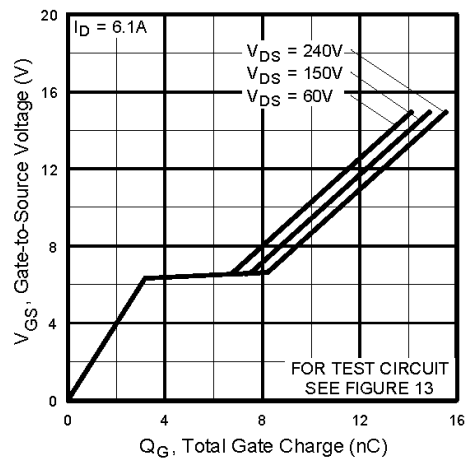


**Fig 4.** Normalized On-Resistance  
 Vs. Temperature

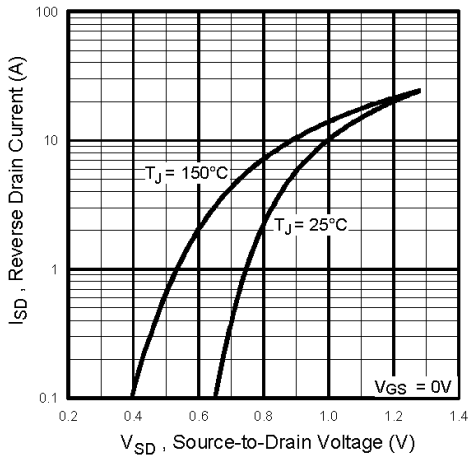
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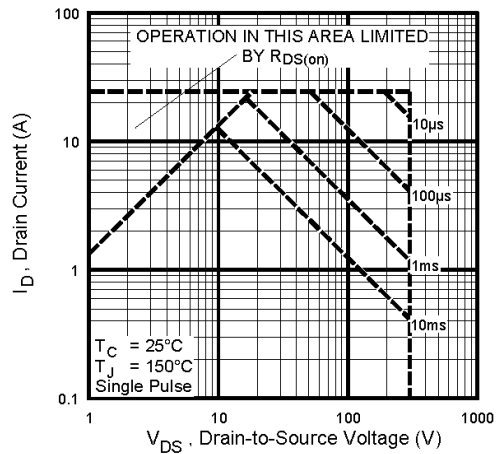
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



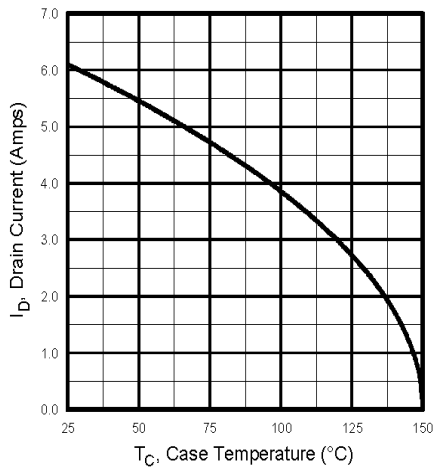
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



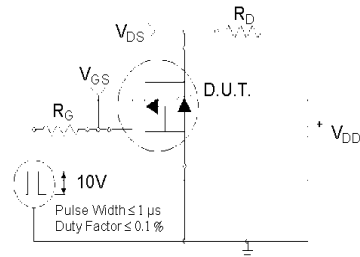
**Fig 7.** Typical Source-Drain Diode Forward Voltage



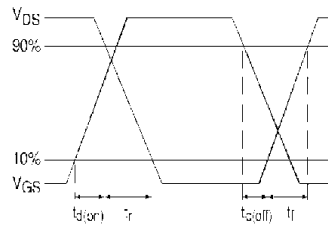
**Fig 8.** Maximum Safe Operating Area



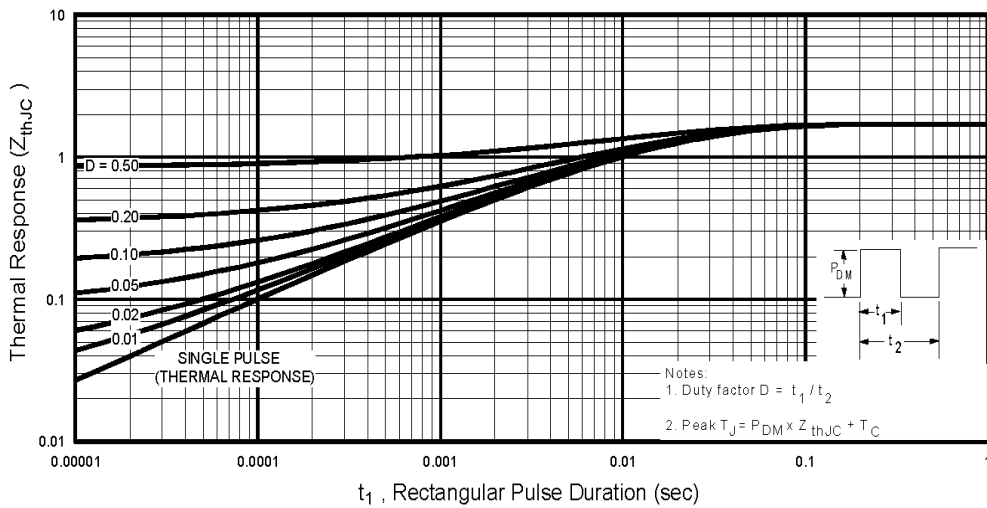
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

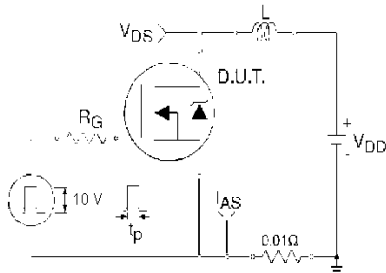


**Fig 10b.** Switching Time Waveforms

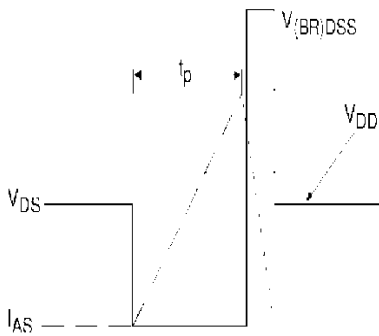


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

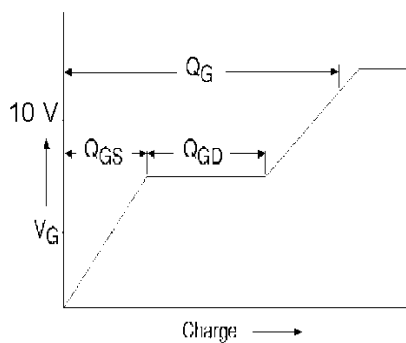
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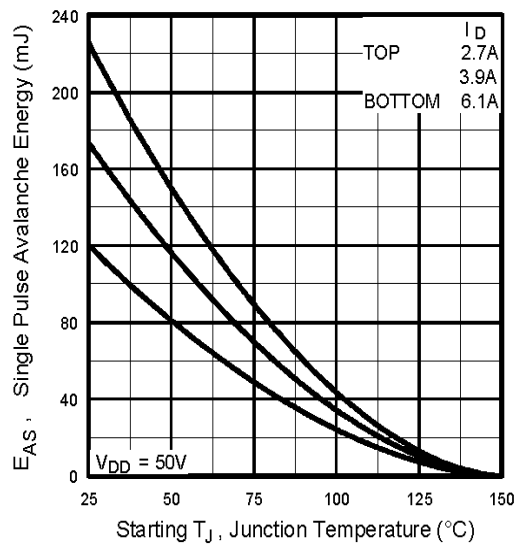
**Fig 12a.** Unclamped Inductive Test Circuit



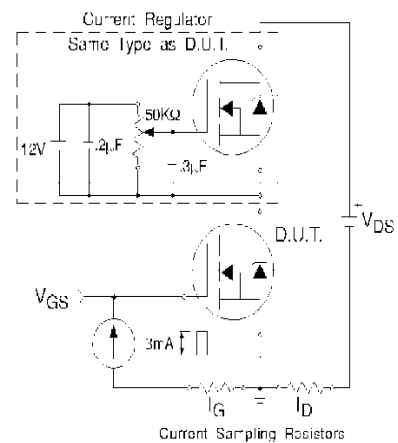
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

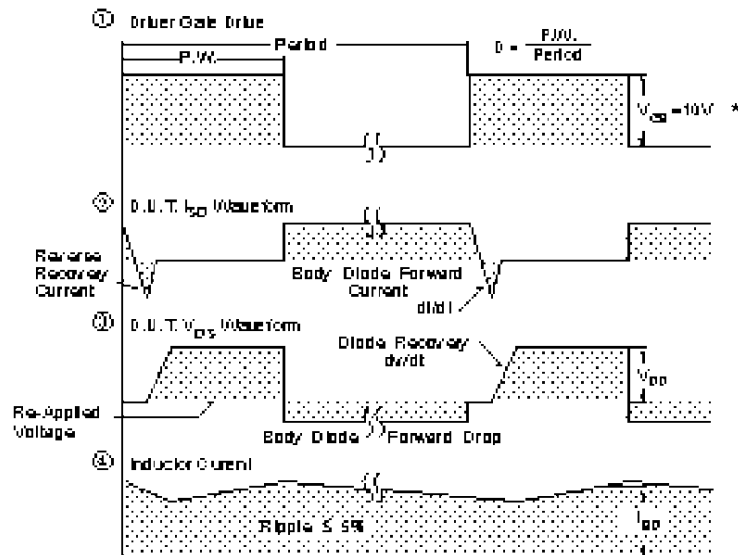
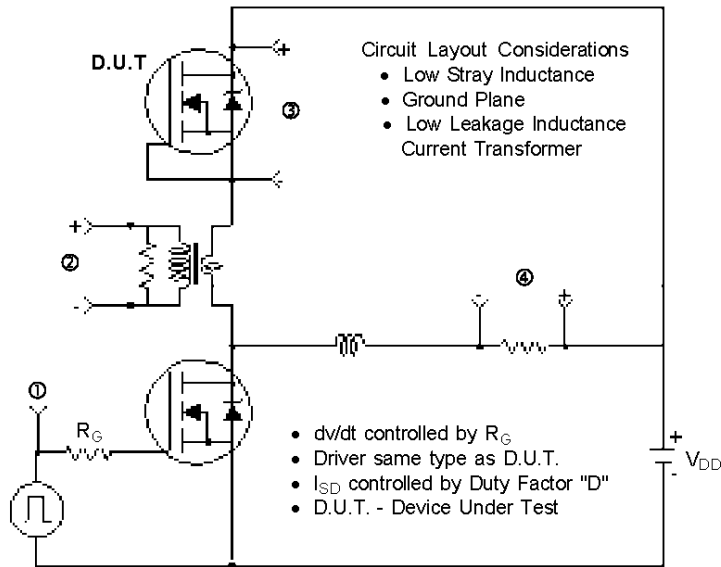


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



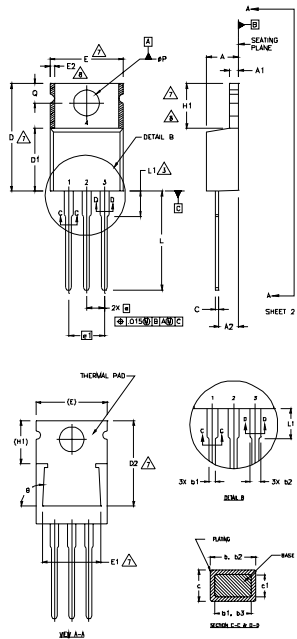
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

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## TO-220AB Package Outline



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2 DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS)
  - 3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
  - 6 CONTROLLING DIMENSION - INCHES.
  - 7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
  - 8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

**LEAD ASSIGNMENTS**

**HELETT**

- 1- GATE
- 2- DRAIN
- 3- SOURCE

**BASEL COPACK**

- 1- GATE
- 2- COLLECTOR
- 3- EMITTER

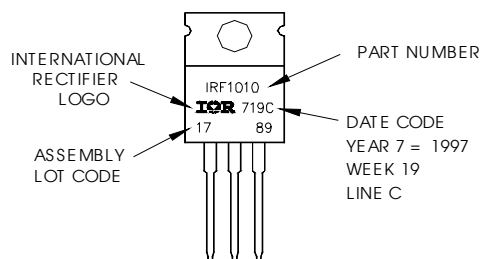
**DODES**

- 1- ANODE/OPEN
- 2- CATHODE
- 3- ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.62	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.356	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	3
ØP	3.54	4.08	.139	.161	
Ø	2.54	3.42	.100	.135	
Ø	90°-93°		90°-93°		

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

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