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2N5518

DIFFERENTIAL PAIRS N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTORS

ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage . . . . . -40 V
Gate Current . . . . . 50 mA
Device Dissipation (each side), T_A = 85° C, (derate 2.0 mW/°C . . . . . 250 mW
Total Device Dissipation, T_A = 85° C, (derate 3.0 mW/° C) . . . . . 375 mW
Storage Temperature Range . . . . . -65 to +150° C

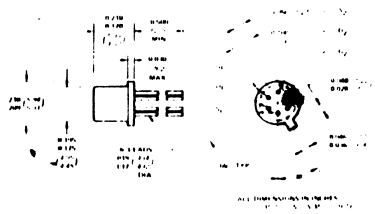
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Test Conditions		Min	Max	Unit
I_{GSS}	Gate Reverse Current	V_{GS} = -30 V, V_{DS} = 0	25° C		-250	pA
			150° C		-250	nA
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1 μA, V_{DS} = 0		-40		V
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = 20 V, I_D = 1 nA		-0.7	-4	V
I_{DSS}	Drain Current at Zero Gate Voltage †	V_{DS} = 20 V, V_{GS} = 0		0.5	7.5	mA
g_{fs}	Common-Source Forward Transconductance †		f = 1 kHz	1000	4000	μmho
g_{oss}	Common-Source Output Conductance				10	μmho
C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1 MHz		5	pF
C_{iss}	Common-Source Input Capacitance				25	pF
$\bar{e}_n$	Equivalent Input Noise Voltage	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz		30	$\frac{nV}{\sqrt{Hz}}$
			f = 1 kHz		10	
I_G	Gate Current		25° C		-100	pA
			125° C		-100	nA
V_{GS}	Gate Source Voltage			-0.2	-3.8	V
g_{fs}	Common-Source Forward Transconductance †		f = 1 kHz	500	1000	μmho
g_{oss}	Common-Source Output Conductance				1	μmho

*JEDEC Registered Data
† Pulse test required, pulsewidth 300 μs, duty cycle ≤ 3%

*MATCHING CHARACTERISTICS

Characteristic		Test Conditions		Min	Max	Unit
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage †	V_{DS} = 20 V, V_{GS} = 0		0.95	1	--
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	V_{DG} = 20 V, I_D = 200 μA	125°C		10	nA
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio †		f = 1 kHz	0.95	1	--
$\lvert g_{oss1} - g_{oss2} \rvert$	Differential Output Conductance		f = 1 kHz		0.1	μmho
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage				15	mV
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift ‡		T_A = 25°C T_B = 125°C		40	μV/°C
			T_A = -55°C T_B = 25°C		40	μV/°C
CMRR	Common Mode Rejection Ratio **	V_{DD} = 10 to 20 V, I_D = 200 μA				dB



All leads isolated from case

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† Pulse test required, pulsewidth 300 μs, duty cycle ≤ 3%

‡ Measured at end points, T_A and T_B. NS

**CMRR = 20 $\log_{10} \Delta V_{DD} / \Delta \lvert V_{GS1} - V_{GS2} \rvert$ (ΔV_{DD} = 10V)