IS66WV1M16DALL
IS66WV1M16DBLL

PRELIMINARY INFORMATION
MARCH 2011

16Mb LOW VOLTAGE, ULTRA LOW POWER PSEUDO CMOS STATIC RAM

FEATURES

- High-speed access time:
  – 70ns (IS66WV1M16DALL/DBLL)
  – 55ns (IS66WV1M16DBLL)
- CMOS low power operation
- Single power supply
  – V_{DD} = 1.7V - 1.95V (IS66WV1M16DALL)
  – V_{DD} = 2.5V - 3.6V (IS66WV1M16DBLL)
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

DESCRIPTION

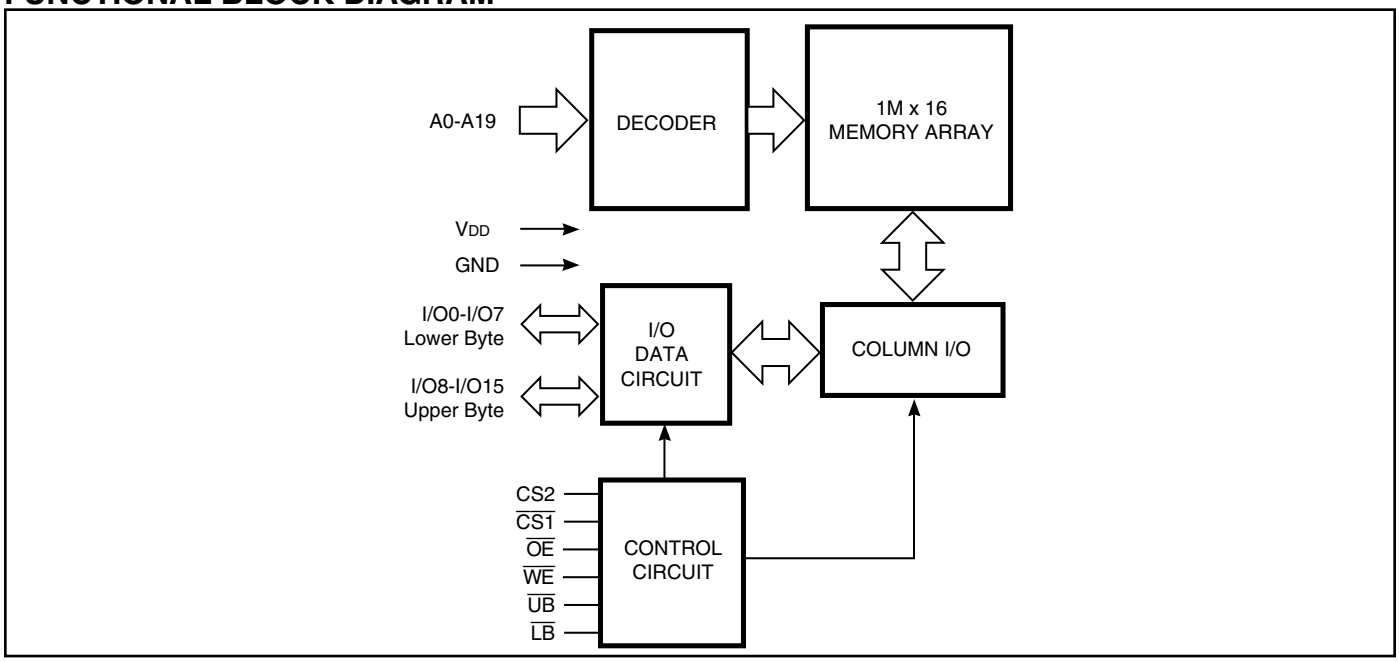
The *ISSI* IS66WV1M16DALL/DBLL is a high-speed, 16M bit static RAMs organized as 1Mb words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) or when $\overline{CS1}$ is LOW, CS2 is HIGH and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

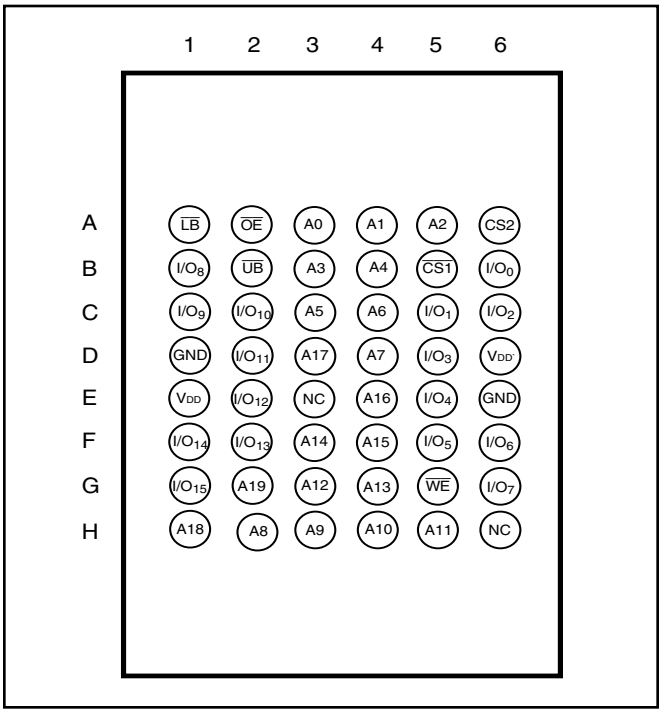
The IS66WV1M16DALL/DBLL is packaged in the JEDEC standard 48-ball mini BGA (6mm x 8mm). The device is also available for die sales.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS:

48-Ball mini BGA (6mm x 8mm)



Note:
TSOP package option is under evaluation.

PIN DESCRIPTIONS

A0-A19	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	H	L	H	L	High-Z	D_{OUT}	
	H	L	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	H	X	H	L	High-Z	D_{IN}	
	L	L	H	X	L	L	D_{IN}	D_{IN}	

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	(70ns)	(55ns)
Commercial	0°C to +70°C	1.7V - 1.95V, 2.5V - 3.6V	2.5V - 3.6V
Industrial	–40°C to +85°C	1.7V - 1.95V, 2.5V - 3.6V	2.5V - 3.6V
Automotive	–40°C to +105°C	2.5V-3.6V	

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.8	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.5V-3.6V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
V_{IL} (min.) = –2.0V AC (pulse width < 10ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.7V-1.95V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.7-1.95V	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.7-1.95V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.7-1.95V	1.4	V_{DD} + 0.2	V
V_{IL}	Input LOW Voltage		1.7-1.95V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
V_{IL} (min.) = –1.0V AC (pulse width < 10ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 1.0V AC (pulse width < 10ns). Not 100% tested.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	1.7V-1.95V (Unit)	2.5V-3.6V (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.7V - 1.95V	2.5V - 3.6V
R1(Ω)	3070	1029
R2(Ω)	3150	1728
V_{REF}	0.9V	1.4V
V_{TM}	1.8V	2.8V

AC TEST LOADS

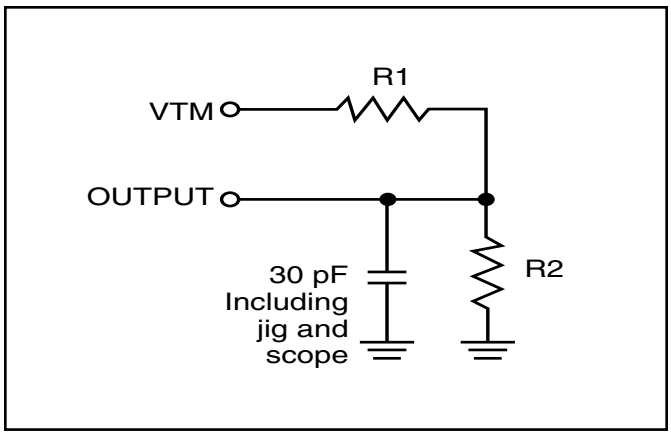


Figure 1

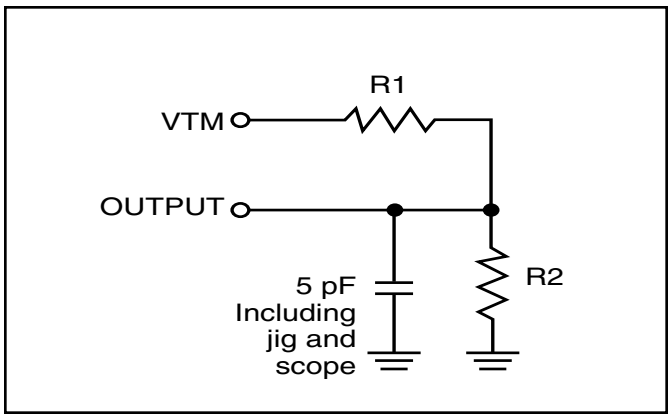


Figure 2

1.7V-1.95V POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} All Inputs 0.4V or V_{DD} – 0.2V	Com. Ind. Auto.	20 25 30	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD} – 0.2V CS2 = V_{DD} – 0.2V, f = 1MHz	Com. Ind. Auto.	4 4 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , CS2 = V_{IL}, f = 1 MHz	Com. Ind. Auto.	0.6 0.6 1	mA
	OR				
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind. Auto.	100 120 150	µA
	OR				
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2=V_{IH} V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V_{DD} – 0.2V			

Note:.
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2.5V-3.6V POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} All Inputs 0.4V or V_{DD} – 0.3V	Com. Ind. Auto. typ.(2)	25 28 35 15	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD} – 0.2V CS2 = V_{DD} – 0.2V, f = 1MHZ	Com. Ind. AUTO.	5 5 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , CS2 = V_{IL}, f = 1 MHz	Com. Ind. AUTO.	0.6 0.6 1	mA
	OR				
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind. Auto. typ.(2)	100 130 150 75	µA
	OR				
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2=V_{IH} V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V_{DD} – 0.2V			

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

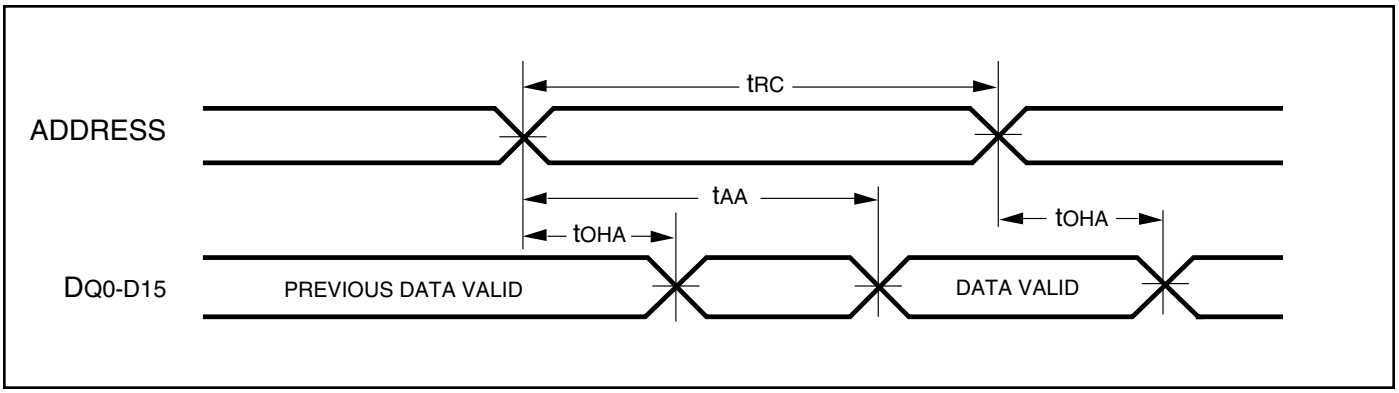
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	20	0	25	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.

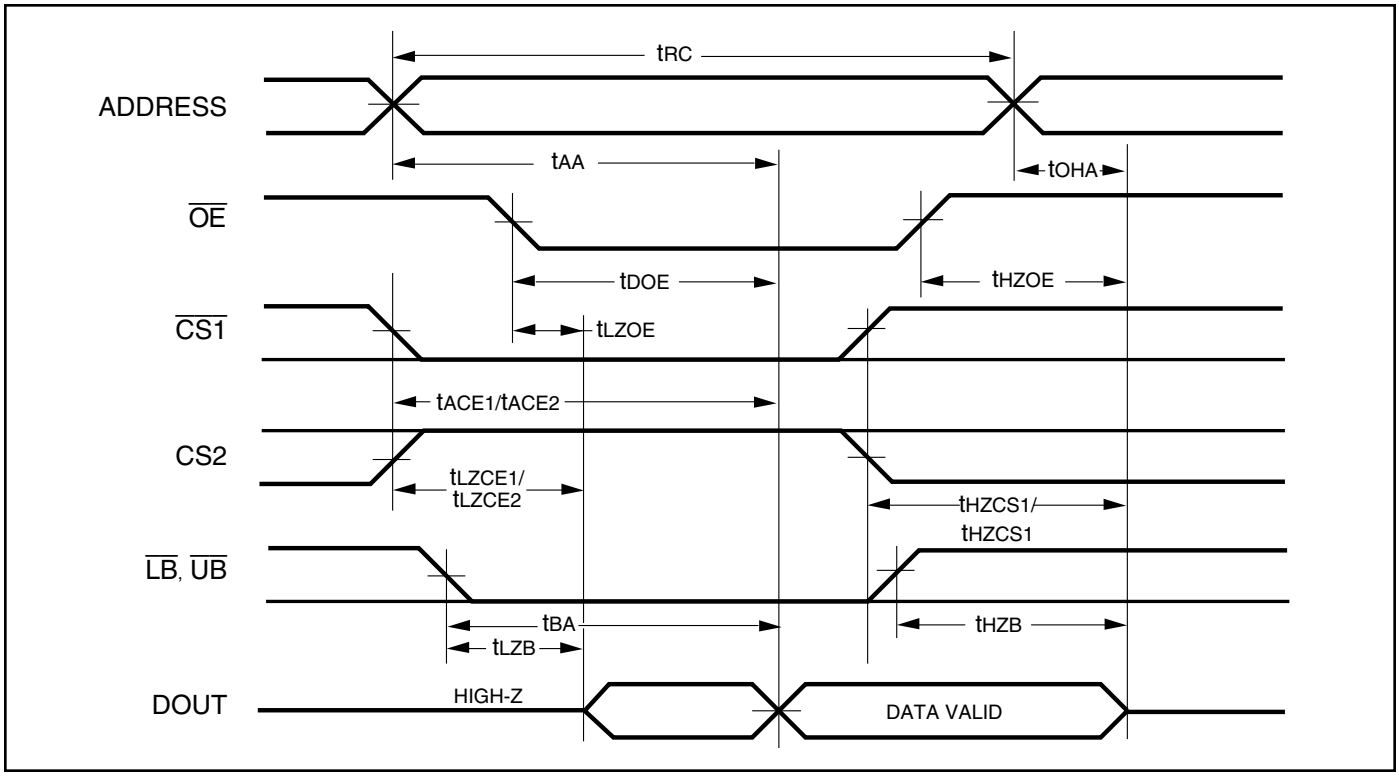
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

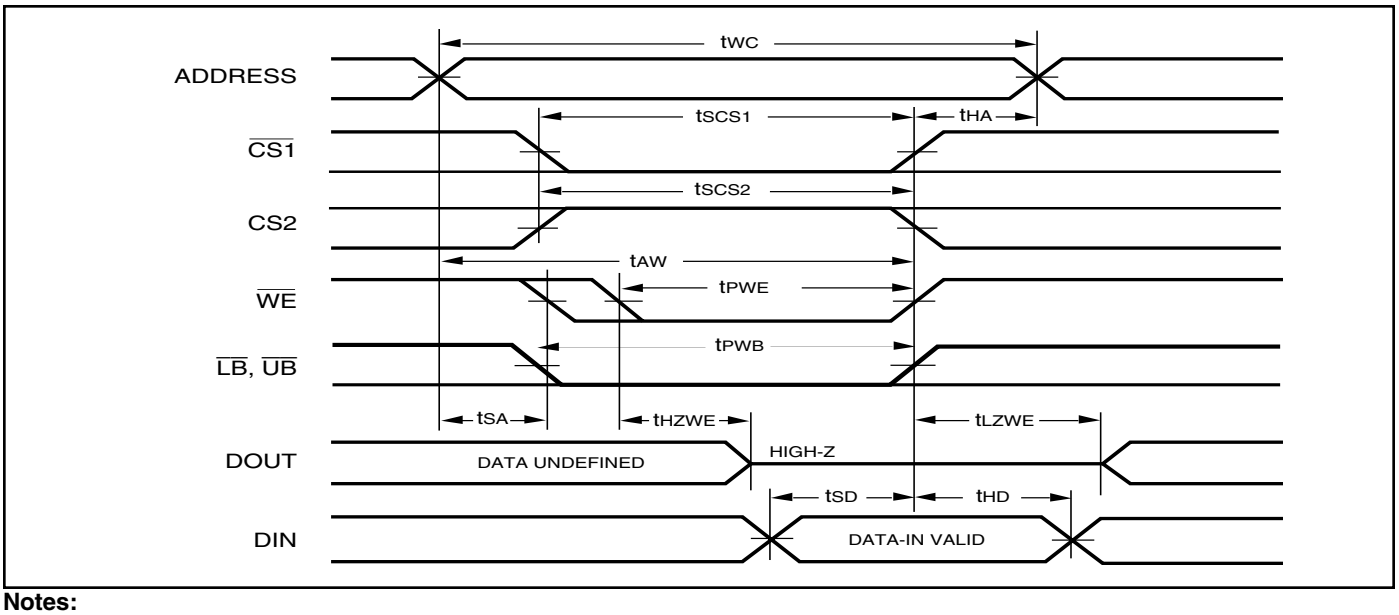
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	45	15,000	60	15,000	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	30	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HZWE} + t_{SD}$ when $\overline{OE}$ is LOW.

AC WAVEFORMS

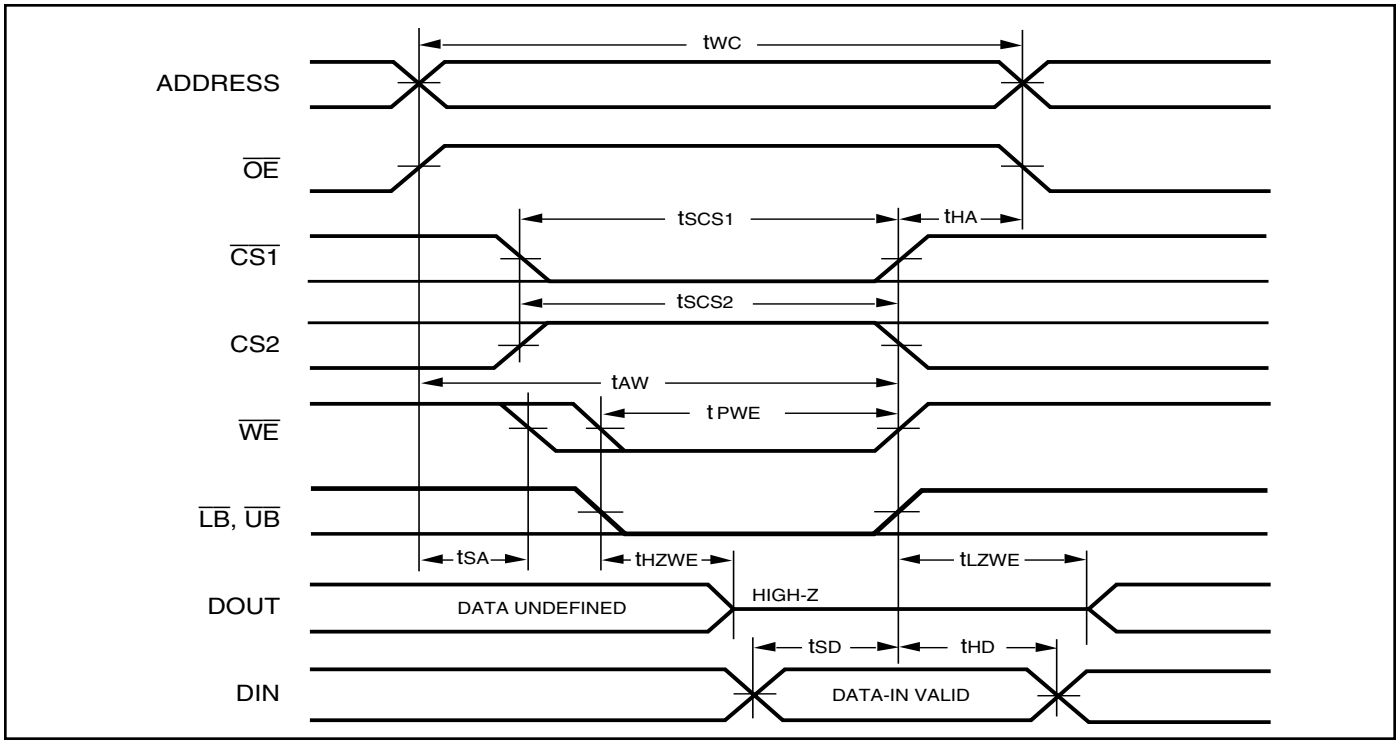
WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



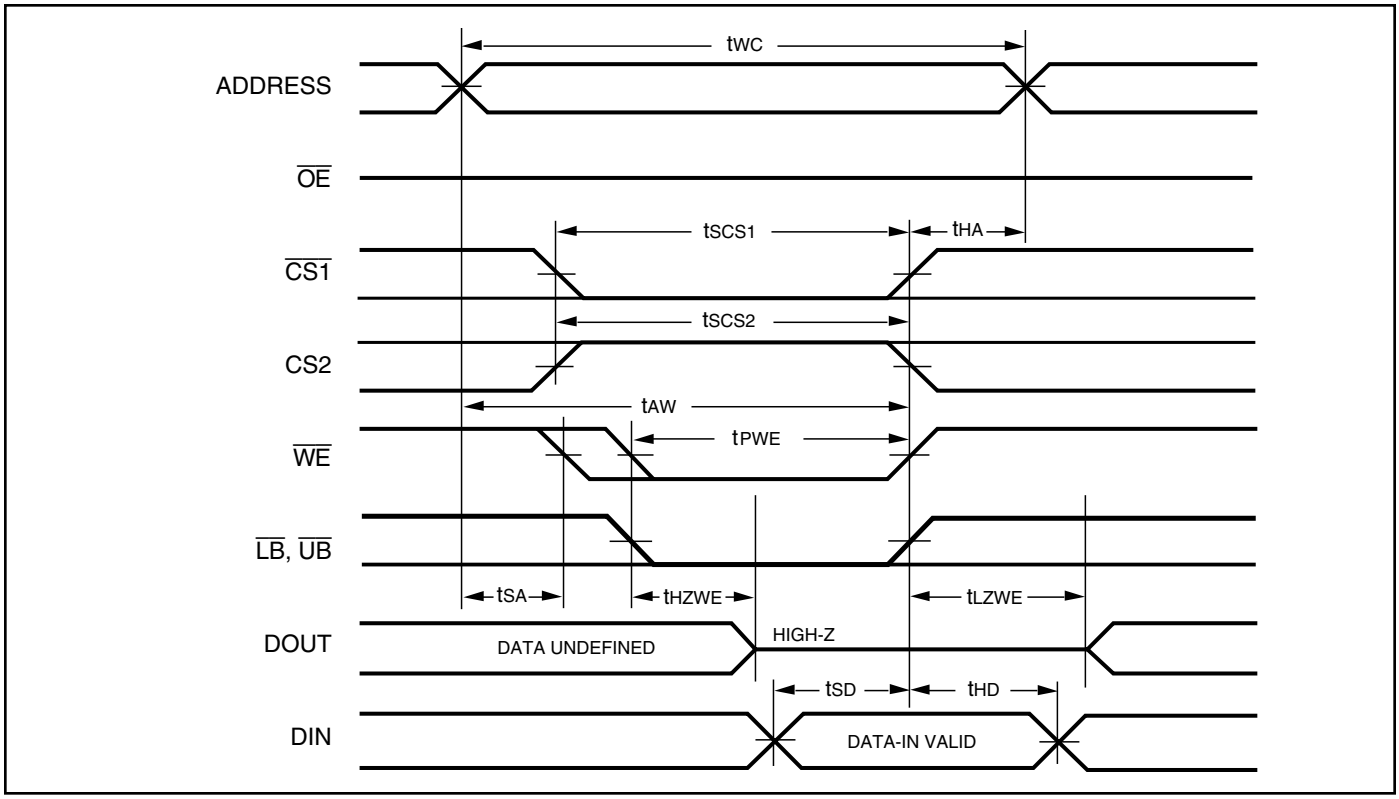
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS1}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)

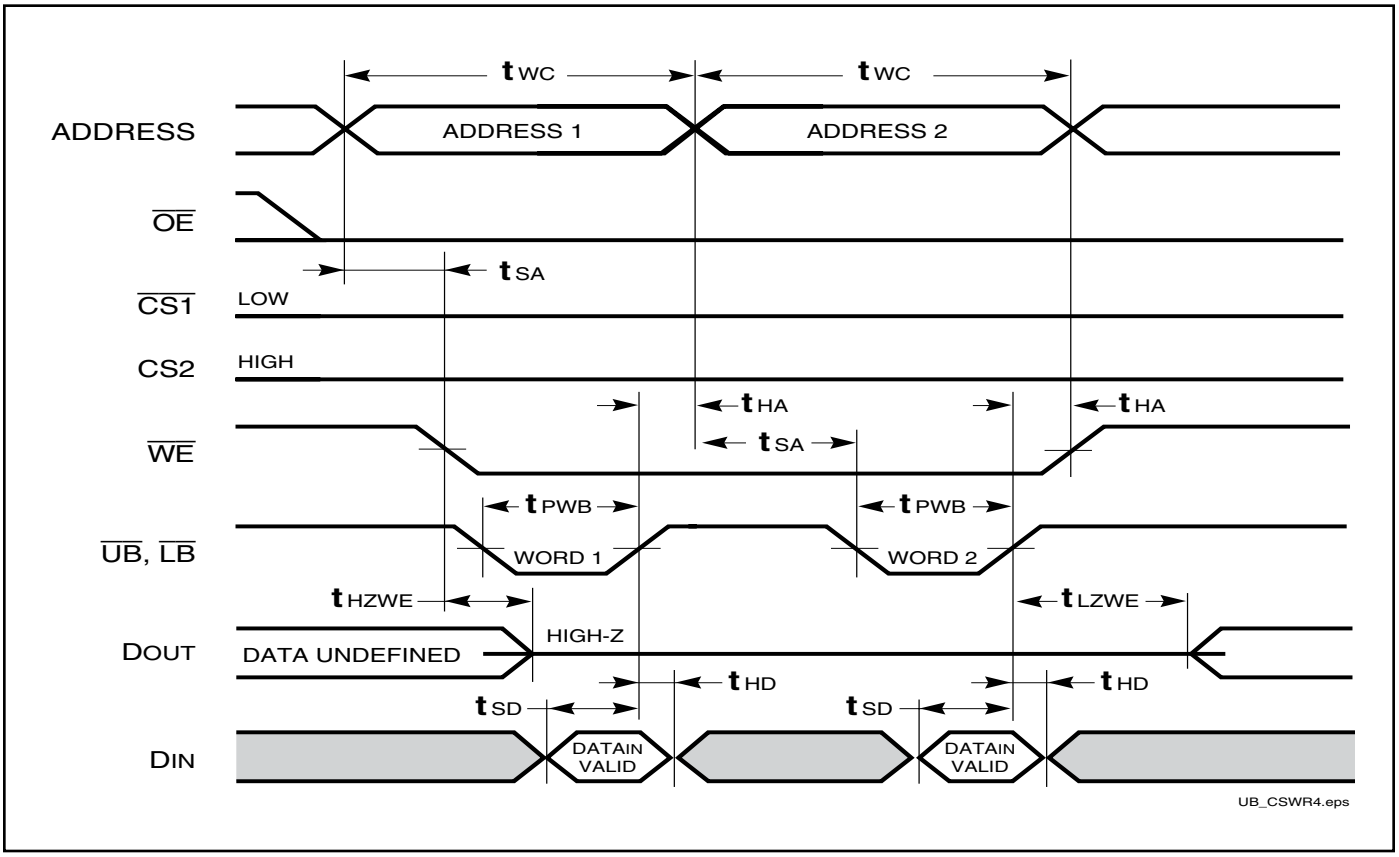


Figure 1: **Avoidable Timing**

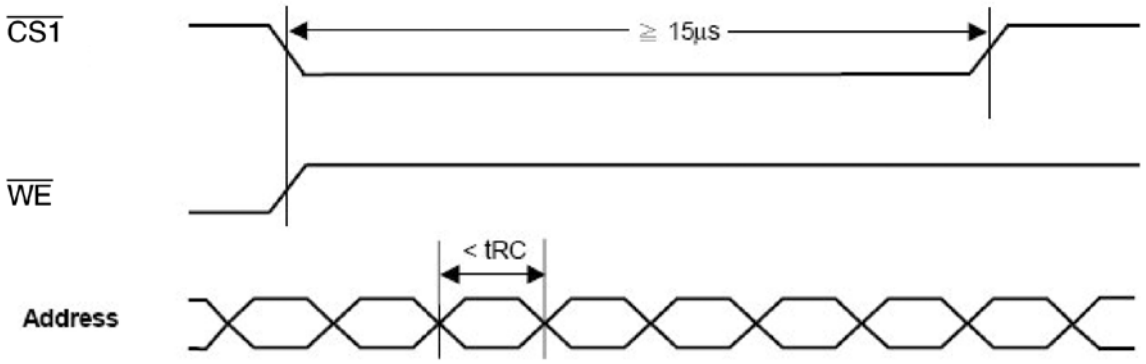


Figure 2:

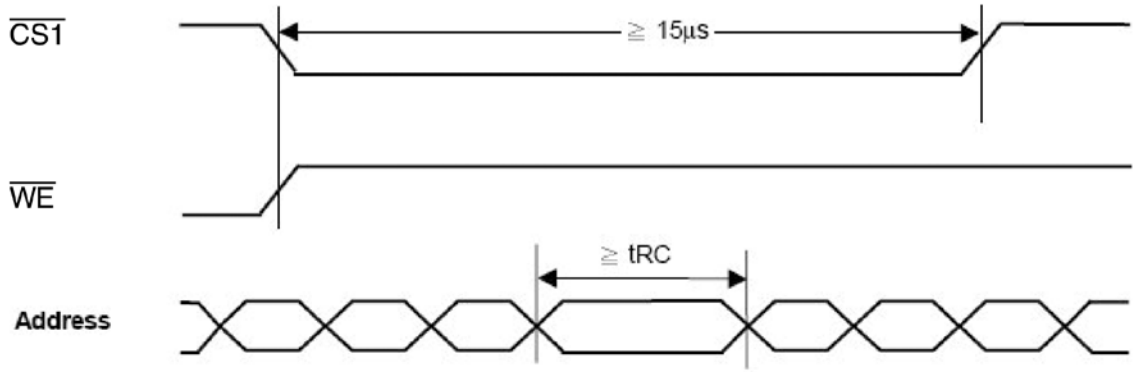
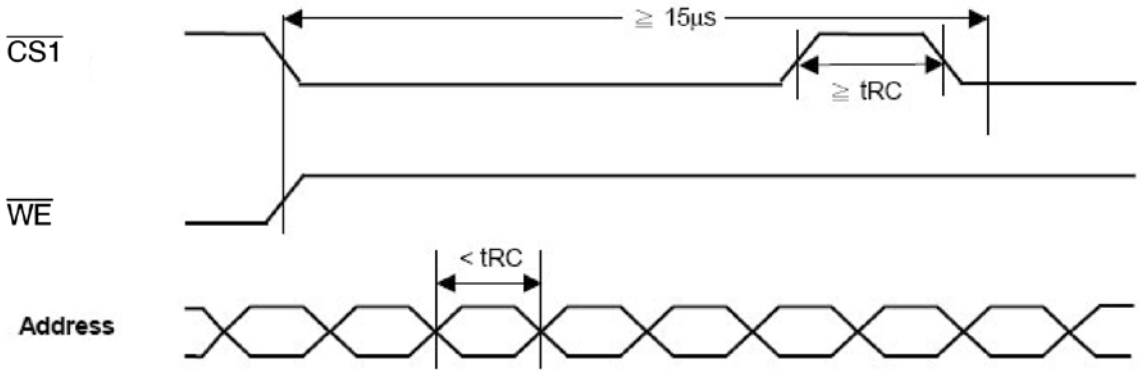


Figure 3:



Please avoid address change for less than t_{RC} during the cycle time longer than 15 µs (Figure 1). Figure 2 & 3 provide work around solution for this issue.

IS66WV1M16DALL

Industrial Range: -40°C to +85°C
Voltage Range: 1.7V to 1.95V

Speed (ns)	Order Part No.	Package
70	IS66WV1M16DALL-70BLI	mini BGA (6mm x 8mm), Lead-free

IS66WV1M16DBLL

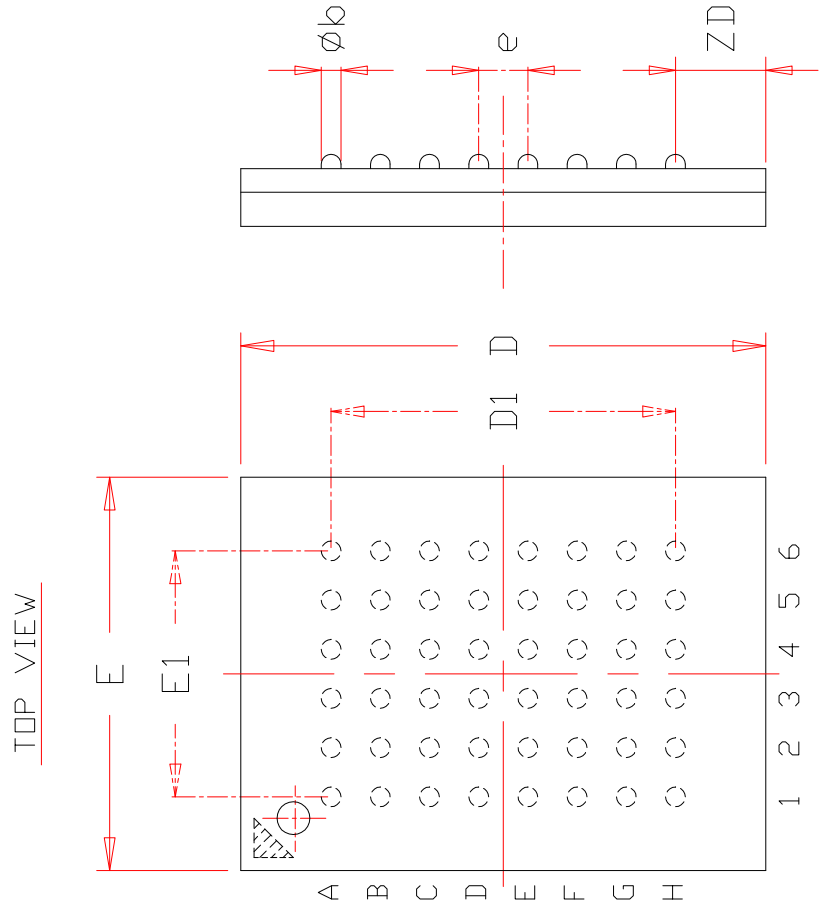
Industrial Range: -40°C to +85°C
Voltage Range: 2.5V to 3.6V

Speed (ns)	Order Part No.	Package
55	IS66WV1M16DBLL-55BLI	mini BGA (6mm x 8mm), Lead-free
70	IS66WV1M16DBLL-70BLI	mini BGA (6mm x 8mm), Lead-free

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC,			0.030 BSC,		
ZD	1.375 REF,			0.054 REF,		
ZE	1.125 REF,			0.044 REF,		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



ISSI	TITLE	48L 6x8mm TF-BGA Package Outline	REV.	C	DATE	08/12/2008