YAMAHA LSI

Preliminary
1995. 12. 8

YSS241

DPLD2

Dolby Pro Logic Decoder 2

■OUTLINE

The YSS241(DPLD2) is a Dolby Pro logic decoder LSI, offering high-quality sound processing by all digital sound processing. In addition, because digital delay memory and all other functions for Dolby Pro logic are included into the single chip, board space can be dramatically reduced.

■FEATURES

- Dolby Pro logic decoder block
  Automatic balance control, Steering logic, Center mode control, 30ms digital delay, Noise generator, Modified B-type noise reduction decoder
- Digital interface for audio signals with 2 channels for input and up to 5 channels for output.
- Direct interface with ITT Semiconductor's MSP3410 through digital interface.
- 2nd-order IIR filter for front 3 channels(L, R, C) to compensate speaker characteristics.
- Yamaha's original surround mode
  Enhanced mode that emphasizes dolby pro logic decoder function when sampling frequency is 32kHz.
  Pseudo-stereo effect for monaural sound source
  Front-wide effect for normal stereo sound source
- Control of parameter from external microprocessor is made through serial 3-line or I^2C bus interface.
- A sampling frequency(fs) can be selected from 32kHz, 44.1kHz or 48kHz.
- Master clock can be selected from 256fs or 18.432MHz (576*32kHz).
- 5V single power supply, Si-gate CMOS process.
- 64 pin QFP (YSS241-F) or 64 pin shrink DIP (YSS241-K).

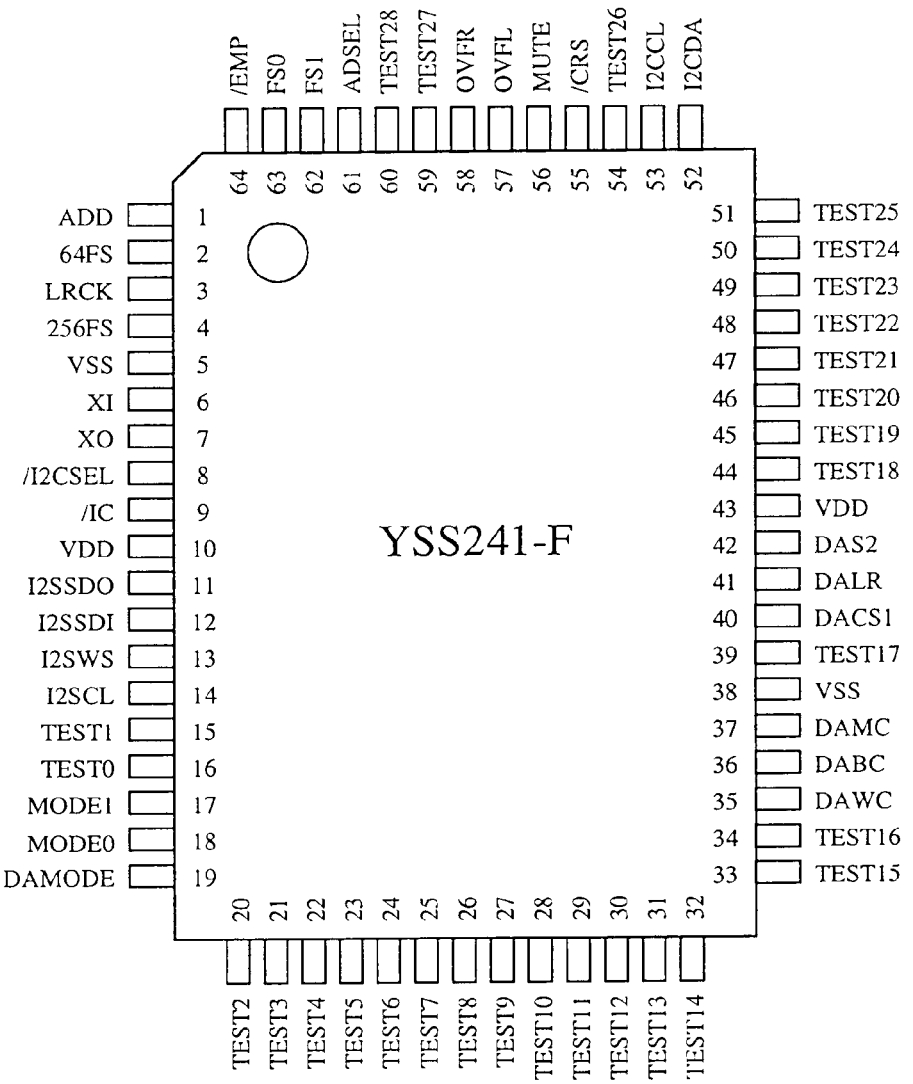
NOTE1) "Dolby Pro Logic" is a trademark of Dolby Laboratories Licensing Corporation. This LSI is available only to licensees of Dolby Laboratories Licensing Corp.

NOTE2) Purchase of I^2C components of YAMAHA Corporation conveys a license under the Philips I^2C patent rights to use these components in an I^2C system, provided that the system conforms to the I^2C standard specification as defined by Philips.

The contents of this catalog are target specifications and are subject to change without prior notice. When using this device, please recheck the specifications.

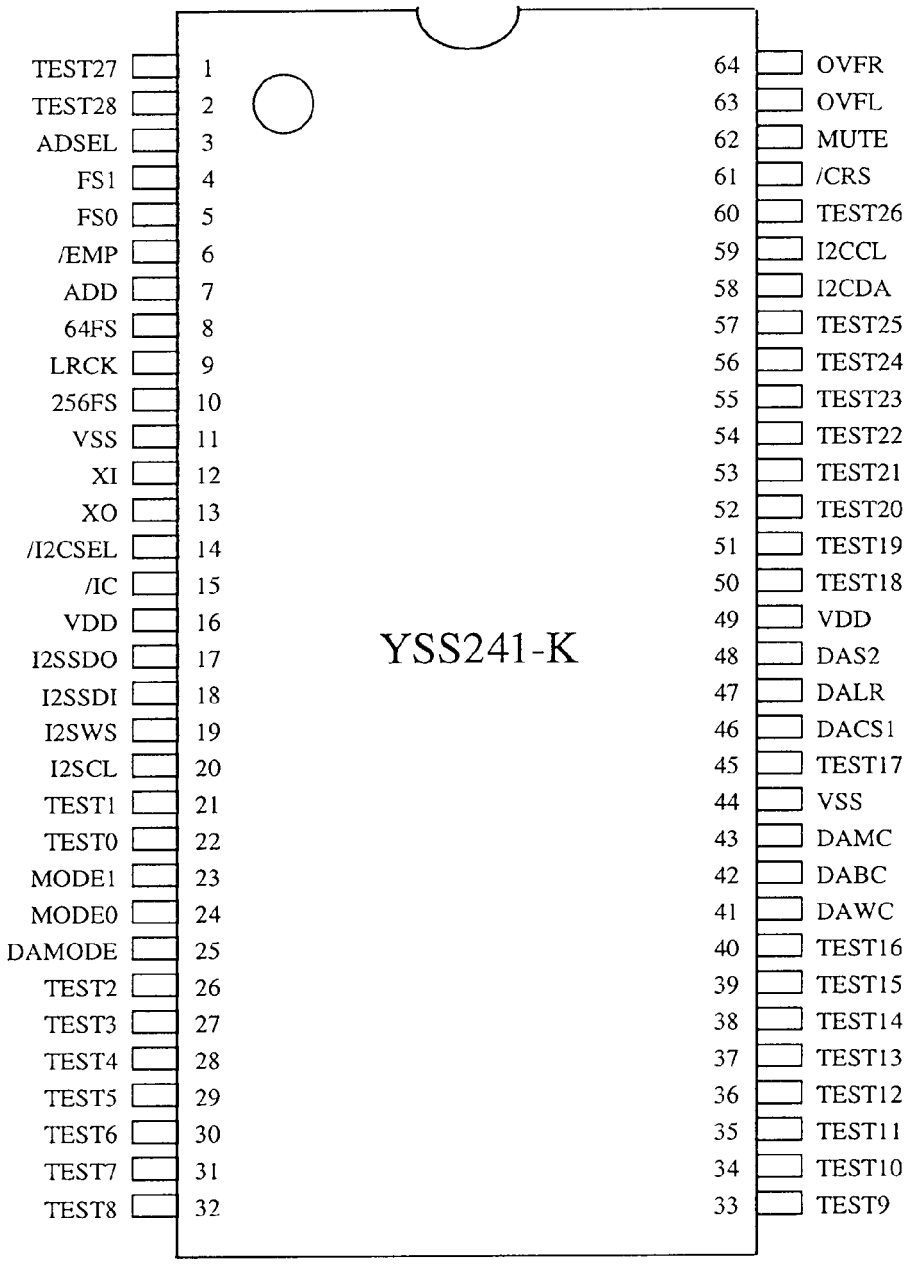
■PIN CONFIGURATION

1) 64pin QFP



<64pin QFP Top View>

2) 64pin SDIP



<64pin SDIP Top View>

■PIN DESCRIPTION

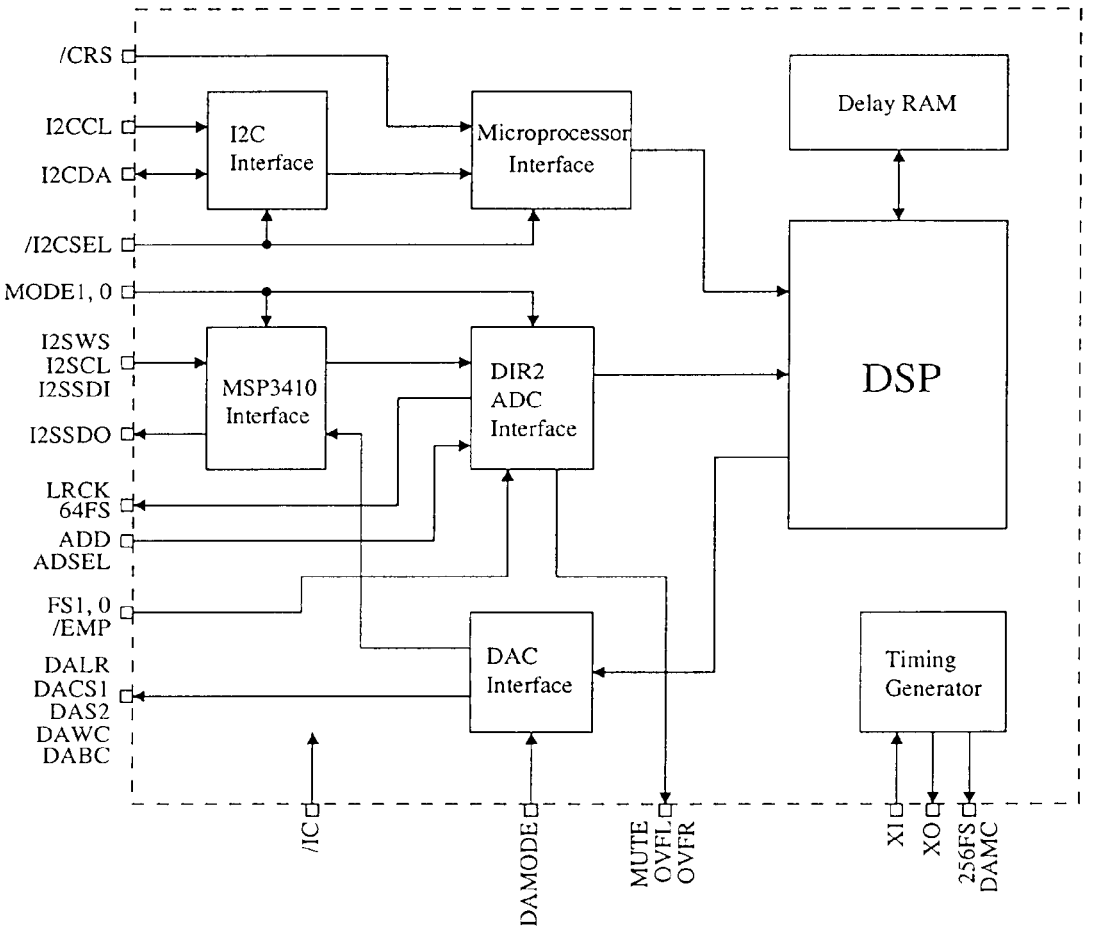
No.		Name	I/O	Function	
QFP	SDIP			Format 4	Format 1, 2, 3
1	7	ADD	I	A/D converter audio data input	Connect with VDD or VSS
2	8	64FS	O	Bit clock output for A/D converter	
3	9	LRCK	O	L/R clock output for A/D converter	
4	10	256FS	O	Master clock output for A/D converter	
5	11	VSS	-	Ground	
6	12	XI	I	Connecting crystal oscillator or input external clock	
7	13	XO	O	Connecting crystal oscillator	
8	14	/I2CSEL	I	Selecting CPU interface ("H" : Serial 3-line system, "L" : I^2C bus system)	
9	15	/IC	Is	Initial clear input	
10	16	VDD	-	+5V power supply	
11	17	I2SSDO	O	No meaning	Serial data output to MSP3410 (*1)
12	18	I2SSDI	I	Audio data input from DIR2	Serial data input from MSP3410
13	19	I2SWS	I	L/R clock input from DIR2	L/R clock input from MSP3410
14	20	I2SCL	Is	Connect with VDD or VSS	Bit clock input from MSP3410
15	21	TEST1	I+	LSI test terminal (To be open in use)	
16	22	TEST0	I+	LSI test terminal (To be open in use)	
17	23	MODE1	I	Selecting audio data input mode	
18	24	MODE0	I	Selecting audio data input mode	
19	25	DAMODE	I+	Selecting audio data output format	
20	26	TEST2	I+	LSI test terminal (To be open in use)	
21	27	TEST3	I+	LSI test terminal (To be open in use)	
22	28	TEST4	I+	LSI test terminal (To be open in use)	
23	29	TEST5	I+	LSI test terminal (To be open in use)	
24	30	TEST6	I+	LSI test terminal (To be open in use)	
25	31	TEST7	I+	LSI test terminal (To be open in use)	
26	32	TEST8	I+	LSI test terminal (To be open in use)	
27	33	TEST9	I+	LSI test terminal (To be open in use)	
28	34	TEST10	I+	LSI test terminal (To be open in use)	
29	35	TEST11	I+	LSI test terminal (To be open in use)	
30	36	TEST12	I+	LSI test terminal (To be open in use)	
31	37	TEST13	I+	LSI test terminal (To be open in use)	
32	38	TEST14	I+	LSI test terminal (To be open in use)	
33	39	TEST15	I+	LSI test terminal (To be open in use)	
34	40	TEST16	I+	LSI test terminal (To be open in use)	
35	41	DAWC	O	L/R clock output for D/A converter	
36	42	DABC	O	Bit clock output for D/A converter	
37	43	DAMC	O	Master clock output for D/A converter	
38	44	VSS	-	Ground	
39	45	TEST17	I+	LSI test terminal (To be open in use)	
40	46	DACS1	O	Audio data output for D/A converter	
41	47	DALR	O	Audio data output for D/A converter	
42	48	DAS2	O	Audio data output for D/A converter	
43	49	VDD	-	+5V power supply	
44	50	TEST18	O	LSI test terminal (To be open in use)	
45	51	TEST19	O	LSI test terminal (To be open in use)	
46	52	TEST20	I+	LSI test terminal (To be open in use)	
47	53	TEST21	O	LSI test terminal (To be open in use)	
48	54	TEST22	I+	LSI test terminal (To be open in use)	

(*1) When format 3 is used, I2SSDO terminal is no meaning.

No.		Name	I/O	Function
QFP	SDIP			
49	55	TEST23	I+	LSI test terminal (To be open in use)
50	56	TEST24	I+	LSI test terminal (To be open in use)
51	57	TEST25	I+	LSI test terminal (To be open in use)
52	58	I2CDA	Is/OD	CPU/I^{2}C bus interface serial data input
53	59	I2CCL	Is	CPU/I^{2}C bus interface bit clock input
54	60	TEST26	O	LSI test terminal (To be open in use)
55	61	/CRS	I	Serial 3-line system (/I2CSEL = "H") : CPU interface reset signal input I^{2}C bus system (/I2CSEL = "L") : Connect with VDD.
56	62	MUTE	O	Detection of system mute
57	63	OVFL	O	Detection of overflow of audio data input (L channel)
58	64	OVFR	O	Detection of overflow of audio data input (R channel)
59	1	TEST27	O	LSI test terminal (To be open in use)
60	2	TEST28	O	LSI test terminal (To be open in use)
61	3	ADSEL	Is	Audio data input switching terminal ("H" : ADD , "L" : I2SSDI)
62	4	FS1	Is	Sampling frequency switching terminal (Effect only when ADSEL = "L")
63	5	FS0	Is	Sampling frequency switching terminal (Effect only when ADSEL = "L")
64	6	/EMP	Is	De-emphasis control input ("L" : ON)

Note) I+ ; Input terminal with pull-up resistor, Is ; Schmidt terminal, OD ; Open drain output terminal

■BLOCK DIAGRAM



■FUNCTION DESCRIPTION

1. Clock signals **XI, XO**

XI and XO terminals are used to make a crystal oscillator circuit. The oscillation frequency of clock signal can be selected from 256fs or 18.432 MHz (576 * 32kHz). Clock signal generated by an external source can be input to XI terminal.

2. Inputting/outputting digital audio signals **MODE1, MODE0, DAMODE, ADSEL, I2SCL, I2SWS, I2SSDI, I2SSDO, ADD, LRCK, 64FS, 256FS, DAWC, DABC, DALR, DACS1, DAS2, DAMC**

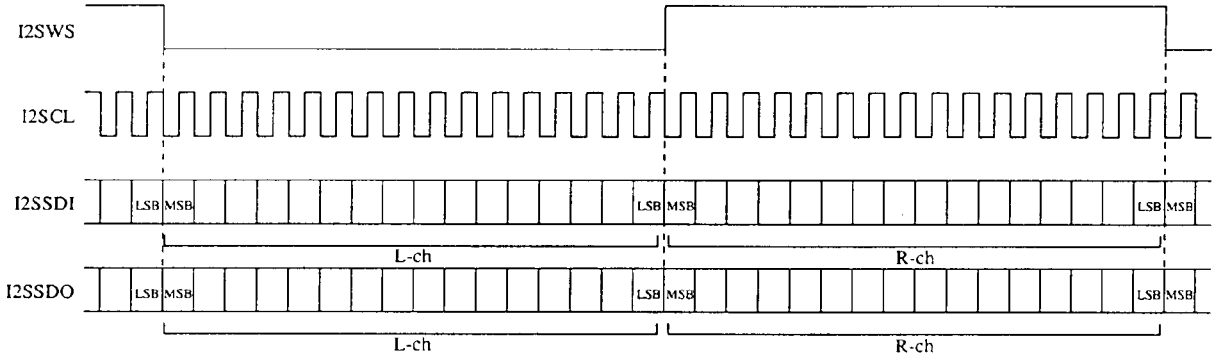
MODE1	MODE0	Type	XI clock input
L	L	Format 1	18.432MHz (576*32kHz)
L	H	Format 2	18.432MHz (576*32kHz)
H	L	Format 3	256fs
H	H	Format 4	256fs

ADSEL terminal is used to switch audio data that are input. When other than format 4, use with ADSEL = "L".
ADSEL = "L" : Inputting through I2SSDI terminal becomes effective.
ADSEL = "H" : Inputting through ADD terminal becomes effective.

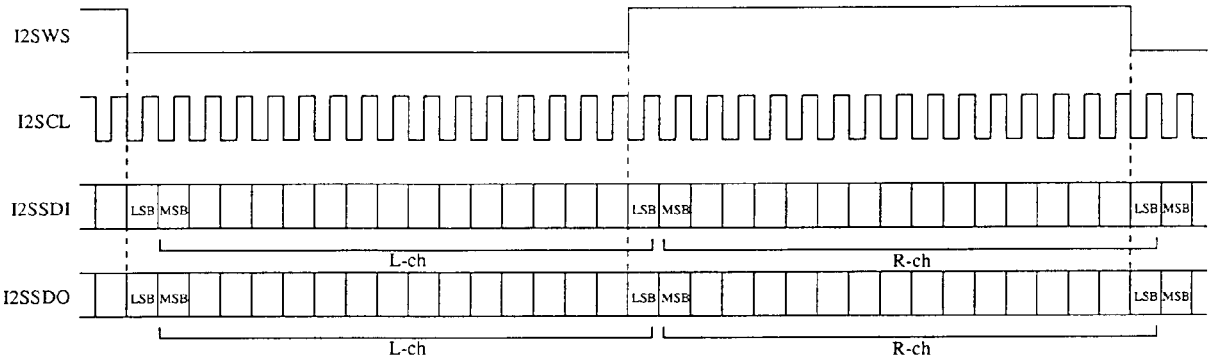
2-1. MSP3410 interface

When connecting this LSI to MSP3410, I2SCL, I2SWS, I2SSDI and I2SSDO terminals are used as described below in each format. Data output from DALR terminal is the same as the one output from I2SSDO.

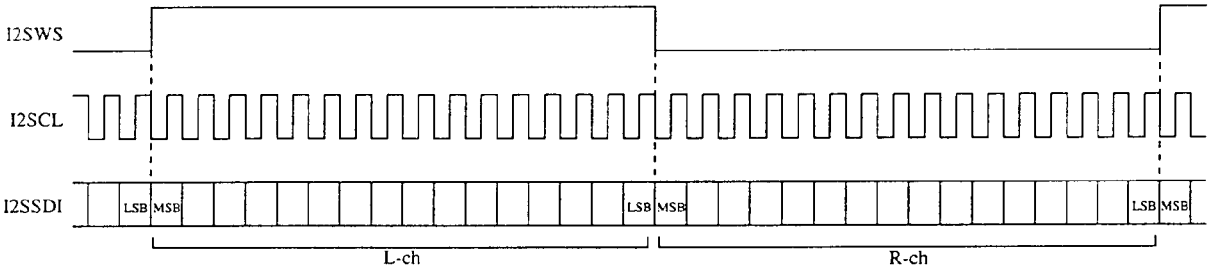
● Format 1 (MODE1, MODE0) = (L, L)



● Format 2 (MODE1, MODE0) = (L, H)

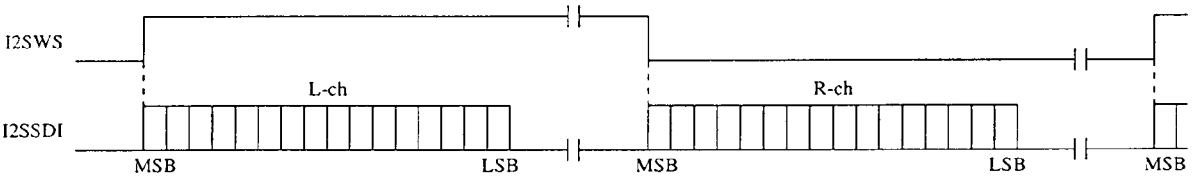


2-2. Format 3 (MODE1, MODE0) = (H, L)



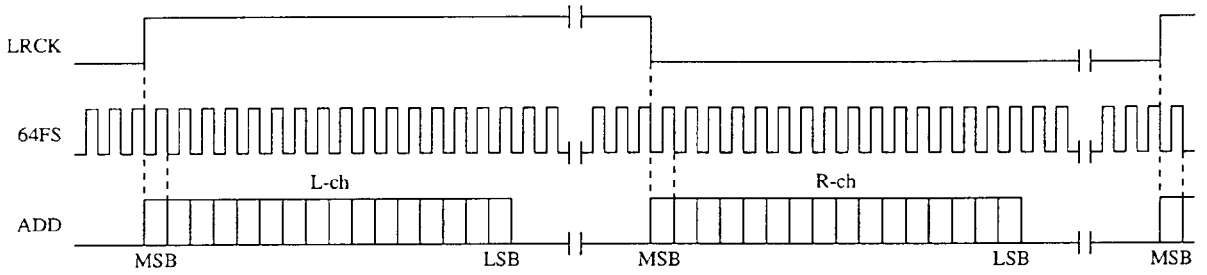
2-3. Format 4 (MODE1, MODE0) = (H, H)

When connecting this LSI to YM3436D(DIR2), the signals are input through I2SWS and I2SSDI terminals using the following format.



The clock output from YM3436D(DIR2) must be used as the one to be input to XI terminal. I2SCL terminal must be connected to VDD or VSS. This mode does not assume connection of this LSI with other than YM3436D(DIR2). Both DOM1 and DOM0 terminals of YM3436D(DIR2) must be set to "L".

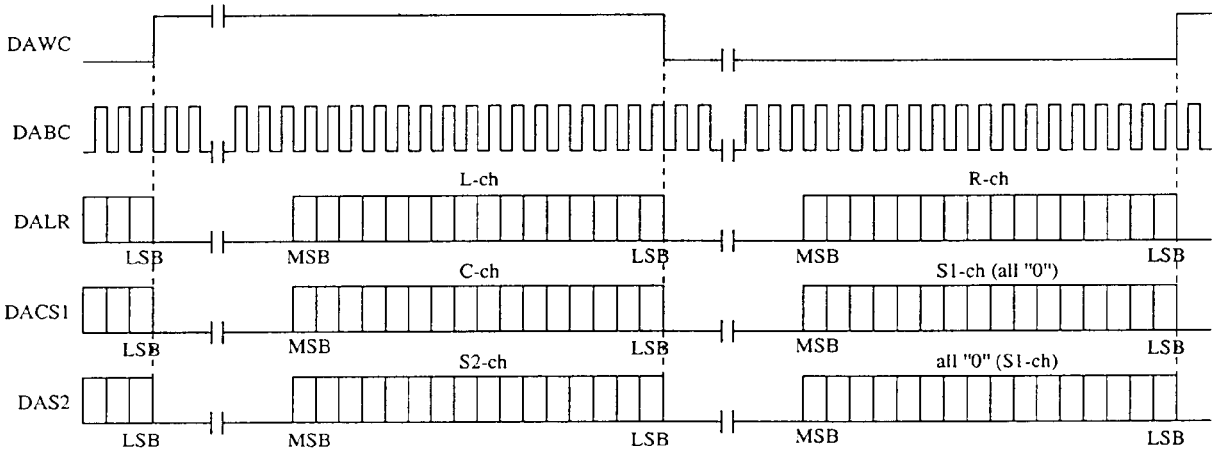
When this LSI is connected to A/D converter, the signals are input through 64FS, LRCK and ADD terminals using the following format. When input of master clock to A/D converter is needed, use the clock that is output from 256FS terminal.



A/D converter and YM3436D(DIR2) can be connected to this LSI at the same time, but A/D converter and MSP3410 cannot be connected to it at the same time.

2-4. Outputting digital audio signals

When connecting this LSI to D/A converter, the signals are output through DAWC, DABC, DACS1, DALR and DAS2 terminals using the following format. When MSP3410 is used (MODE1 = "L"), Data output from I2SSDO terminal is the same as the one output from DALR.



When input of master clock to D/A converter is needed, use clock that is output from DAMC terminal. Frequency of clock that is output from DAMC terminal depends on the state of MODE1 terminal as described below.
D/A converter output can select the combination of center channel (C-ch) and surround channel (S1, S2-ch) by using DAMODE terminal. (In above parenthesize when DAMODE = "L".)

MODE1	DAMC
L	384fs
H	256fs

DAMODE	DALR	DACS1	DAS2
L	L, R	C	S2, S1
H (no connect)	L, R	C, S1	S2

3. Status information **FS1, FS0, /EMP**

FS1 and FS0 terminals are used to specify a sampling frequency. This function is valid only when ADSEL = "L".

FS1	FS0	Sampling frequency
L	L	44.1kHz
L	H	48kHz
H	L	Do not set.
H	H	32kHz

When YM3436D(DIR2) is used, the FS1 and FS0 terminals of this LSI can be connected directly to FS1 and FS0 terminals of YM3436D respectively.

/EMP terminal is used to control de-emphasis.

/EMP	
L	De-emphasis is turned on.
H	De-emphasis is turned off.

4. CPU interface **/I2CSEL, I2CCL, I2CDA, /CRS**

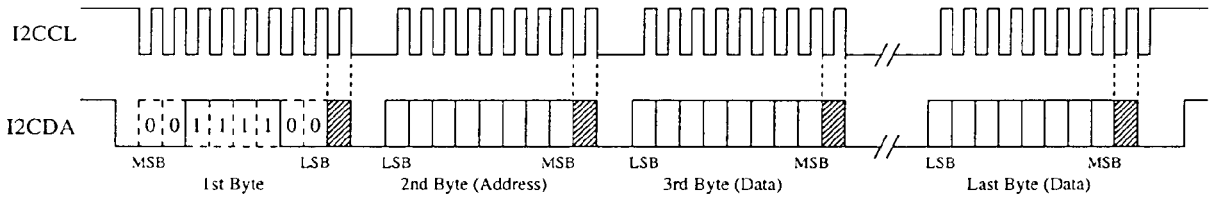
For this YSS241(DPLD2), I^2C bus interface or 3-line serial interface can be used as a CPU interface.

/I2CSEL	CPU interface
L	I^2C bus interface
H	3-line serial interface

4-1. I^2C bus interface (/I2CSEL = "L")

● I^2C bus format signal

Transfer register data from I^2C bus using the following format.



Every time each of the above bytes has been transferred, an acknowledge signal (ACK : slant line) "L" is output. When I^2C bus is used, /CRS terminal must be connected to VDD.

● First byte

MSB	B6	B5	B4	B3	B2	B1	LSB
0	0	1	1	1	1	0	0

This byte indicates slave address that is given specifically for YSS241(DPLD2)

● 2Nth (even-numbered) byte

MSB	B6	B5	B4	B3	B2	B1	LSB
Register address							

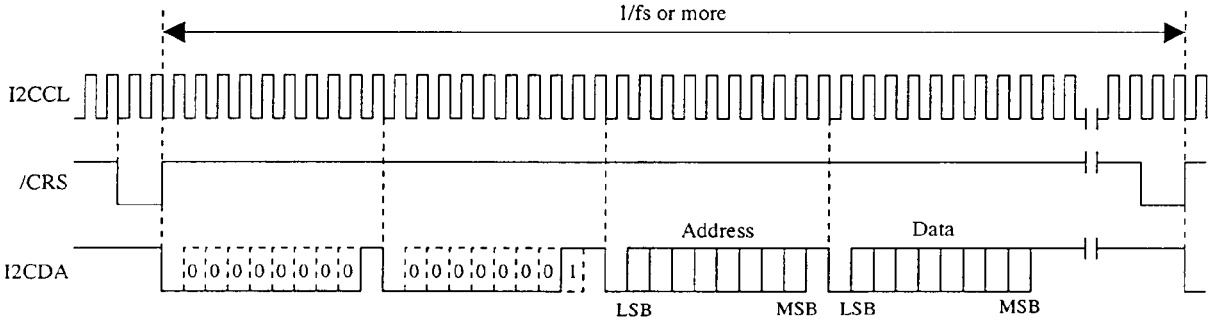
● 2N+1th (odd-numbered) byte

MSB	B6	B5	B4	B3	B2	B1	LSB
Register data							

Note) For the second and after bytes, even-numbered bytes must be used to specify register addresses of YSS241(DPLD2) and odd-numbered bytes to specify register data.

4-2. 3-line serial interface (/I2CSEL = "H")

Register address and data are set using the following format. A register data is set using 4 bytes. /CRS terminal is a reset input terminal of CPU interface. /CRS terminal must be set to "L" every time a register data has been set.



5. Outputting State of Audio Signals **MUTE, OVFL, OVFR**

Terminal	Function
MUTE	"H" : Indicates muting by register, initial clear or change of state of YM3436D(DIR2).
OVFL	"H" : Indicates that L-ch input overflows. (note)
OVFR	"H" : Indicates that R-ch input overflows. (note)

note) Detecting input level of -0.5dB or more for 0dB (maximum input level) is regarded as "overflow".

6. Initial Clear /IC

This LSI requires initial clear when turning on the power. The /IC terminal should be set to "L" at 1 μ s or more.

7. LSI test terminals **TEST0～TEST28**

These terminals are for testing this LSI. They must be open in normal use.

■CONTROL OF REGISTERS

1. Register map

Address(HEX)	Acronym	Name of register
00	SCR	SYSTEM CONTROL REGISTER
01	LCR	LOAD CONTROL REGISTER
02	ADR	ADDRESS REGISTER
03	PGR	PAGE REGISTER
04	LDR	DATA L REGISTER
05	HDR	DATA H REGISTER
06	DCR	DOLBY CONTROL REGISTER
07	SGR	STEERING GAIN REGISTER
F0, F1, F2	TR	TEST REGISTER (Data writing prohibited)

2. Registers

● SYSTEM CONTROL REGISTER (SCR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
00	IC	MUTE	SYNC ENABLE	FS0	FS1	FAST RAM CLEAR	1	MUTE CLEAR ENABLE

Set "1" on B6.

Name	Functions
IC	"1" : Initial clear (/IC sets this bit to "1".)
MUTE	"1" : Clear of accumulator (/IC sets this bit to "1".)
SYNC ENABLE	"0" : Internal DSP counter operates independent from the state of I2SWS. "1" : Internal DSP counter starts synchronizing with I2SWS. (/IC sets this bit to "0".)
FS0, FS1	FS0 = 0, FS1 = 0 : 44.1kHz FS0 = 1, FS1 = 0 : 48kHz FS0 = 1, FS1 = 1 : 32kHz This bit is valid only when ADSEL = "H". (/IC sets these bits to "0".)
FAST RAM CLEAR	"1" : Fast clearing of Delay RAM (/IC sets this bit to "0".)
MUTE CLEAR ENABLE	The rise from "0" to "1" avoids the state of mute. (/IC sets this bit to "0".)

● LOAD CONTROL REGISTER (LCR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
01	LCR0	LCR1	AUTI	*	*	*	*	*

Do not care about bits MSB to B3.

Name	Function
LCR0	"1" : After data have been written into LDR, the data in HDR and LDR become valid.
LCR1	"1" : After data have been written into HDR, the data in HDR and LDR become valid.
AUTI	"1" : Auto-increment of address register is turned on.

When "1" is set on both LCR0 and LCR1, data in HDR and LDR become valid at the moment data is written into either HDR or LDR.

● ADDRESS REGISTER (ADR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
02	ADR0	ADR1	ADR2	ADR3	ADR4	ADR5	*	*

Do not care about bits MSB and B6.

○ ADR5 to ADR0 : These bits specify address pointer of data register selected by PGR (Page Register).

● PAGE REGISTER (PGR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
03	PAG0	PAG1	PAG2	DPLD/DSP	*	*	*	*

DPLD/DSP	PAG2	PAG1	PAG0	Acronym	Content of data register
0	0	*	*	TEST	Do not use this in normal operation.
0	1	1	0	RAMAD	RAM address register
0	1	1	1	COE	DSP coefficient register
1	*	*	*	DPLDC	Coefficient register for Dolby Pro Logic Decoder

Do not care about "*".

Data in LDR and HDR are written into data registers RAMAD, COE and DPLDC.

Data	LDR								HDR							
Register	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
RAMAD	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	"0"	"0"	"0"	"0"	"0"
COE	C0	C1	C2	C3	C4	C5	C6	C7								
DPLDC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15

○ Data Register

This LSI has three types of data registers, RAMAD, COE and DPLDC, as described below.

- RAMAD

This data register specifies reading and writing pointers of RAM for delaying in sound field simulation. The configuration of this register is 32 words x 11 bits, and 000H to 5FFH can be used. For reading pointer to which two memory pointers are assigned, set the same value on the two memory pointers. Delay time is calculated by using the following formula;
Delay time (seconds) = (Reading pointer - Writing pointer) x (1/fs),
where fs is a sampling frequency.

Numbers of delay taps in sound field simulation (See "4. Sound Field Simulation".) correspond to RAMAD00 to 1F respectively. It is not necessary to set data to memory addresses (0DH, 0EH, 0FH and 1FH) which are not shown in the sound field simulation.

- COE

Coefficients for sound field simulation is set on this data register. Its configuration is 64 words x 8 bits. The coefficient is calculated using the following formula.

$$COE = (-1) \times C_7 + \sum_{N=0}^{6} C_N \times 2^{N-7}$$

Numbers of coefficients in sound field simulation correspond to COE00 to 3F respectively. "7FH" is set to following coefficient registers with the addresses that are not shown in the sound field simulation.

09H, 0AH, 0BH, 0CH, 0DH, 1BH, 20H, 2AH, 2BH, 2CH

It is not necessary to set coefficient on coefficient address 38H.

- DPLDC

Coefficient data for Dolby Pro Logic Decoder is set on this data register. Its configuration is 59 words x 16 bits. The coefficient is calculated using the following formula.

$$DPLDC = (-1) \times D_{15} + \sum_{N=0}^{14} D_N \times 2^{N-15}$$

00 to 3A of signal flow correspond to DPLDC 00 to 3A respectively.

● DATA L REGISTER (LDR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
04	LDR0	LDR1	LDR2	LDR3	LDR4	LDR5	LDR6	LDR7

○ Lower 8 bit data of data register is written into this register.

● DATA H REGISTER (HDR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
05	HDR0	HDR1	HDR2	HDR3	HDR4	HDR5	HDR6	HDR7

○ Upper 8 bit data of data register is written into this register.

● DOLBY CONTROL REGISTER (DCR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
06	STEERING OFF	SURROUND STEERING OFF	MMIX ON	INPUT BALANCE OFF	1	N.R. OFF	INPUT MUTE	*

Do not care about MSB. Set "1" on B4.

Name	Function
STEERING OFF	"1" : Adaptive matrix circuit is turned off. "0" : Adaptive matrix circuit is turned on.
SURROUND STEERING OFF	"1" : Surround channel steering is turned off. "0" : Surround channel steering is turned on.
MMIX ON	"1" : LR audio synthesizing circuit of Combining Network is microprocessor controlled. Volume synthesizing ratio is set through DPLDC00 to 07. "0" : LR audio synthesizing circuit of Combining Network is controlled by adaptive matrix circuit.
INPUT BALANCE OFF	"1" : Auto input balance circuit is turned off. "0" : Auto input balance circuit is turned on. This bit is valid only when STEERING OFF = "0".
N.R. OFF	"1" : A variety of B type noise reduction is turned off. "0" : A variety of B type noise reduction is turned on.
INPUT MUTE	"1" : Input audio data is fixed to "0".

(/IC sets all bits of DCR to "0".)

● STEERING GAIN REGISTER (SGR)

ADDR	LSB	B1	B2	B3	B4	B5	B6	MSB
07	SG0	SG1	SG2	SG3	SG4	SG5	SG6	STEERING GAIN MODE

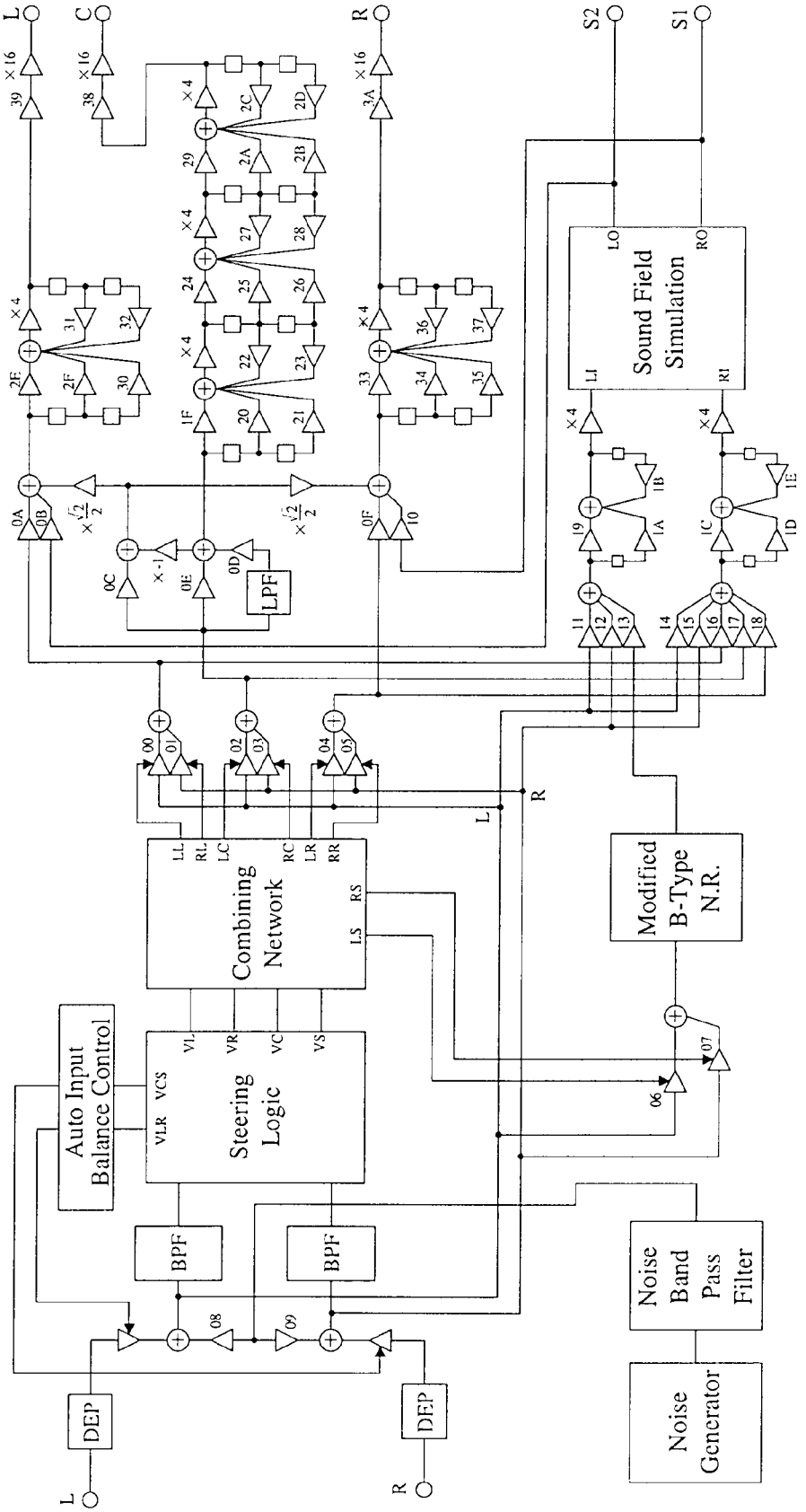
Name	Function
SG0～6	Sets steering gain. Increasing steering gain from 0 to 127 spoils steering gradually.
STEERING GAIN MODE	"1" : Operation of this LSI in this mode is similar to that of analog circuit. It is recommended to set steering gain in the range between 15 and 20 inclusive. "0" : In this mode, this LSI shows good corner separation.

(/IC sets all bits of SGR to "0".)

● TEST REGISTER (TR)

Do not gain access to test registers which addresses are F0, F1 and F2.

3. Signal flow



4. Sound field simulation