Data sheet acquired from Harris Semiconductor
SCHS200B

November 1997 - Revised March 2002

High Speed CMOS Logic Decade Counter/Divider with 10 Decoded Outputs

Features

- **Fully Static Operation**
- **Buffered Inputs**
- **Common Reset**
- **Positive Edge Clocking**
- **Typical f_{MAX} = 50MHz at V_{CC} = 5V, C_L = 15pF, T_A = 25^oC**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

Description

The 'HC4017 is a high speed silicon gate CMOS 5-stage Johnson counter with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition clock period of the 10 clock period cycle. The CARRY (TC) output transitions low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE ($\overline{CE}$) to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET (MR) input is also provided which when taken high sets all the decoded outputs, except "0", low.

The device can drive up to 10 low power Schottky equivalent loads.

Ordering Information

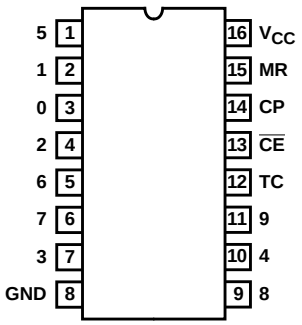
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC4017F3A	-55 to 125	16 Ld CERDIP
CD74HC4017E	-55 to 125	16 Ld PDIP
CD74HC4017NSR	-55 to 125	16 Ld SOP

NOTES:

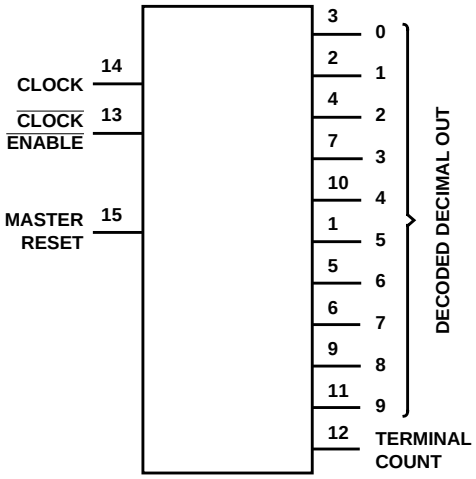
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinout

CD54HC4017
(CERDIP)
CD74HC4017
(PDIP, SOP)
TOP VIEW



Functional Diagram



TRUTH TABLE

CP	$\overline{CE}$	MR	OUTPUT STATE †
L	X	L	No Change
X	H	L	No Change
X	X	H	“0” = H, “1”-”9” = L
↑	L	L	Increments Counter
↓	X	L	No Change
X	↑	L	No Change
H	↓	L	Increments Counter

NOTE:
H = High Level
L = Low Level
↑ = High to Low Transition
↓ = Low to High Transition
X = Don’t Care.
† If n < 5 TC = H, Otherwise = L

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 3):
PDIP Package . . . . . 67°C/W
SOP Package . . . . . 64°C/W
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

NOTE: For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Maximum Clock Frequency	f_{MAX}	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	35	-	20	-	MHz
			6	35	-	-	49	-	23	-	MHz
CP Pulse Width	t_W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
MR Pulse Width	t_W	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Set-up Time, $\overline{CE}$ to CP	t_{SU}	-	2	75	-	-	95	-	110	-	ns
			4.5	15	-	-	19	-	22	-	ns
			6	13	-	-	16	-	19	-	ns
Hold Time, $\overline{CE}$ to CP	t_H	-	2	0	-	-	0	-	0	-	ns
			4.5	0	-	-	0	-	0	-	ns
			6	0	-	-	0	-	0	-	ns
MR Removal Time	t_{REM}	-	2	5	-	-	5	-	5	-	ns
			4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay CP to any Dec. Out	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	230	-	290	-	345	ns
		C_L = 50pF	4.5	-	-	46	-	58	-	69	ns
		C_L = 15pF	5	-	19	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	39	-	49	-	59	ns
CP to TC	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	230	-	290	-	345	ns
		C_L = 50pF	4.5	-	-	46	-	58	-	69	ns
		C_L = 15pF	5	-	19	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	39	-	49	-	59	ns
$\overline{CE}$ to any Dec. Out	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	250	-	315	-	375	ns
		C_L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	43	-	54	-	64	ns
$\overline{CE}$ to TC	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	250	-	315	-	375	ns
		C_L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	43	-	54	-	64	ns

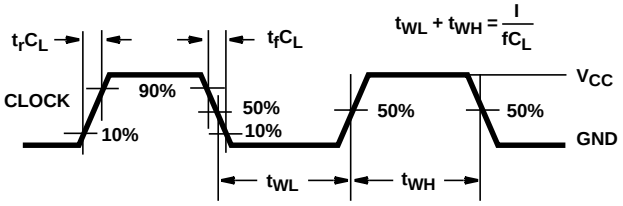
Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
MR to any Dec. Out	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	230	-	290	-	345	ns
		C_L = 50pF	4.5	-	-	46	-	58	-	69	ns
		C_L = 15pF	5	-	19	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	39	-	49	-	59	ns
MR to TC	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	230	-	290	-	345	ns
		C_L = 50pF	4.5	-	-	46	-	58	-	69	ns
		C_L = 15pF	5	-	19	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	39	-	49	-	59	ns
Transition Time TC, Dec. Out	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
		C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C_L = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum CP Frequency	f_{MAX}	C_L = 15pF	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	C_L = 15pF	5	-	39	-	-	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per package.
5. $P_D = V_{CC}^2 f_i \Sigma \; C_L V_{CC}^2 fo$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

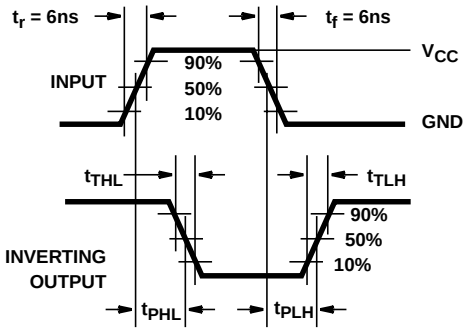


FIGURE 2. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)

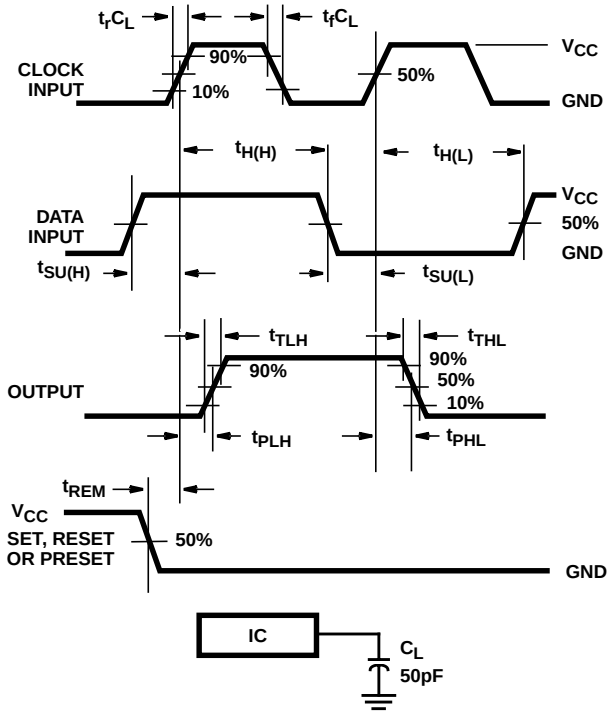


FIGURE 3. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Timing Diagrams

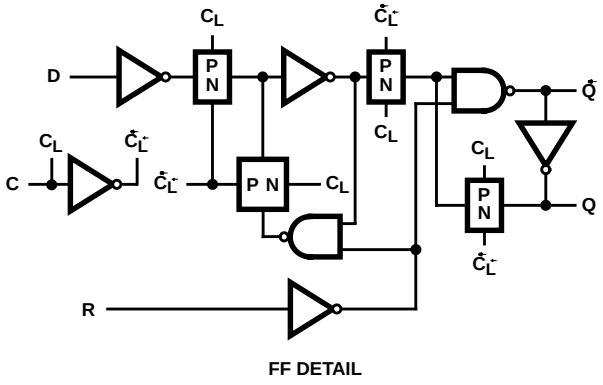


FIGURE 4.

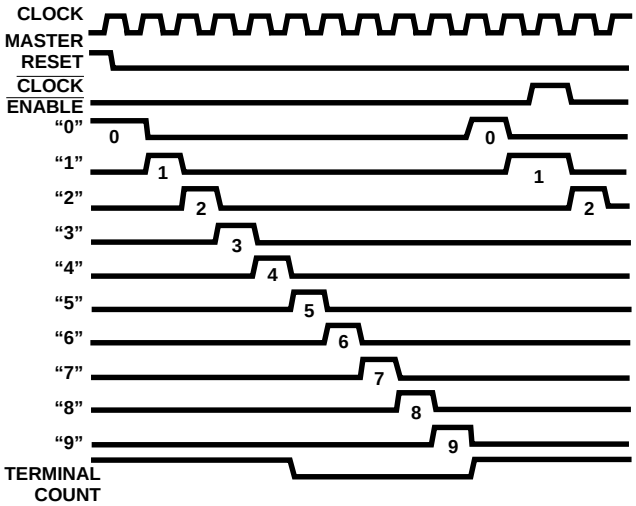


FIGURE 5.

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