Author: Don LaFontaine

Building an Accurate SPICE Model for Low Noise, Low Power Precision Amplifiers

Abstract

In today's fast moving competitive markets, more and more customers are requesting SPICE models to run comprehensive circuit simulations. System engineers are requiring increasingly accurate models for all types of integrated circuits. Earlier SPICE models (1980) had to minimize the number of nonlinear elements to minimize simulation time, all at the cost of accuracy. Today's models, thanks to the advancement of computing power, can increase the number of nonlinear elements and improve the accuracy of the models. The focus of this Application Note is to provide a method for developing a multi-stage SPICE model for low noise and low power operational amplifiers. The model presented, started with the work from Mark Alexander and Derek F. Bowers from Analog Devices (Appnote AN-138, 1990) [1]. The final model ended up with several key architectural changes that were required to model today's low noise, and low power precision amplifiers.

This application note provides a systematic process that simplifies the understanding of how to build an accurate straightforward SPICE model. This is accomplished by a model architecture that processes the input signal through several stages. The model parameters can easily be calculated using a hand calculator or Excel spreadsheet. The application note does not discuss the process of using SPICE, and assumes the user is familiar with this software.

The model presented in this application note is the ISL28127 single-pole 10MHz amplifier. The model enables the user to simulate important AC and DC parameters of an amplifier. For higher speed amplifiers, with multiple poles and zeros, reference AN-138 [1].

The AC parameters incorporated into the model are: 1/f and flat-band noise, slew rate, CMRR, gain and phase. The DC parameters are VOS, IOS, total supply current and output voltage swing. The model uses typical (+25°C) parameters given in the “Electrical Specifications” table of the data sheet [2].

Introduction

The key to an accurate model is the input stage. The closer you model the input stage to the actual amplifier, the better your results. With only a few of the process parameters of the input stage transistors or MOSFETs, you can achieve very accurate AC representation of the amplifiers performance.

Another advantage of this model's architecture is the ability to model amplifiers with split supplies. There is no ground reference in any of the signal processing blocks. Instead, after the differential to single-ended conversion, all internally generated node voltages are referenced to the mid point of the supplies, much like the actual operation of an amplifier.

Discussed in this application note are the following topics:

1. The different cascaded stages of the SPICE Model:
   - Voltage Noise Stage
   - Input Stage
   - 1st Gain Stage
   - 2nd Gain Stage
   - Mid Supply Stage
   - Supply Isolation Stage
   - Common Mode Gain Stage
   - Output Stage
2. How the VCCS stages works
3. How the VCCS output stage works
4. Systematic process for calculating model parameters
5. Simulation results. Actual device vs simulation
6. Conclusions

Cascaded Stages

Figure 1 is the schematic for the SPICE model and Figure 2 is the net list. Notice from the schematic, the only circuitry resembling an amplifier is the Input Stage. All other stages process the input signal with Voltage Controlled Current Sources (VCCS) and Voltage Controlled Voltage Sources (VCVS) along with diodes, DC supplies, simple resistors, capacitors and inductors.

The circuit schematic is built from eight different functional blocks. Each block is discussed in the following sections, with details of the blocks’ functionality and design considerations.

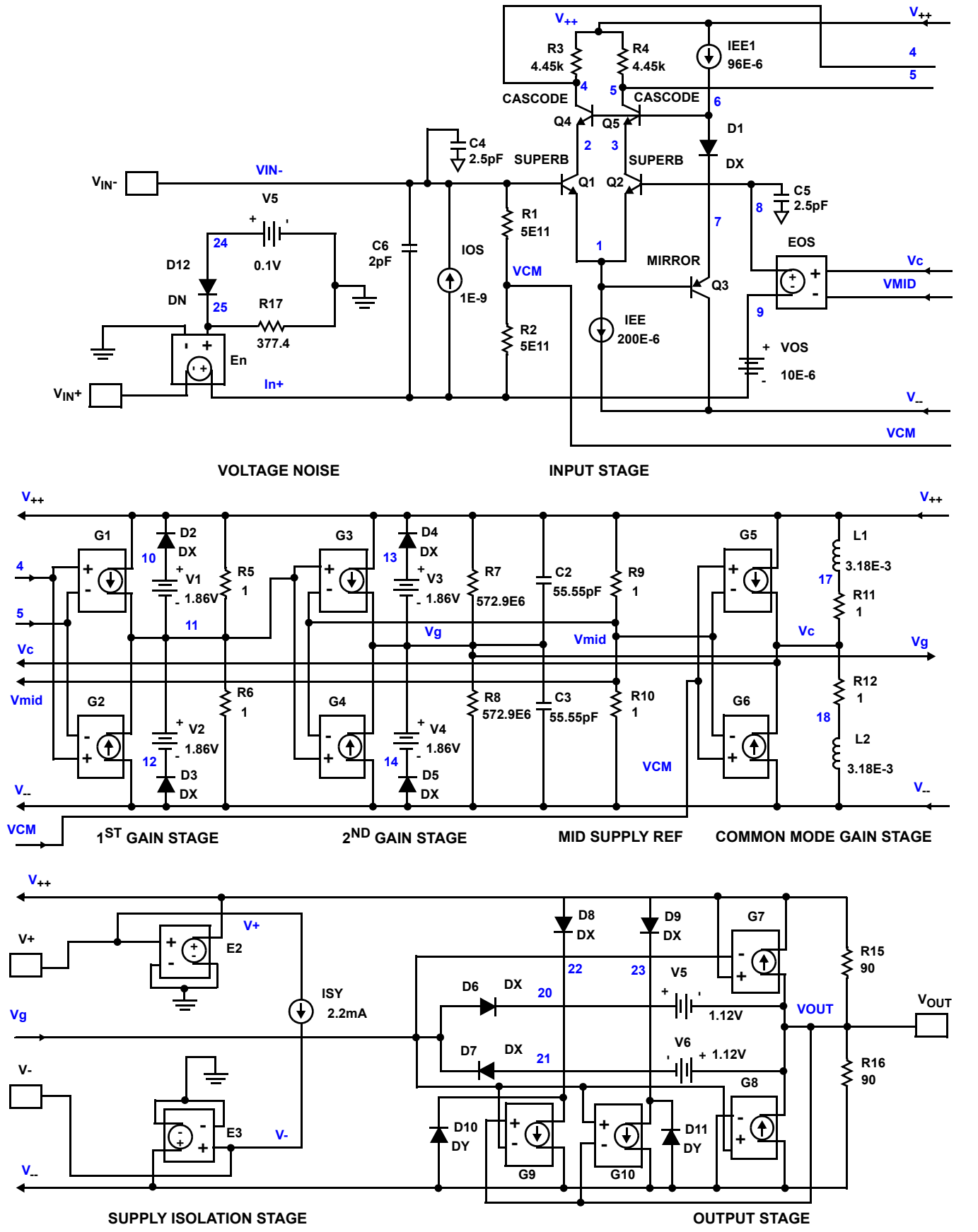


FIGURE 1. SPICE SCHEMATIC

```
* source ISL28127_SPICEmodel
* Revision C, August 8th 2009 LaFontaine
* Model for Noise, supply currents, 150dB f=50Hz
CMRR, *128dB f=5Hz AOL
*Copyright 2009 by Intersil Corporation
*Refer to data sheet “LICENSE STATEMENT” Use of
*this model indicates your acceptance with the
*terms and provisions in the License Statement.
* Connections: +input
*               |    -input
*               |    |    +Vsupply
*               |    |    |    -Vsupply
*               |    |    |    |    output
*               |    |    |    |    |
.subckt ISL28127subckt Vin+ Vin-V+ V- VOUT
* source ISL28127_SPICEMODEL_0_0
*
*Voltage Noise
E_En          IN+ VIN+ 25 0 1
R_R17          25 0  377.4
D_D12          24 25 DN
V_V7          24 0 0.1
*
*Input Stage
I_IOS          IN+ VIN- DC 1e-9
C_C6          IN+ VIN- 2E-12
R_R1          VCM VIN-  5e11
R_R2          IN+ VCM  5e11
Q_Q1          2 VIN- 1 SuperB
Q_Q2          3 8 1 SuperB
Q_Q3          V-- 1 7 Mirror
Q_Q4          4 6 2 Cascode
Q_Q5          5 6 3 Cascode
R_R3          4 V++ 4.45e3
R_R4          5 V++ 4.45e3
C_C4 VIN- 0  2.5e-12
C_C5 8 0  2.5e-12
D_D1          6 7 DX
I_IEE          1 V-- DC 200e-6
I_IEE1          V++ 6 DC 96e-6
V_VOS          9 IN+ 10e-6
E_EOS          8 9 VC VMID 1
*
*1st Gain Stage
G_G1          V++ 11 4 5 0.0487707
G_G2          V-- 11 4 5 0.0487707
R_R5          11 V++ 1
R_R6          V-- 11  1
D_D2          10 V++ DX
D_D3          V-- 12 DX
V_V1          10 11 1.86
V_V2          11 12 1.86
*
*2nd Gain Stage
G_G3          V++ VG 11 VMID 4.60767E-3
G_G4          V-- VG 11 VMID 4.60767E-3
R_R7          VG V++ 572.958E6
R_R8          V-- VG  572.958E6
C_C2          VG V++ 55.55e-12
C_C3          V-- VG  55.55e-12
D_D4          13 V++ DX
D_D5          V-- 14 DX
V_V3          13 VG 1.86
V_V4          VG 14 1.86
*
*Mid supply Ref
R_R9          VMID V++ 1
R_R10          V-- VMID  1
I_ISY     V+ V- DC 2.2E-3
E_E2          V++ 0 V+ 0 1
E_E3          V-- 0 V- 0 1
*
*Common Mode Gain Stage with Zero
G_G5          V++ VC VCM VMID 31.6228e-9
G_G6          V-- VC VCM VMID 31.6228e-9
R_R11          VC 17  1
R_R12          18 VC  1
L_L1          17 V++ 3.183e-3
L_L2          18 V-- 3.183e-3
*
*Output Stage with Correction Current Sources
G_G7          VOUT V++ V++ VG 1.11e-2
G_G8          V-- VOUT VG V-- 1.11e-2
G_G9          22 V-- VOUT VG 1.11e-2
G_G10          23 V-- VG VOUT 1.11e-2
D_D6          VG 20 DX
D_D7          21 VG DX
D_D8          V++ 22 DX
D_D9          V++ 23 DX
D_D10          V-- 22 DY
D_D11          V-- 23 DY
V_V5          20 VOUT 1.12
V_V6          VOUT 21 1.12
R_R15          VOUT V++ 9E1
R_R16          V-- VOUT  9E1
*
.model SuperB npn
+ is=184E-15 bf=30e3 va=15 ik=70E-3 rb=50
+ re=0.065 rc=35 cje=1.5E-12 cjc=2E-12
+ kf=0 af=0
.model Cascode npn
+ is=502E-18 bf=150 va=300 ik=17E-3 rb=140
+ re=0.011 rc=900 cje=0.2E-12 cjc=0.16E-12f
+ kf=0 af=0
.model Mirror pnp
+ is=4E-15 bf=150 va=50 ik=138E-3 rb=185
+ re=0.101 rc=180 cje=1.34E-12 cjc=0.44E-12
+ kf=0 af=0
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28127subckt
```

FIGURE 2. SPICE NET LIST

Voltage Noise Stage

The first stage in the model schematic, moving from left to right, is the Voltage Noise Stage. This stage generates the 1/f and flat-band noise. To generate a flat-band voltage noise of a precision amplifier with only 4nV/√Hz, all diodes and transistor model parameters kf (flicker noise coefficient) and af (flicker noise exponent) need to be set to zero. To lower the noise floor of the model to single digit nanovolts, it may be necessary to reduce the network's Johnson noise [3] by reducing the resistance values where possible. Before reducing the resistor values, the process is to calculate the standard resistor values and complete all simulation tweaks. Once this is done, the last step is to tweak the Voltage Noise Stage by dropping the resistor values to 1Ω while recalculating the g_m and time constants of the stages to maintain the same transfer function for that stage. Resistors R_5, R_6, and R_9 thru R_{12} are resistors that can easily be set to 1Ω. For amplifiers with noise levels in the flat-band range of 100's of nV, reducing the network's Johnson noise may not be necessary. Initial noise simulations will tell you if this step is necessary. With the model's flat-band noise set below the amplifier's noise floor, the user can now adjust the 1/f and flat-band noise with adjustments to DN, R_{17} and V_5.

Input Stage

The ISL28127 was selected for this application note to illustrate the level of accuracy obtainable by modeling an amplifiers exact input structure. The Input Stage of the ISL28127 consists of five bipolar transistors that model the actual device configuration, as shown in Figure 1. This however will not be the case for most SPICE models. Figure 3 and Figure 4 show typical NMOS and PMOS input stages respectively.

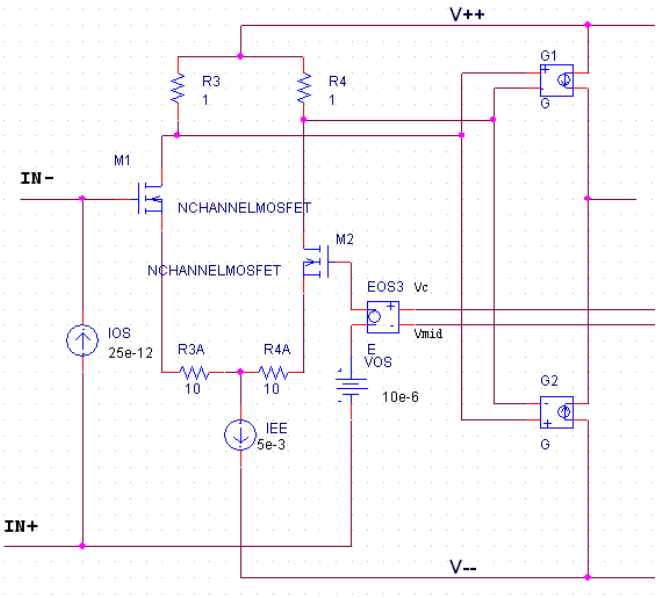


FIGURE 3. TYPICAL NMOS INPUT STAGE

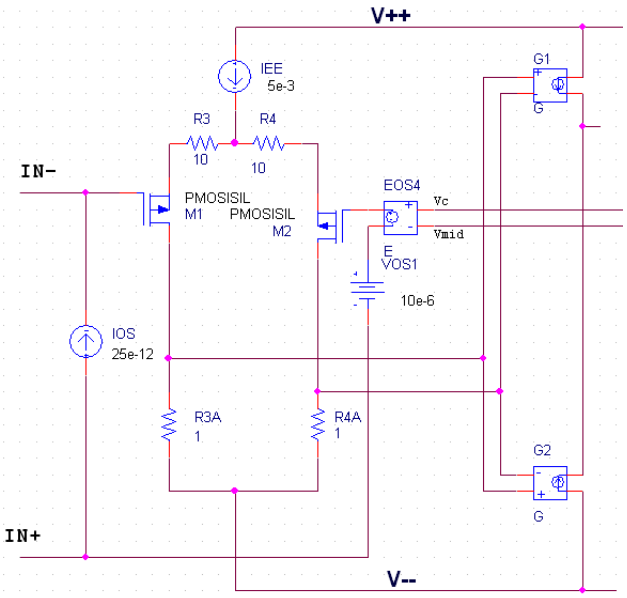


FIGURE 4. TYPICAL PMOS INPUT STAGE

The Input Stage can be configured with the same type of input device (NPN, PNP, P and N channel MOSFETs or J-FETS) as the physical op amp being modeled. The Input Stage includes a current supply to model IOS, a voltage supply to model VOS and a VCVS along with R_1 and R_2 to account for CMRR of the device.

1st Gain Stage

The purpose of the 1st Gain Stage is to set the combined gain of the Input Stage and the 1st Gain Stage to 1. Setting the combined gains to 1 simplifies the calculation to determine the slew-rate limiting components in the 2nd Gain Stage. Diodes D_2 and D_3 along with DC supplies V_1 and V_2 might be unnecessary, because their function is to clamp the output voltage swing and were going to do that in the next stage. We left them in because they're free. DC supply voltages V_1 and V_2 should be slightly larger than V_3 and V_4 in the 2nd Gain Stage. The thought is to limit most of the signal amplitude in the 1st stage and do the final amplitude tweak in the 2nd stage.

2nd Gain Stage

The 2nd Gain Stage is where the AVOL, bandwidth and slew-rate of the amplifier are set using G_3, G_4, R_7, R_8, C_2 and C_3. Diodes D_4 and D_5 along with DC supplies V_3 and V_4 are used to set the maximum output voltage swing.

Mid Supply Reference Stage

The Mid Supply Reference Stage is simply two equal resistors R_9 and R_{10}. These resistors are used to generate a mid supply reference voltage. The resistor values are set to 1Ω to reduce the Johnson voltage noise of the model. The high current that flows through these resistors is transparent to the model user because of the Supply Isolation Stage, more free stuff.

Common Mode Gain Stage

The Common Mode Gain Stage consists of two VCCS's that drive two equal resistors in series with an inductor connected to the supply rails. The inductors simulate the typical fall-off of CMRR that most amplifiers exhibit as the input frequency is increased. The current sources are controlled by the input common mode voltage (generated by resistors R_1 and R_2 in the Input Stage) relative to the mid supply voltage. Each control source has a g_m equal to the reciprocal of the associated resistor value divided by the CMRR of the amplifier at DC (Equation 10). The inductors add a zero to the common-mode gain, which is equivalent to adding a pole to the CMRR. The common-mode voltage, after being scaled and appropriately frequency shaped, is then added back into the Input Stage via the VCVS called EOS.

Supply Isolation Stage

The Supply Isolation Stage consists of two VCVS's and a current source. This stage enables the user to program the total supply current of the amplifier with just one entry in the node list. It also isolates the internal supply currents from the external supply current seen by the user. This enables the model to provide the correct supply current for low power amplifiers with low voltage noise.

Output Stage

The operation of the Output Stage is not entirely obvious. The amplifier's output signal, after receiving all the appropriate frequency shaping, appears as a voltage referenced to mid supply at the inputs to G_7 and G_8. G_7 and G_8 drive two equal resistors connected to the supply rails and act as active current generators. Both G_7 and G_8 generate just enough current to provide the desired voltage drop across its parallel resistor. Refer to the section "How the VCCS Output Stage Works" on page 6.

When there is no load on the output, the model draws no current from either supply rail, thus behaving like an amplifier output. Simulating the right output resistance means the DC open loop gain will be properly reduced as the amplifier is loaded.

When a load is applied to the output, equal currents will be pulled from both supply rails. To make the output behave like a real amplifier, G_9 and G_{10} force the appropriate amount of current to make it appear as if all the current is being sourced or sunk from the correct supply.

Output short circuit protection is provided by diodes D_6 and D_7 along with DC supplies V_5 and V_6. Under fault conditions, the output voltage is clamped to the previous frequency shaping stage. The output short circuit current limit is determined by adjusting the value of V_5 and V_6.

How the VCCS Stage Works

When the voltage at the inputs to G_1 and G_2 (Figure 5) increases, the resultant voltage at the Midpoint will rise. Likewise, when the voltage at the inputs decrease, the midpoint voltage will decrease. If the g_m of the stage is equal to the reciprocal of the parallel resistor, the stage has a positive unity gain.

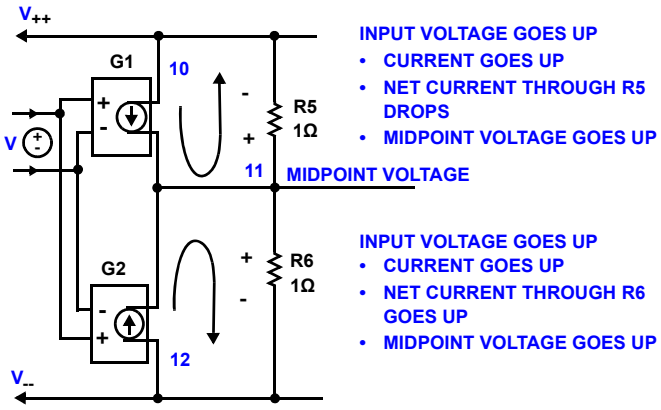


FIGURE 5. HOW THE VCCS WORKS

The single-ended equivalent circuit of Figure 5 is shown in Figure 6. The circuit shown in Figure 6 is sometimes easier to help visualize the signal flow through the stages.

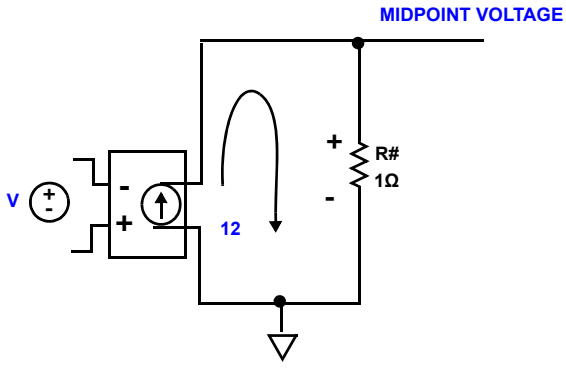
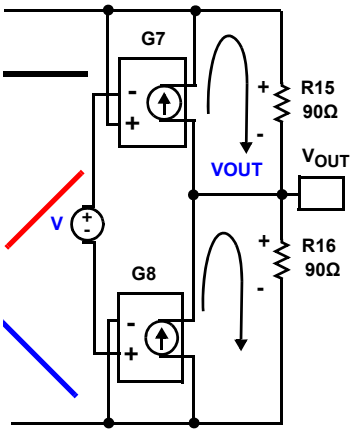


FIGURE 6. SINGLE-ENDED EQUIVALENT CIRCUIT TO FIGURE 5

How the VCCS Output Stage Works

Figure 7 explains how the Output Stage works for a steady input voltage, an increasing input voltage and a decreasing input voltage.



INPUT VOLTAGE CONSTANT
- VOLTAGE DROP ACROSS RESISTORS EQUALLY OPPOSE EACH OTHER
- OUTPUT VOLTAGE STAYS AT MID SUPPLY

INPUT VOLTAGE GOES UP
- CURRENT REDUCES IN R15
- CURRENT INCREASES IN R16
- MIDPOINT VOLTAGE GOES UP

INPUT VOLTAGE GOES UP
- CURRENT INCREASES IN R15
- CURRENT REDUCES IN R16
- MIDPOINT VOLTAGE GOES DOWN

FIGURE 7. HOW THE VCCS OUTPUT STAGE WORKS

A Systematic Process for Calculating Model Parameters

Table 1 is a list of the amplifiers parameters required to calculate the model parameters. The values shown in the table are for the ISL28127 model.

Once the values in Table 1 are determined, the model parameters given in Equations 1 through 15 can be calculated and put into the SPICE schematic.

TABLE 1. DEVICE PARAMETERS

PARAMETER	VALUE	UNITS	COMMENTS
Quiescent Supply Current	2.2E-3	A	
VCC	15	V	
VEE	-15	V	
IEE	200E-6	A	Differential input current source
Slew Rate	3.6E6	V/sec	
Fp1	5	Hz	Dominant Pole (Figure 8)
AVOL	2640E3	V/V	128.43dB
VOS	1E-5	V	
IOS	1E-9	A	
Temperature	25	C	
Vt	0.0257	V	
Differential Input Resistance	5E-11	Ω	Default value if unknown
CMRR	3.16E7	V/V	150dB
Fcm	50	Hz	Common mode pole
Rout	45	Ω	
Isc	45	mA	
Voh	13.7	V	Vout max
Vol	-13.7	V	Vout max

The following equations will determine the model parameters for the SPICE schematic. Putting them into an Excel spreadsheet will enable the user to change critical specs and quickly see the effect on the op amp performance. The calculations are given for each stage of the model.

Input Stage and Gain Stage Calculations

The process to set the Slew Rate and unity gain bandwidth, for a single pole stage, is accomplished in 3 steps:

- Determine the Capacitor value knowing IEE and the Slew Rate (Equation 1). This effectively sets the maximum frequency for the single pole RC network, and therefore the unity gain bandwidth.
- Determine the Resistor value knowing the dominant pole frequency (Equation 2). This effectively sets the break point for the RC network.
- Determine the g_m of the VCCS knowing the desired AVOL and R value of the RC network.

STEP 1

$$C_2 = C_3 = \frac{IEE}{SlewRate} \quad \text{(EQ. 1)}$$

$$C_2 = C_3 = \frac{200 \times 10^{-6}}{3.6 \times 10^{-6}} = 55.55pF$$

IEE is the value of the current source feeding the input differential pair (reference Figure 1). Under Slew Rate conditions, instantaneously all of this current is flowing through one side of the differential pair (until the feedback loop catches up). Equation 1 is used to calculate the capacitor value to set the Slew Rate of the model. Equation 1 is basically $I_C = Cdv/dt$, with Slew Rate equal to dv/dt and IEE equal to I_C.

Equation 2 calculates the value of the resistor for a set capacitor value of $C_{2,3}$ and dominant pole frequency fp1.

STEP 2

$$R_7 = R_8 = \frac{1}{2\pi f_{p1} C_{2,3}} \quad \text{(EQ. 2)}$$

$$R_7 = R_8 = \frac{1}{2\pi(5)(55.55pF)} = 572.958M\Omega$$

Where f_{p1} = dominant pole (reference Figure 8).

Figure 8 shows the relationship of the unity gain bandwidth to the dominant pole frequency and AVOL.

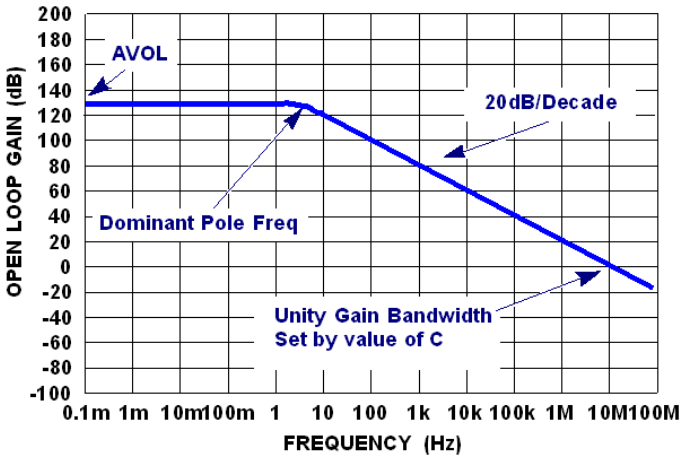


FIGURE 8. AVOL vs FREQUENCY

STEP 3

$$G_3 = G_4 = \frac{AVOL}{R_{7,8}} \qquad \text{(EQ. 3)}$$

$$G_3 = G_4 = \frac{2640\times10^{6}}{572.958\times10^{6}} = 4.6\times10^{-3}$$

Once again, the 1st Gain Stage is used to set the combined gain of the input stage and the 1st Gain Stage to 1. The voltage required at the input of G_3 and G_4 to cause 200 x 10^{-6} to flow through R_7 and R_8 is calculated in Equation 4.

$$g_m = \frac{I}{V} \Rightarrow V_{G_{3,4}} = \frac{I}{g_m} = \frac{200\times10^{-6}}{4.6\times10^{-3}} = 43.4\text{mV} \qquad \text{(EQ. 4)}$$

During Slew Rate limit, the current through either resistor R_3 or R_4 will be clamped by the 200 x 10^{-6} current sink. Which resistor has the current depends upon the polarity of the input voltage (positive R_4, negative R_3). This current will flow through the 4.45kΩ resistor resulting in a voltage drop of (200 x 10^{-6}) x (4.45kΩ) = 890mV. This voltage drop appears at the input to G_1 and G_2. In order to set the combined gain of the input stage and the 1st stage to one, we need to calculate the g_m of G_1 and G_2 so their output voltage equals 43.4mV (Equation 4) when 890mV is at their inputs. If we set the resistor value in parallel with the outputs of G_1 and G_2 to 1Ω, then the voltage will equal the current and we can write Equation 5 to solve for the g_m of G_1 and G_2.

$$G_1 = G_2 \Rightarrow g_m = \frac{I}{V} = \frac{43.4\times10^{3}}{890\times10^{-3}} = 48.77\times10^{-3} \qquad \text{(EQ. 5)}$$

If the design review document is not available, set R_3 and R_4 to 1Ω for the calculation of the voltage appearing at the inputs to G_1 and G_2.

$$R_3 = R_4 = 4.45\text{k}\Omega \quad \text{(from design review)} \qquad \text{(EQ. 6)}$$

Equations 7 and 8 are used to set V_1 through V_4 voltages for the maximum output voltage swing. The output voltage will be clamped at a voltage equal to V_{++} - ($V_{1,3}$ + $V_{D2,D4}$) for positive input voltage swings and V_{--} + ($V_{2,4}$ + $V_{D3,D5}$) for negative input voltage swings.

$$V_{1,3} = V_{CC} - (V_{OUTMAX}) + V_T\text{Ln}\left(\frac{2I_{EE}}{I_S}\right) \qquad \text{(EQ. 7)}$$

$$V_{2,4} = (-V_{OUTMAX}) - V_{EE} + V_T\text{Ln}\left(\frac{2I_{EE}}{I_S}\right) \qquad \text{(EQ. 8)}$$

Where V_T = 0.02585V at T = +25°C.

I_S = 1 x 10-12 A (for both diodes).

You can substitute some data sheet parameters directly into the model. These parameters are:

EOS = Input Offset Voltage (DC component only).

IOS = Input Offset Current.

C_{diff} = Input differential capacitance (not shown in this model).

Common-Mode Gain Stage

$$R_{11} = R_{12} = 1\text{M}\Omega \qquad \text{(EQ. 9)}$$

$$G_7 = G_8 = \frac{1}{R_{11,12}\times\text{CMRR}} \qquad \text{(EQ. 10)}$$

$$L_1 = L_2 = \frac{R_{11,12}}{2\pi\text{fp(cm)}} \qquad \text{(EQ. 11)}$$

Where fcm is common-mode pole from the CMRR vs Frequency curve (similar to the dominant frequency pole shown in Figure 8).

Output Stage

Setting the g_m equal to the reciprocal of $2R_{OUT}$ results in unity gain through G7-G10. The value of $2R_{OUT}$ results from the need to have the output currents appear to be coming from one supply rail.

$$G_7 = G_8 = G_9 = G_{10} = \frac{1}{2R_{OUT}} \qquad \text{(EQ. 12)}$$

$$R_{15} = R_{16} = 2\times R_{OUT} \qquad \text{(EQ. 13)}$$

$$V_3 = I_{SC}(0.764)R_{OUT} - V_T\text{Ln}\left(\frac{20\times10^{6}}{I_S}\right) \qquad \text{(EQ. 14)}$$

$$V_4 = \left|I_{SC}(0.764)R_{OUT}\right| - V_T\text{Ln}\left(\frac{20\times10^{6}}{I_S}\right) \qquad \text{(EQ. 15)}$$

Simulation Results

Figures 9 through 14 compare actual device performance to simulation results. For a complete set of comparisons, reference the data sheet [2].

Characterization vs Simulation Results

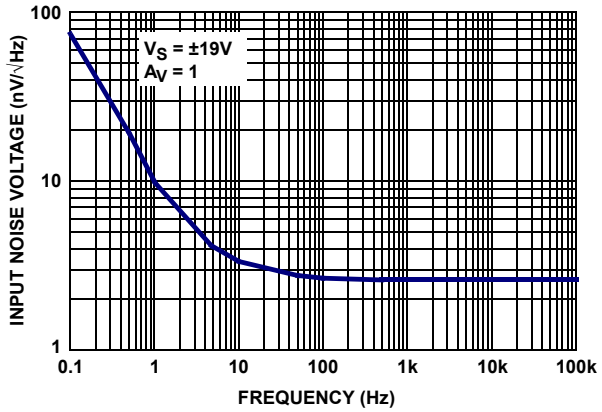


FIGURE 9. CHARACTERIZED INPUT NOISE VOLTAGE

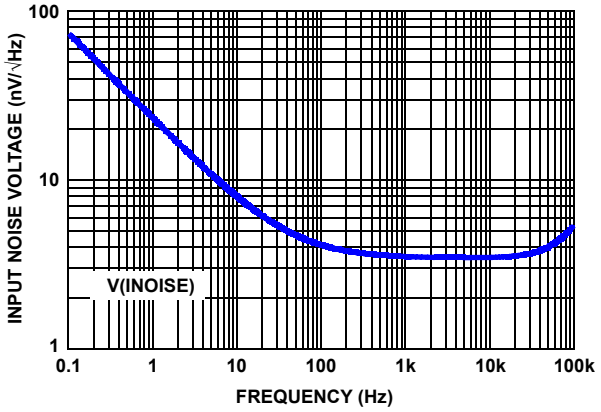


FIGURE 10. SIMULATED INPUT NOISE VOLTAGE

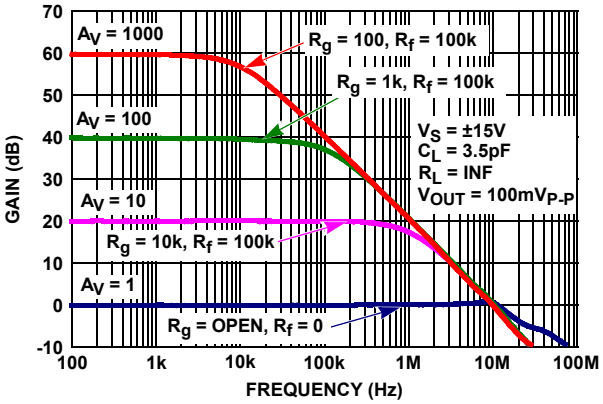


FIGURE 11. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

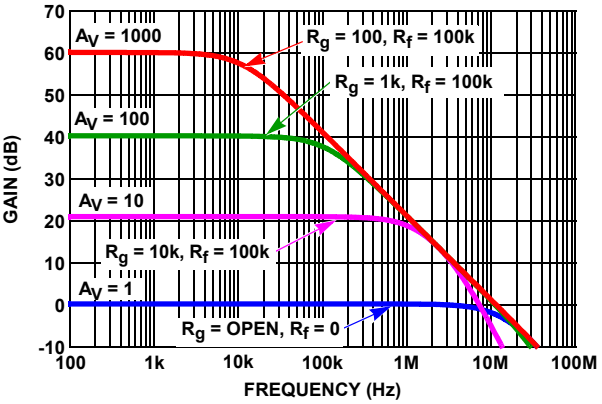


FIGURE 12. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

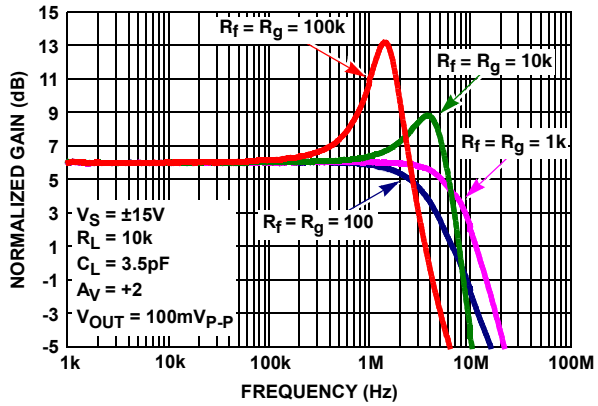


FIGURE 13. CHARACTERIZED CLOSED LOOP GAIN vs R_f/R_g

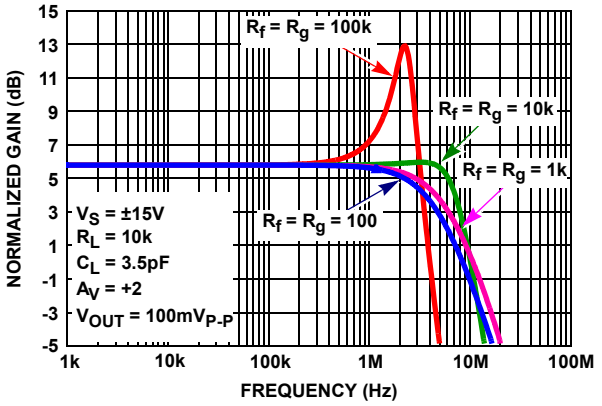


FIGURE 14. SIMULATED CLOSED LOOP GAIN vs R_f/R_g

Characterization vs Simulation Results (Continued)

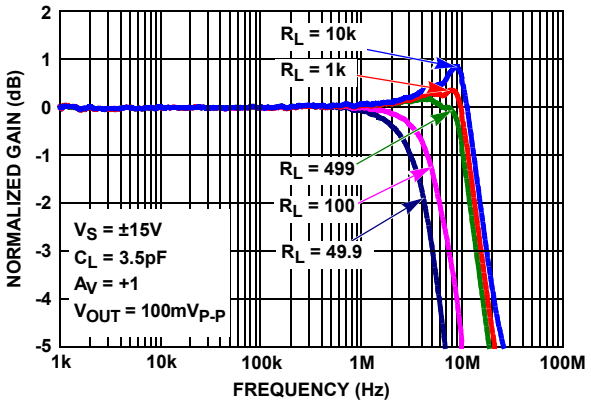


FIGURE 15. CHARACTERIZED CLOSED LOOP GAIN vs R_L

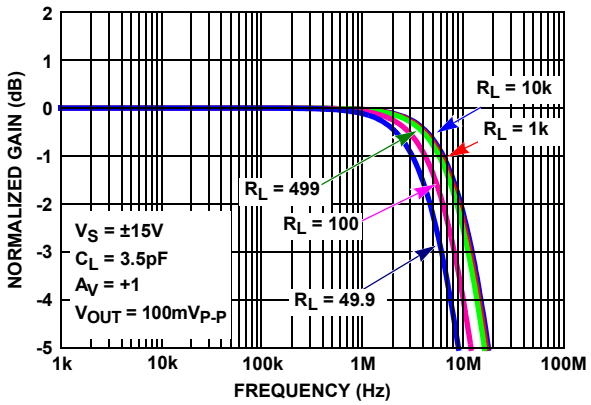


FIGURE 16. SIMULATED CLOSED LOOP GAIN vs R_L

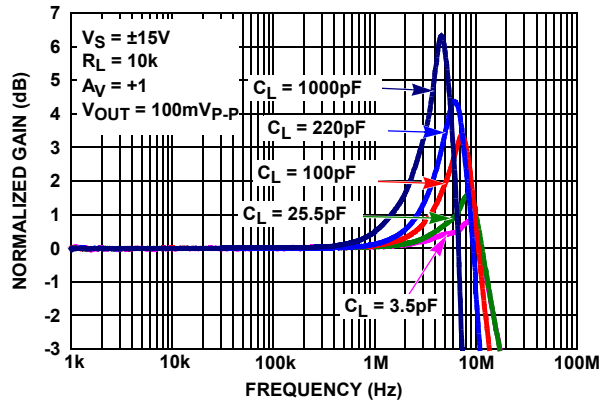


FIGURE 17. CHARACTERIZED CLOSED LOOP GAIN vs C_L

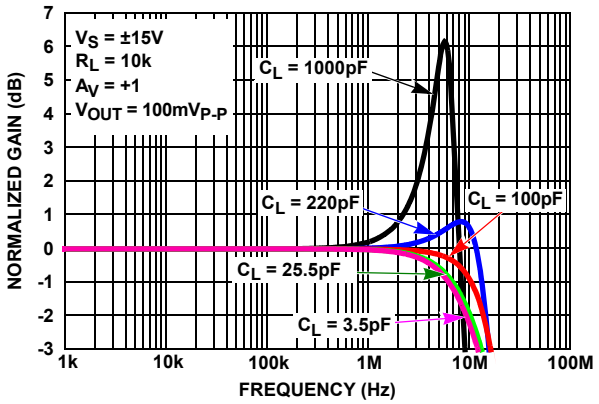


FIGURE 18. SIMULATED CLOSED LOOP GAIN vs C_L

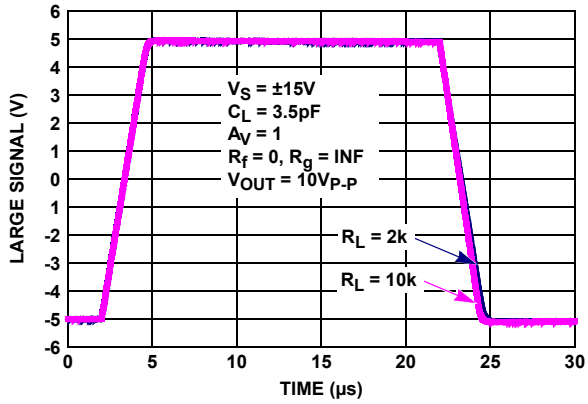


FIGURE 19. CHARACTERIZED LARGE SIGNAL 10V STEP RESPONSE

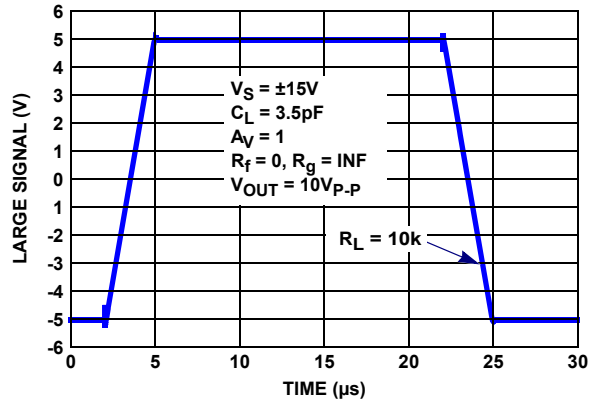


FIGURE 20. SIMULATED LARGE SIGNAL 10V STEP RESPONSE

Characterization vs Simulation Results (Continued)

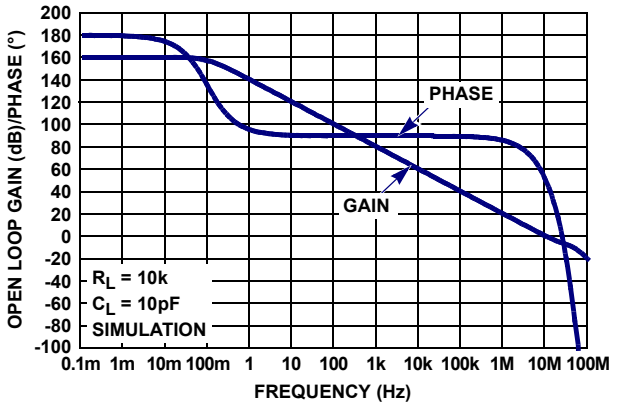


FIGURE 21. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

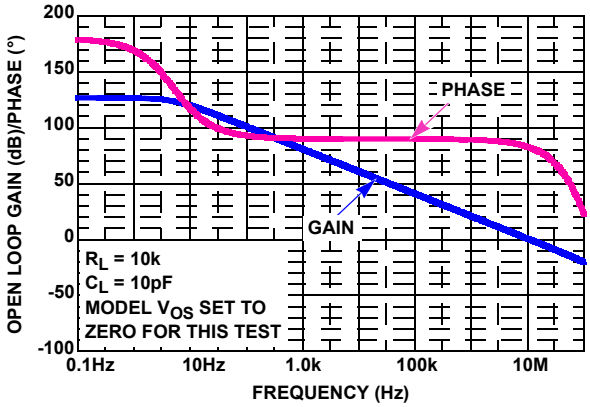


FIGURE 22. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

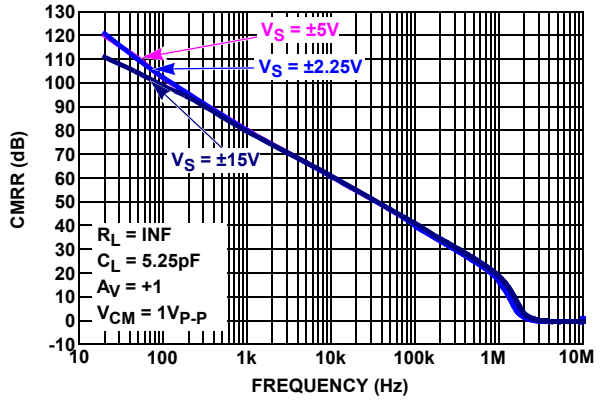


FIGURE 23. CHARACTERIZED CMRR vs FREQUENCY

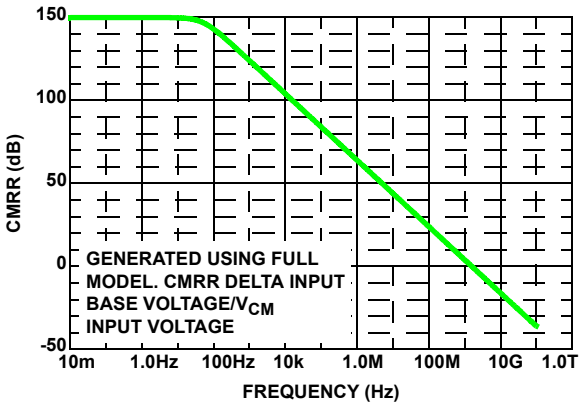


FIGURE 24. SIMULATED CMRR vs FREQUENCY

Conclusions

This Application Note has presented a method for building an accurate straightforward SPICE model for today's low noise and low power precision amplifiers. The extremely close simulation to actual part comparison results was achieved by taking advantage of today's improved computing power and modeling 5 bipolar transistors with their specific model parameters for each type of transistor. Improvements to previous models include the ability to model single digit nanovolt noise parameters and very low total system supply currents for micro-powered amplifiers.

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I would also like to thank Bob Pospisil for his technical expertise with op amps and helping me solve various problems along the way.

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[1] Mark Alexander and Derek F. Bowers, Application Note AN-138, "SPICE-Compatible Op Amp Macro-Models", Analog Devices.

[2] ISL28127, ISL28227 FN6633 Intersil data sheet http://www.intersil.com/data/fn/fn6633.pdf.

[3] Derek F. Bowers, IEEE 1989, "Minimizing Noise in Analog Bipolar Circuit Design", Precision Monolithics, Inc.