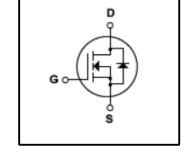


Silicon N-Channel MOSFET

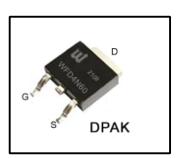
Features

- $4A,600V.R_{DS(on)}(Max\ 2.5\Omega)@V_{GS}=10V$
- Ultra-low Gate Charge(Typical 16nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Isolation Voltage (VISO = 4000V AC)
- Maximum Junction Temperature Range(150°C)



General Description

This Power MOSFET is produced using Winsemi's advanced Planar stripe, DMOS technology. This latest technology has Been Especially designed to minimize on-state resistance, have a high Rugged avalanche characteristics. This devices is specially well Suited for half bridge and full bridge resonant topology line a Electronic lamp ballast.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
VDSS	Drain Source Voltage	600	V
lp	Continuous Drain Current(@Tc=25°ℂ)	4	Α
l ID	Continuous Drain Current(@Tc=100℃)	2.5	А
Ірм	Drain Current Pulsed (Note1)	16	A
Vgs	Gate to Source Voltage	±30	V
Eas	Single Pulsed Avalanche Energy (Note 2)	240	mJ
Ear	Repetitive Avalanche Energy (Note 1)	10	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
Pp	Total Power Dissipation(@Tc=25℃)	80	W
PD	Derating Factor above 25℃	0.78	W/℃
TJ, Tstg	Junction and Storage Temperature	-55~150	°C
TL	Channel Temperature	300	$^{\circ}$

Thermal Characteristics

Symbol	Doramotor	Value			Linita
Symbol	Parameter	Min	Тур	Max	Units
Rajc	Thermal Resistance, Junction-to-Case	-	-	1.56	°C/W
RQJA	Thermal Resistance, Junction-to-Ambient*			50	
R _{QJA}	Thermal Resistance, Junction-to-Ambient	-	-	110	°C/W

^{*}When mounted on the minimum pad size recommended(PCB Mount)





Electrical Characteristics (Tc = 25° C)

Charac	teristics	Symbol	Test Condition	Min	Туре	Max	Unit
Gate leakage cu	rrent	Igss	Vgs = ±30 V, Vps = 0 V	-	-	±100	nA
Gate-source bre	akdown voltage	V _{(BR)GSS}	I _G = ±10 μA, V _{DS} = 0 V	±30	-	-	V
Drain cut-off current			V _{DS} = 600 V, V _{GS} = 0 V	-	-	10	μA
		Ipss	V _{DS} = 480 V, T _c = 125°C	-	-	100	μA
Drain-source bre	eakdown voltage	V(BR)DSS	I _D = 250 μA, V _{GS} = 0 V	600	-	-	V
Gate threshold v	oltage	VGS(th)	V _{DS} = 10 V, I _D =250 μA	2	-	4	V
Drain-source Of	N resistance	RDS(ON)	Vgs = 10 V, ID =3.25A	-	1.8	2.5	Ω
Input capacitance		Ciss	V _{DS} = 25 V,	-	545	670	
Reverse transfer capacitance		Crss	V _G S = 0 V,	-	7	10	pF
Output capacitar	Output capacitance		f = 1 MHz	-	70	90	
	Rise time	tr	V _{DD} =300 V,	-	10	30	
Outlibe in a time	Turn-on time	ton	I _D = 4.4 A	-	35	80	
Switching time	Fall time	tf	R _G =25 Ω	-	45	100	ns
	Turn-off time	toff	(Note4,5)	-	20	50	
Total gate charge (gate-source		0-	V _{DD} = 480 V,		16	20	
plus gate-drain)		Qg	Vgs = 10 V,	-	16	20	-0
Gate-source charge		Qgs	I _D =4.4A	-	3.4	-	nC
Gate-drain ("miller") Charge		Qgd	(Note4,5)	-	7	-	

Source-Drain Ratings and Characteristics (Ta = 25° C)

Characteristics	Symbol	Test Condition	Min	Туре	Max	Unit
Continuous drain reverse current	IDR	-	-	-	4	Α
Pulse drain reverse current	IDRP	-	-	-	17.6	Α
Forward voltage (diode)	VDSF	IDR =4.4 A, VGS = 0 V	-	-	1.4	V
Reverse recovery time	trr	IDR = 4.4 A, VGS = 0 V,	-	390	-	ns
Reverse recovery charge	Qrr	dl _{DR} / dt = 100 A / μs	-	2.2	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=18.5mH,I_{AS}=4.4A,V_DD=50V,R_G=0\Omega,Starting T_J=25 $^{\circ}\mathrm{C}$

 $3.I_{SD} \!\! \leq \!\! 4A,\! di/dt \!\! \leq \!\! 200A/us, \ V_{DD} \!\! < \!\! BV_{DSS},\! STARTING \ T_J \!\! = \!\! 25\,^{\circ}\! C$

4.Pulse Test: Pulse Width≤300us,Duty Cycle≤2%

 $5. Essentially independent of operating \ temperature.\\$

This transistor is an electrostatic sensitive device

Please handle with caution



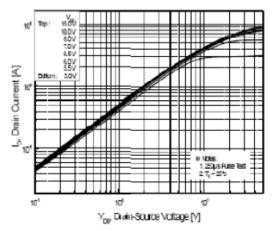


Fig.1 On-State Characteristics

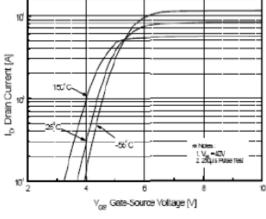


Fig.2 Transfer Current characteristics

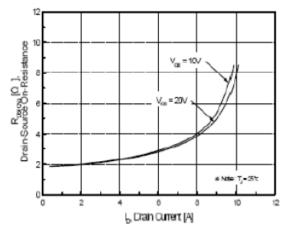


Fig3. On Resistance Variation vs
Drain current

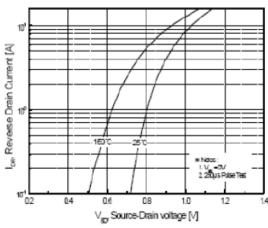


Fig.4 Body Diode Forward Voltage Variation vs Source Current and Temperature

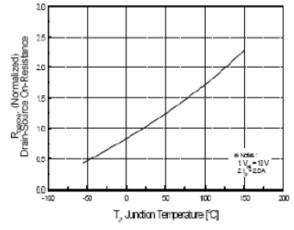


Fig.5 On-Resistance Variation vs

Junction Temperature

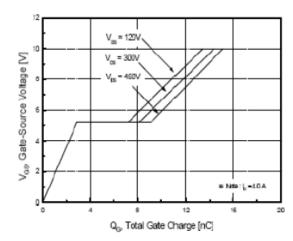


Fig.6 Gate Charge Characteristics

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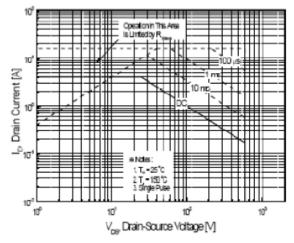


Fig.7 Maximum Safe Operation Area

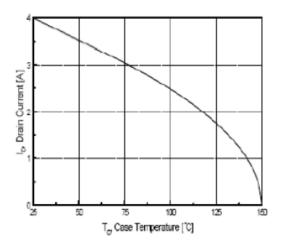


Fig.8 Maximum Drain Current vs Case Temperature

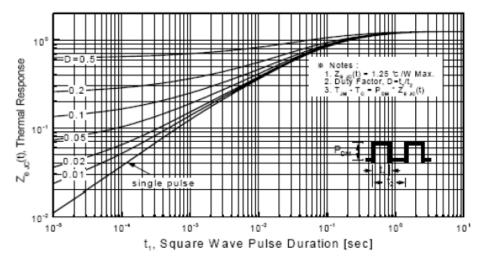


Fig.9 Transient Thermal Response curve



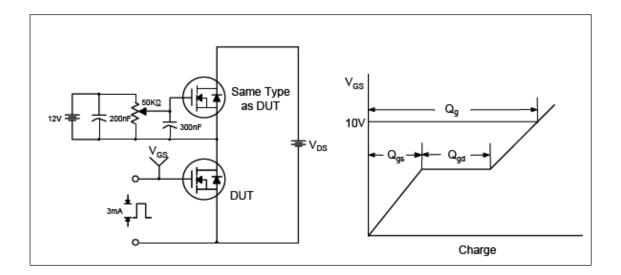


Fig.10 Gate Test Circuit & Waveform

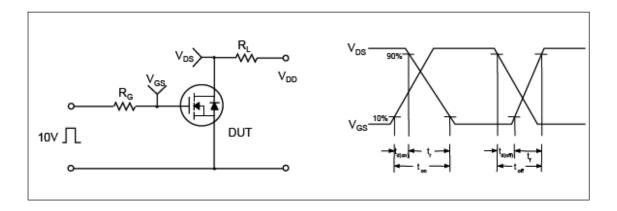


Fig.11 Resistive Switching Test Circuit & Waveform

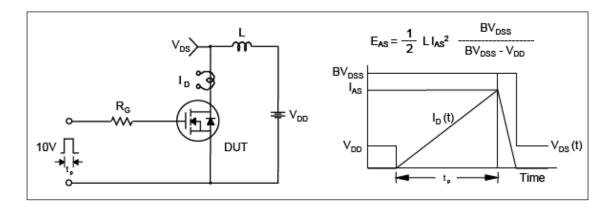


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform

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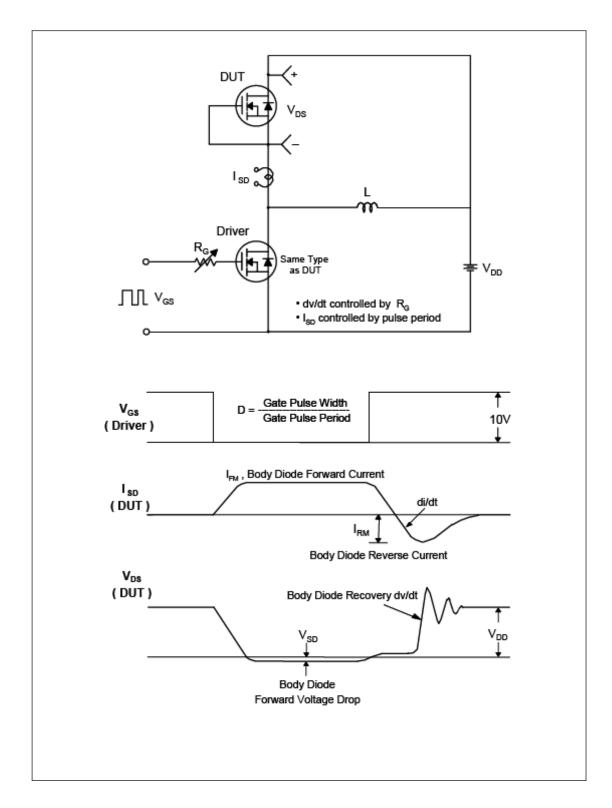


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

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TO-252 Package Dimension

