

Transistors

2.5V Drive Nch+Nch MOS FET

QS6K1

●Structure

Silicon N-channel
MOS FET

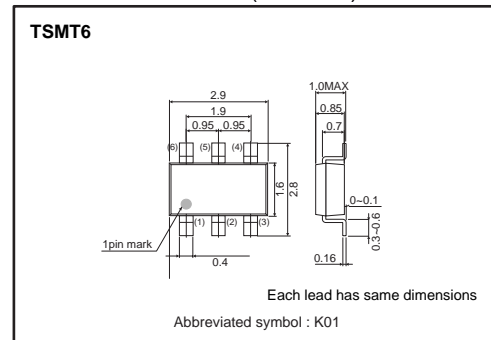
●Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small and Surface Mount Package (TSM T6).

●Application

Power switching, DC / DC converter.

●External dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6K1		○

●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	30	V	
Gate-source voltage	V_{GSS}	12	V	
Drain current	Continuous	I_D	±1.0	A
	Pulsed	I_{DP} *1	±4.0	A
Source current (Body diode)	Continuous	I_S	0.8	A
	Pulsed	I_{SP} *1	4.0	A
Total power dissipation (Tc=25°C)	P_D *2	1.25	W / TOTAL	
		0.9	W / ELEMENT	
Channel temperature	T_{ch}	150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

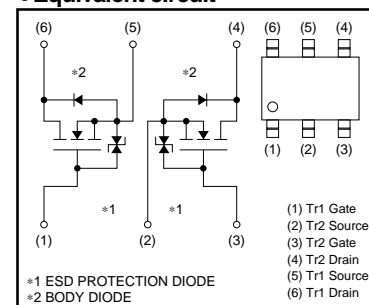
*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$
*2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)$ *	100	°C / W / TOTAL
		139	°C / W / ELEMENT

* Mounted on a ceramic board

●Equivalent circuit



*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

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●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	10	μA	$V_{GS}=12V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	–	–	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.5	–	1.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	170	238	m Ω	$I_D=1.0A, V_{GS}=4.5V$
		–	180	252		$I_D=1.0A, V_{GS}=4.0V$
		–	260	364		$I_D=1.0A, V_{GS}=2.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.0	–	–	S	$I_D=1.0A, V_{DS}=10V$
Input capacitance	C_{iss}	–	77	–	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	–	25	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	–	15	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	7	–	ns	$I_D=500mA, V_{DD} \approx 15V$
Rise time	t_r *	–	7	–	ns	$V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}$ *	–	15	–	ns	$R_L=30.0\Omega$
Fall time	t_f *	–	6	–	ns	$R_G=10\Omega$
Total gate charge	Q_g *	–	1.7	2.4	nC	$V_{DD} \approx 15V$
Gate-source charge	Q_{gs} *	–	0.4	–	nC	$V_{GS}=4.5V$
Gate-drain charge	Q_{gd} *	–	0.4	–	nC	$I_D=1.0A$

*Pulsed

●Body diode characteristics (Source-Drain) (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	1.2	V	$I_S=3.2A, V_{GS}=0V$

*Pulsed

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●Electrical characteristic curves

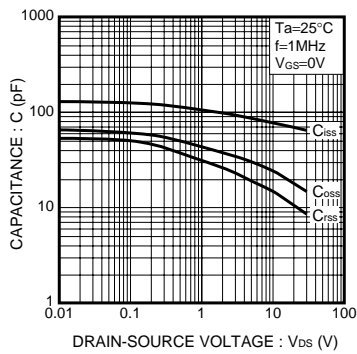


Fig.1 Typical Capacitance vs. Drain-Source Voltage

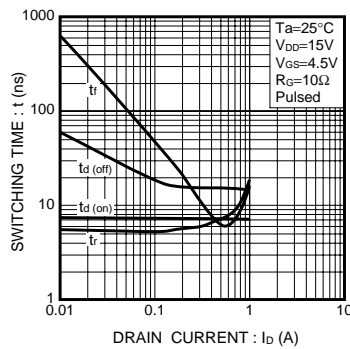


Fig.2 Switching Characteristics

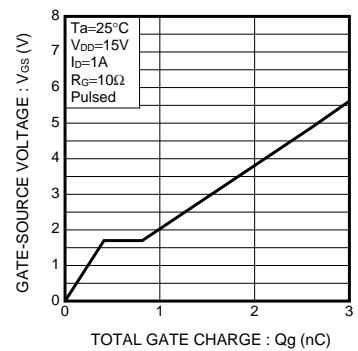


Fig.3 Dynamic Input Characteristics

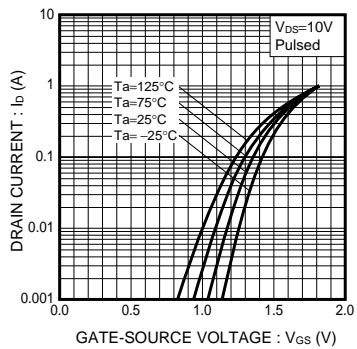


Fig.4 Typical Transfer Characteristics

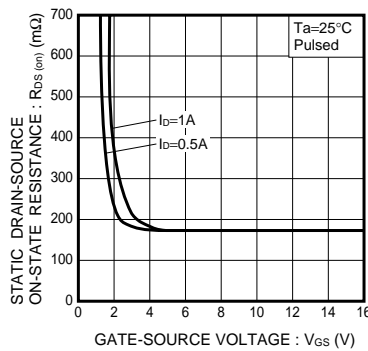


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

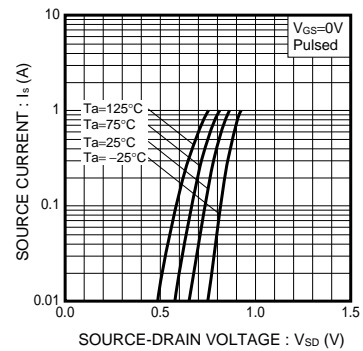


Fig.6 Source Current vs. Source-Drain Voltage

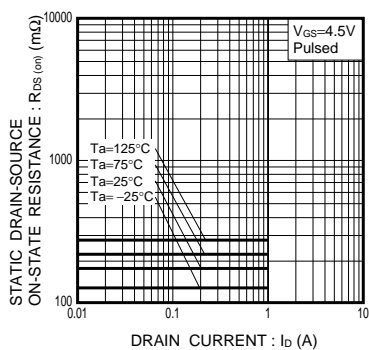


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

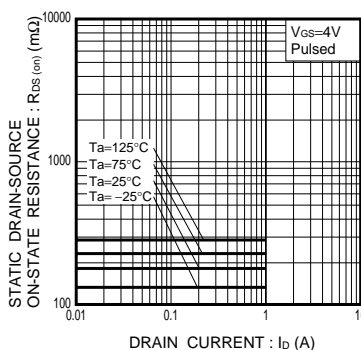


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

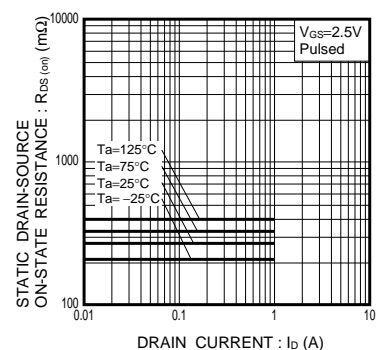


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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